Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	45
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 6x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2142fbd64-151

- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- Up to 21 external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2141FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2142FBD64			
LPC2144FBD64			
LPC2146FBD64			
LPC2148FBD64			

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Endpoint USB RAM	ADC (channels overall)	DAC	Temperature range
LPC2141FBD64	32 kB	8 kB	2 kB	1 (6 channels)	-	−40 °C to +85 °C
LPC2142FBD64	64 kB	16 kB	2 kB	1 (6 channels)	1	−40 °C to +85 °C
LPC2144FBD64	128 kB	16 kB	2 kB	2 (14 channels)	1	−40 °C to +85 °C
LPC2146FBD64	256 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	−40 °C to +85 °C
LPC2148FBD64	512 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	−40 °C to +85 °C

[1] While the USB DMA is the primary user of the additional 8 kB RAM, this RAM is also accessible at any time by the CPU as a general purpose RAM for data and code storage.

5. Pinning information

5.1 Pinning

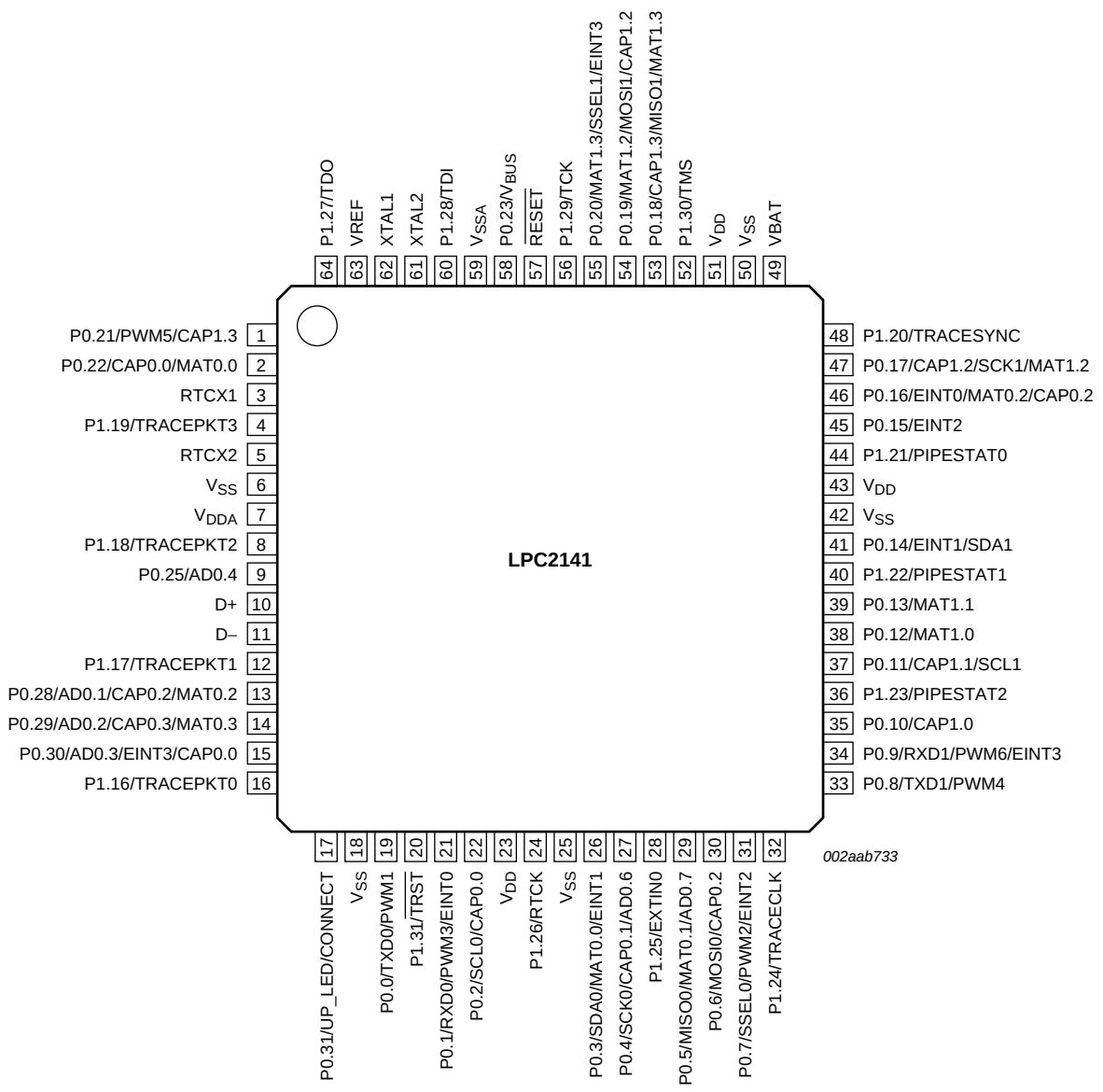

Fig 2. LPC2141 pinning

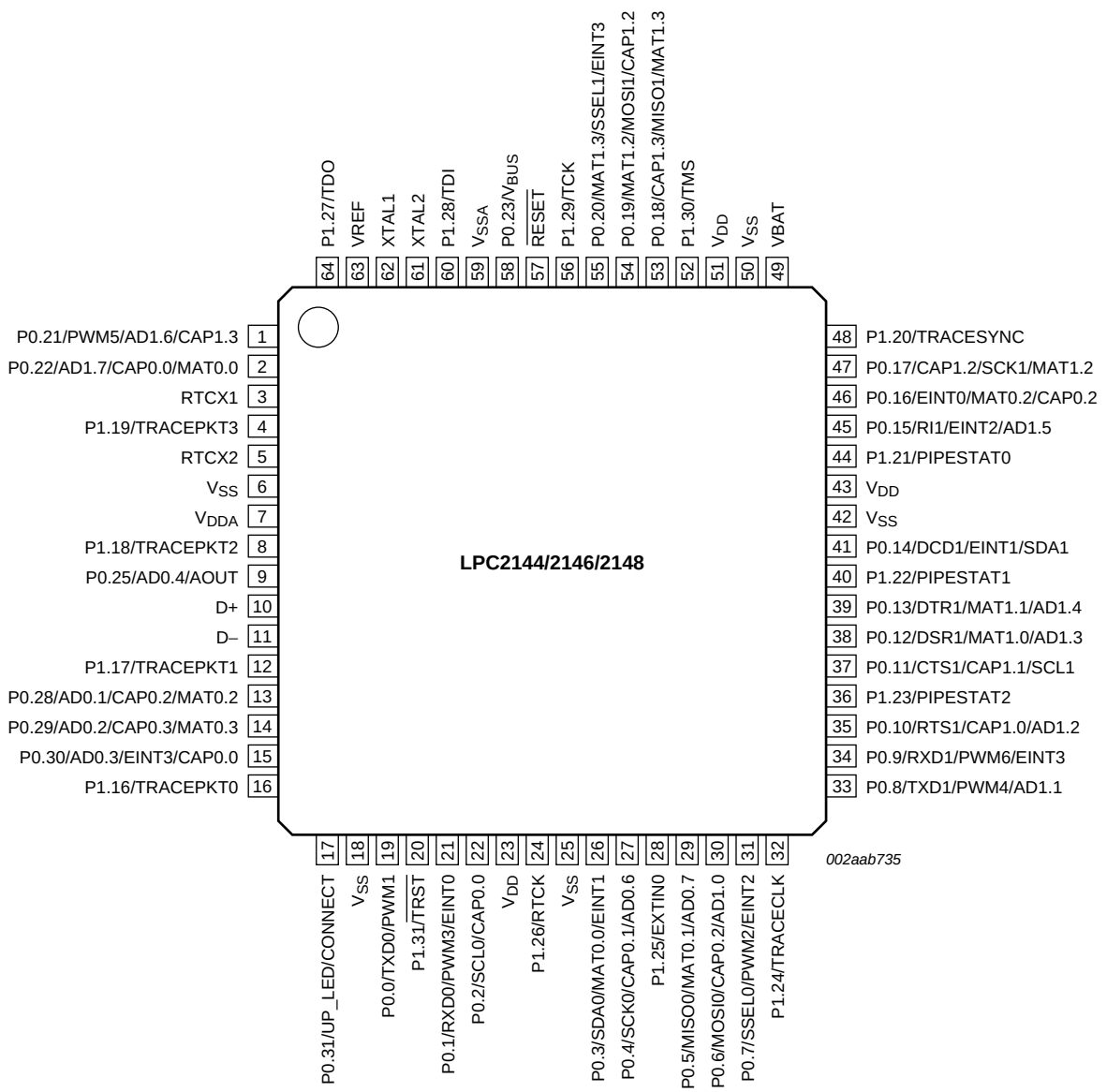

Fig 4. LPC2144/46/48 pinning

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.29/AD0.2/ CAP0.3/MAT0.3	14[4]	I/O	**P0.29 —** General purpose input/output digital pin (GPIO).
		I	**AD0.2 —** ADC 0, input 2.
		I	**CAP0.3 —** Capture input for Timer 0, channel 3.
		O	**MAT0.3 —** Match output for Timer 0, channel 3.
P0.30/AD0.3/ EINT3/CAP0.0	15[4]	I/O	**P0.30 —** General purpose input/output digital pin (GPIO).
		I	**AD0.3 —** ADC 0, input 3.
		I	**EINT3 —** External interrupt 3 input.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.31/UP_LED/ CONNECT	17[6]	O	**P0.31 —** General purpose output only digital pin (GPO).
		O	**UP_LED —** USB GoodLink LED indicator. It is LOW when device is configured (non-control endpoints enabled). It is HIGH when the device is not configured or during global suspend.
		O	**CONNECT —** Signal used to switch an external 1.5 kΩ resistor under the software control. Used with the SoftConnect USB feature. **Important:** This is an digital output only pin. This pin MUST NOT be externally pulled LOW when RESET pin is LOW or the JTAG port will be disabled.
P1.0 to P1.31		I/O	**Port 1:** Port 1 is a 32-bit bidirectional I/O port with individual direction controls for each bit. The operation of port 1 pins depends upon the pin function selected via the pin connect block. Pins 0 through 15 of port 1 are not available.
P1.16/ TRACEPKT0	16[6]	I/O	**P1.16 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT0 —** Trace Packet, bit 0.
P1.17/ TRACEPKT1	12[6]	I/O	**P1.17 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT1 —** Trace Packet, bit 1.
P1.18/ TRACEPKT2	8[6]	I/O	**P1.18 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT2 —** Trace Packet, bit 2.
P1.19/ TRACEPKT3	4[6]	I/O	**P1.19 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACEPKT3 —** Trace Packet, bit 3.
P1.20/ TRACESYNC	48[6]	I/O	**P1.20 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACESYNC —** Trace Synchronization. **Note:** LOW on this pin while RESET is LOW enables pins P1.25:16 to operate as Trace port after reset.
P1.21/ PIPESTAT0	44[6]	I/O	**P1.21 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT0 —** Pipeline Status, bit 0.
P1.22/ PIPESTAT1	40[6]	I/O	**P1.22 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT1 —** Pipeline Status, bit 1.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30 % over Thumb mode.

6.2 On-chip flash program memory

The LPC2141/42/44/46/48 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user's code on LPC2141/42/44/46/48 is 32 kB, 64 kB, 128 kB, 256 kB and 500 kB respectively.

The LPC2141/42/44/46/48 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

In case of LPC2146/48 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

6.4 Memory map

The LPC2141/42/44/46/48 memory map incorporates several distinct regions, as shown in Figure 5.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

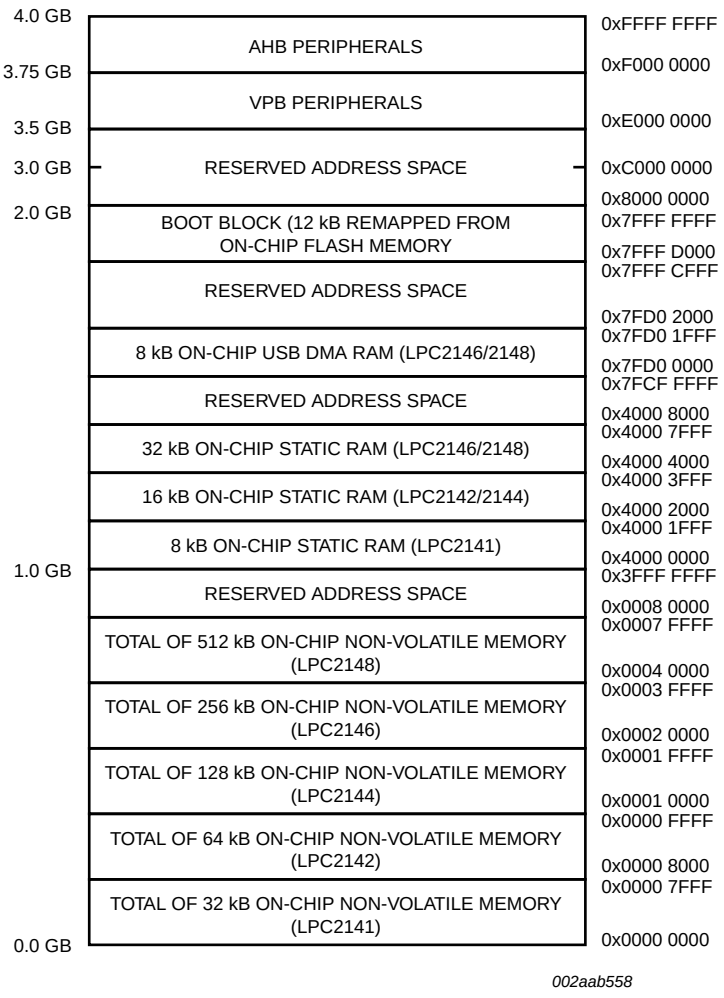

Fig 5. LPC2141/42/44/46/48 memory map

6.7 Fast general purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2141/42/44/46/48 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2141/42 contain one and the LPC2144/46/48 contain two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

6.8.1 Features

- 10 bit successive approximation analog to digital converter.
- Measurement range of 0 V to VREF (2.5 V $\leq$ VREF $\leq$ V_{DDA}).
- Each converter capable of performing more than 400000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters (LPC2142/44/46/48 only).

6.9 10-bit DAC

The DAC enables the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

6.9.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.

- Selectable speed versus power.

6.10 USB 2.0 device controller

The USB is a 4-wire serial bus that supports communication between a host and a number (127 max) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, unplugging, and dynamic configuration of the devices. All transactions are initiated by the host controller.

The LPC2141/42/44/46/48 is equipped with a USB device controller that enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled.

A DMA controller (available in LPC2146/48 only) can transfer data between an endpoint buffer and the USB RAM.

6.10.1 Features

- Fully compliant with USB 2.0 Full-speed specification.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports SoftConnect and GoodLink LED indicator. These two functions are sharing one pin.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints (LPC2146/48 only).
- One duplex DMA channel serves all endpoints (LPC2146/48 only).
- Allows dynamic switching between CPU controlled and DMA modes (only in LPC2146/48).
- Double buffer implementation for bulk and isochronous endpoints.

6.11 UARTs

The LPC2141/42/44/46/48 each contain two UARTs. In addition to standard transmit and receive data lines, the LPC2144/46/48 UART1 also provides a full modem control handshake interface.

Compared to previous LPC2000 microcontrollers, UARTs in LPC2141/42/44/46/48 introduce a fractional baud rate generator for both UARTs, enabling these microcontrollers to achieve standard baud rates such as 115200 with any crystal frequency above 2 MHz. In addition, auto-CTS/RTS flow-control functions are fully implemented in hardware (UART1 in LPC2144/46/48 only).

- Stop timer on match with optional interrupt generation.
- Reset timer on match with optional interrupt generation.

- Four external outputs per timer/counter corresponding to match registers, with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.

6.16 Watchdog timer

The purpose of the watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the watchdog will generate a system reset if the user program fails to 'feed' (or reload) the watchdog within a predetermined amount of time.

6.16.1 Features

- Internally resets chip if not periodically reloaded.
- Debug mode.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/Incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scaler.
- Selectable time period from ($T_{cy(PCLK)} \times 256 \times 4$) to ($T_{cy(PCLK)} \times 2^{32} \times 4$) in multiples of $T_{cy(PCLK)} \times 4$.

6.17 Real-time clock

The RTC is designed to provide a set of counters to measure time when normal or idle operating mode is selected. The RTC has been designed to use little power, making it suitable for battery powered systems where the CPU is not running continuously (Idle mode).

6.17.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra-low power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Can use either the RTC dedicated 32 kHz oscillator input or clock derived from the external crystal/oscillator input at XTAL1. Programmable reference clock divider allows fine adjustment of the RTC.
- Dedicated power supply pin can be connected to a battery or the main 3.3 V.

6.18 Pulse width modulator

The PWM is based on the standard timer block and inherits all of its features, although only the PWM function is pinned out on the LPC2141/42/44/46/48. The timer is designed to count cycles of the peripheral clock (PCLK) and optionally generate interrupts or perform other actions when specified timer values occur, based on seven match registers. The PWM function is also based on match register events.

The ability to separately control rising and falling edge locations allows the PWM to be used for more applications. For instance, multi-phase motor control typically requires three non-overlapping PWM outputs with individual control of all three pulse widths and positions.

Two match registers can be used to provide a single edge controlled PWM output. One match register (MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. Additional single edge controlled PWM outputs require only one match register each, since the repetition rate is the same for all PWM outputs. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when an MR0 match occurs.

Three match registers can be used to provide a PWM output with both edges controlled. Again, the MR0 match register controls the PWM cycle rate. The other match registers control the two PWM edge positions. Additional double edge controlled PWM outputs require only two match registers each, since the repetition rate is the same for all PWM outputs.

With double edge controlled PWM outputs, specific match registers control the rising and falling edge of the output. This allows both positive going PWM pulses (when the rising edge occurs prior to the falling edge), and negative going PWM pulses (when the falling edge occurs prior to the rising edge).

6.18.1 Features

- Seven match registers allow up to six single edge controlled or three double edge controlled PWM outputs, or a mix of both types.
- The match registers also allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Supports single edge controlled and/or double edge controlled PWM outputs. Single edge controlled PWM outputs all go HIGH at the beginning of each cycle unless the output is a constant LOW. Double edge controlled PWM outputs can have either edge occur at any position within a cycle. This allows for both positive going and negative going pulses.
- Pulse period and width can be any number of timer counts. This allows complete flexibility in the trade-off between resolution and repetition rate. All PWM outputs will occur at the same repetition rate.
- Double edge controlled PWM outputs can be programmed to be either positive going or negative going pulses.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage (core and external rail)			−0.5	+3.6	V
V_{DDA}	analog 3.3 V pad supply voltage			−0.5	+4.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT	for the RTC		−0.5	+4.6	V
$V_{i(VREF)}$	input voltage on pin VREF			−0.5	+4.6	V
V_{IA}	analog input voltage	on ADC related pins		−0.5	+5.1	V
V_I	input voltage	5 V tolerant I/O pins; only valid when the V_{DD} supply voltage is present	[2]	−0.5	+6.0	V
		other I/O pins	[2][3]	−0.5	V_{DD} + 0.5	V
I_{DD}	supply current	per supply pin	[4]	-	100	mA
I_{SS}	ground current	per ground pin	[4]	-	100	mA
I_{sink}	sink current	for I^2C-bus; DC; T = 85 °C		-	20	mA
T_{stg}	storage temperature		[5]	−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption		-	1.5	W
V_{esd}	electrostatic discharge voltage	human body model	[6]			
		all pins		−4000	+4000	V

[1] The following applies to the Limiting values:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Including voltage on outputs in 3-state mode.

[3] Not to exceed 4.6 V.

[4] The peak current is limited to 25 times the corresponding maximum current.

[5] Dependent on package type.

[6] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

8. Static characteristics

Table 5. Static characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{DD}	supply voltage		[2]	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.3 V pad		3.0	3.3	3.6	V
$V_{i(VBAT)}$	input voltage on pin VBAT		[3]	2.0	3.3	3.6	V
$V_{i(VREF)}$	input voltage on pin VREF			2.5	3.3	V_{DDA}	V
Standard port pins, $\overline{\text{RESET}}$, P1.26/RTCK							
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down		-	-	3	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down		-	-	3	μA
I_{latch}	I/O latch-up current	$-(0.5V_{DD}) < V_I < (1.5V_{DD})$; T_j < 125 °C		-	-	100	mA
V_I	input voltage	pin configured to provide a digital function	[4][5][6][7]	0	-	5.5	V
V_O	output voltage	output active		0	-	V_{DD}	V
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
V_{hys}	hysteresis voltage			0.4	-	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA	[8]	$V_{DD} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −4 mA	[8]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{OH} = V_{DD} - 0.4$ V	[8]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[8]	4	-	-	mA
I_{OHS}	HIGH-level short-circuit output current	V_{OH} = 0 V	[9]	-	-	−45	mA
I_{OLS}	LOW-level short-circuit output current	$V_{OL} = V_{DDA}$	[9]	-	-	50	mA
I_{pd}	pull-down current	V_I = 5 V	[10]	10	50	150	μA
I_{pu}	pull-up current	V_I = 0 V	[11]	−15	−50	−85	μA
		$V_{DD} < V_I$ < 5 V	[10]	0	0	0	μA

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(act)}$	active mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C; code `while(1){}` executed from flash, no active peripherals		-	15	50	
		CCLK = 10 MHz					mA
		CCLK = 60 MHz		-	40	70	mA
		V_{DD} = 3.3 V; T_{amb} = 25 °C; code executed from flash; USB enabled and active; all other peripherals disabled		-	27	70	
		CCLK = 12 MHz					mA
		CCLK = 60 MHz		-	57	90	mA
$I_{DD(pd)}$	Power-down mode supply current	V_{DD} = 3.3 V; T_{amb} = 25 °C		-	40	100	µA
		V_{DD} = 3.3 V; T_{amb} = 85 °C		-	250	500	µA
I_{BATpd}	Power-down mode battery supply current	RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C	[12]	-	15	30	
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 2.5 V					µA
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V		-	20	40	µA
I_{BATact}	active mode battery supply current	CCLK = 60 MHz; PCLK = 15 MHz; PCLK enabled to RTCK; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C	[12]	-	78	-	
		V_{DD} = 3.0 V; $V_{i(VBAT)}$ = 3.0 V					µA
$I_{BATact(opt)}$	optimized active mode battery supply current	PCLK disabled to RTCK in the PCONP register; RTC clock = 32 kHz (from RTCXn pins); T_{amb} = 25 °C; $V_{i(VBAT)}$ = 3.3 V	[12][13]	-	23	-	
		CCLK = 25 MHz					µA
		CCLK = 60 MHz		-	30	-	µA
I^2C-bus pins							
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.05V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OLS} = 3 mA	[8]	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{DD}$	[14]	-	2	4	µA
		V_I = 5 V		-	10	22	µA
Oscillator pins							
$V_{i(XTAL1)}$	input voltage on pin XTAL1			−0.5	1.8	1.95	V

Table 5. Static characteristics *…continued*

T_{amb} = −40 °C to +85 °C for commercial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$V_{o(XTAL2)}$	output voltage on pin XTAL2		−0.5	1.8	1.95	V
$V_{i(RTCX1)}$	input voltage on pin RTCX1		−0.5	1.8	1.95	V
$V_{o(RTCX2)}$	output voltage on pin RTCX2		−0.5	1.8	1.95	V
USB pins						
I_{OZ}	OFF-state output current	0 V < V_I < 3.3 V	-	-	±10	μA
V_{BUS}	V_{BUS} line input voltage on the USB connector		-	-	5.25	V
V_{DI}	differential input sensitivity	|(D+) − (D−)|	0.2	-	-	V
V_{CM}	differential common-mode range	includes V_{DI} range	0.8	-	2.5	V
$V_{th(rs)se}$	single-ended receiver switching threshold voltage		0.8	-	2.0	V
V_{OL}	LOW output level	R_L of 1.5 kΩ to 3.6 V	-	-	0.3	V
V_{OH}	HIGH output level	R_L of 15 kΩ to GND	2.8	-	3.6	V
C_{trans}	transceiver capacitance	pin to GND	-	-	20	pF
Z_{DRV}	driver output impedance for driver which is not high-speed capable	steady state drive [15]	29	-	44	Ω
R_{pu}	pull-up resistance	SoftConnect = ON	1.1	-	1.9	kΩ

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Core and external rail.

[3] The RTC typically fails when $V_{i(VBAT)}$ drops below 1.6 V.

[4] Including voltage on outputs in 3-state mode.

[5] V_{DD} supply voltages must be present.

[6] 3-state outputs go into 3-state mode when V_{DD} is grounded.

[7] Please also see the errata note mentioned in errata sheet.

[8] Accounts for 100 mV voltage drop in all supply lines.

[9] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

[10] Minimum condition for V_I = 4.5 V, maximum condition for V_I = 5.5 V.

[11] Applies to P1.16 to P1.31.

[12] On pin VBAT.

[13] Optimized for low battery consumption.

[14] To V_{SS}.

[15] Includes external resistors of 33 Ω ± 1 % on D+ and D−.

9. Dynamic characteristics

Table 6. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_r/t_f)	90	-	110	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 7	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 7	−2	-	+5	ns
t_{JR1}	receiver jitter to next transition		−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 7	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 7	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2, P0.3, P0.11, and P0.14)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2, P0.3, P0.11, and P0.14)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

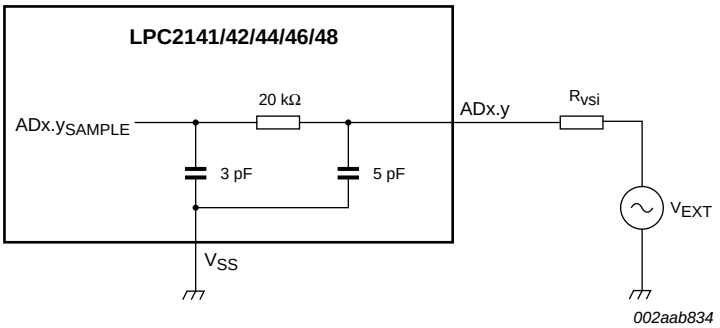

Fig 9. Suggested ADC interface - LPC2141/42/44/46/48 ADx.y pin

11. DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{DDA} = 3.0 V to 3.6 V; T_{amb} = –40 °C to +85 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_D	differential linearity error		-	±1	-	LSB
$E_{L(adj)}$	integral non-linearity		-	±1.5	-	LSB
E_O	offset error		-	0.6	-	%
E_G	gain error		-	0.6	-	%
C_L	load capacitance		-	200	-	pF
R_L	load resistance		1	-	-	kΩ

Table 10. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}/C_{X2}
5 MHz to 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz to 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz to 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 11. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters): high frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz to 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz to 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

12.3 RTC 32 kHz oscillator component selection

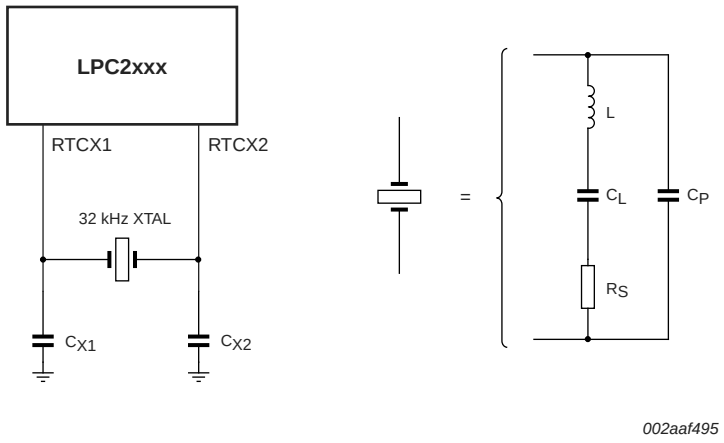

Fig 14. RTC oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

The RTC external oscillator circuit is shown in Figure 14. Since the feedback resistance is integrated on chip, only a crystal, the capacitances C_{X1} and C_{X2} need to be connected externally to the microcontroller.

Table 12 gives the crystal parameters that should be used. C_L is the typical load capacitance of the crystal and is usually specified by the crystal manufacturer. The actual C_L influences oscillation frequency. When using a crystal that is manufactured for a different load capacitance, the circuit will oscillate at a slightly different frequency (depending on the quality of the crystal) compared to the specified one. Therefore for an accurate time reference it is advised to use the load capacitors as specified in Table 12

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2141_42_44_46_48 v.5	20110812	Product data sheet	-	LPC2141_42_44_46_48 v.4
Modifications:	• Table 3 “Pin description”: Added Table note [10] to RTCX1 and RTCX2 pins. • Table 4 “Limiting values”: Added parameter I_{sink}. • Table 5 “Static characteristics”, I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 5 “Static characteristics”: Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Table 5 “Static characteristics”: Updated Table note [15]. • Added Section 11 “DAC electrical characteristics”. • Added Section 12.2 “Crystal oscillator XTAL input and component selection”. • Added Section 12.3 “RTC 32 kHz oscillator component selection”. • Added Section 12.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Updated Figure 8 “ADC characteristics”.			
LPC2141_42_44_46_48 v.4	20081117	Product data sheet	-	LPC2141_42_44_46_48 v.3
Modifications:	• Replaced all occurrences of VPB with APB. • Table 3: clarified which pins do/don’t have internal pull-ups. • Table 4: changed storage temperature range from −40 °C/125 °C to −65 °C/150 °C. • Table 5: added Table note 7 to input voltage spec. • Table 5: modified Table note 9. • Table 5: moved hysteresis voltage (0.4 V) from typ to min column. • Figure 8: updated figure and figure title, removed note			
LPC2141_42_44_46_48 v.3	20071019	Product data sheet	-	LPC2141_42_44_46_48 v.2
LPC2141_42_44_46_48 v.2	20060828	Product data sheet	-	LPC2141_42_44_46_48 v.1
LPC2141_42_44_46_48 v.1	20051003	Preliminary data sheet	-	-

18. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 12 August 2011
Document identifier: LPC2141_42_44_46_48