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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	60MHz
Connectivity	I²C, Microwire, SPI, SSI, SSP, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 14x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc2146fbd64-151

- Multiple serial interfaces including two UARTs (16C550), two Fast I^2C-bus (400 kbit/s), SPI and SSP with buffering and variable data length capabilities.
- Vectored Interrupt Controller (VIC) with configurable priorities and vector addresses.
- Up to 45 of 5 V tolerant fast general purpose I/O pins in a tiny LQFP64 package.
- Up to 21 external interrupt pins available.
- 60 MHz maximum CPU clock available from programmable on-chip PLL with settling time of 100 μs.
- On-chip integrated oscillator operates with an external crystal from 1 MHz to 25 MHz.
- Power saving modes include Idle and Power-down.
- Individual enable/disable of peripheral functions as well as peripheral clock scaling for additional power optimization.
- Processor wake-up from Power-down mode via external interrupt or BOD.
- Single power supply chip with POR and BOD circuits:
  - CPU operating voltage range of 3.0 V to 3.6 V (3.3 V ± 10 %) with 5 V tolerant I/O pads.

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC2141FBD64	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2
LPC2142FBD64			
LPC2144FBD64			
LPC2146FBD64			
LPC2148FBD64			

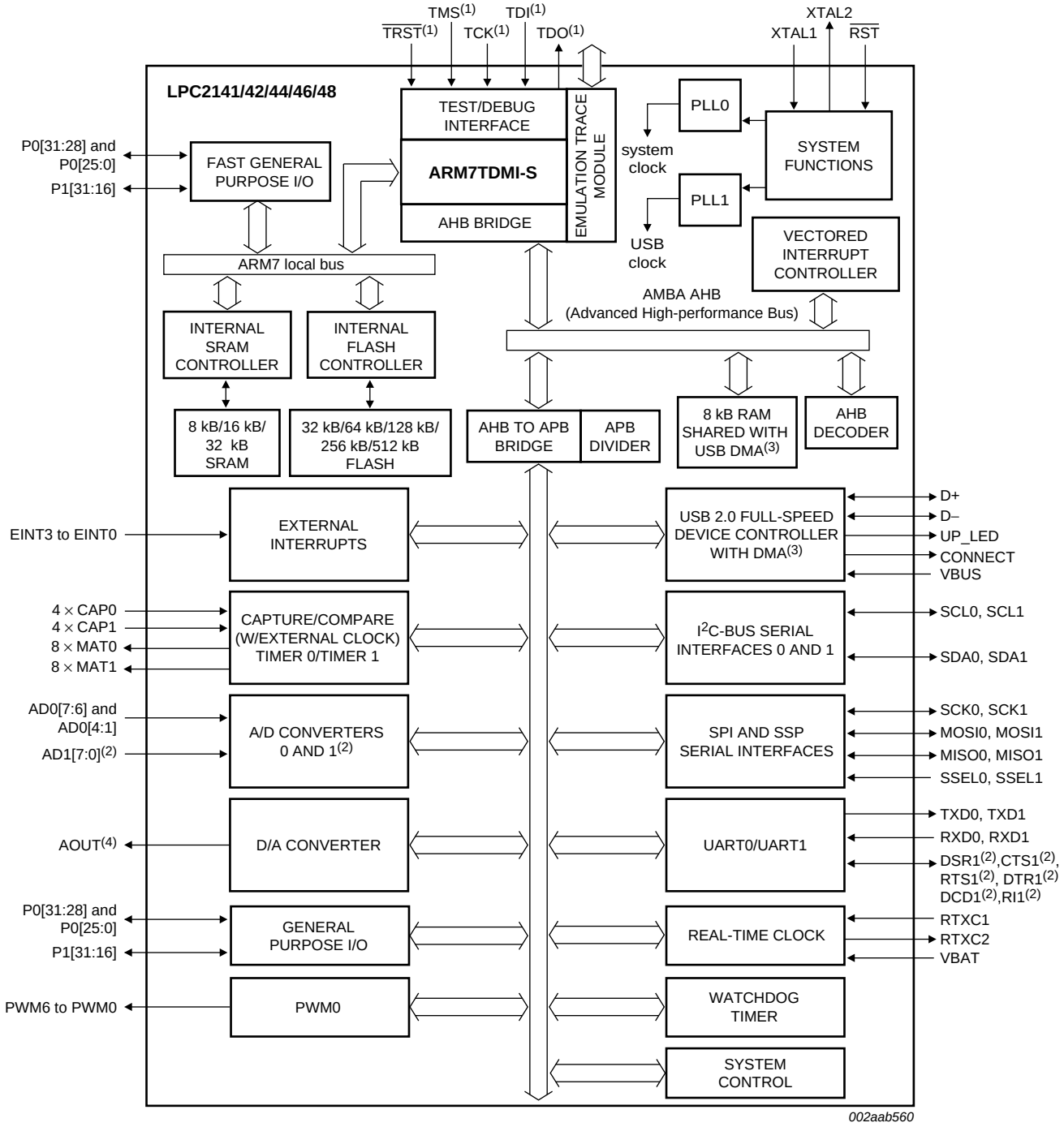
3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Endpoint USB RAM	ADC (channels overall)	DAC	Temperature range
LPC2141FBD64	32 kB	8 kB	2 kB	1 (6 channels)	-	−40 °C to +85 °C
LPC2142FBD64	64 kB	16 kB	2 kB	1 (6 channels)	1	−40 °C to +85 °C
LPC2144FBD64	128 kB	16 kB	2 kB	2 (14 channels)	1	−40 °C to +85 °C
LPC2146FBD64	256 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	−40 °C to +85 °C
LPC2148FBD64	512 kB	32 kB + 8 kB shared with USB DMA[1]	2 kB	2 (14 channels)	1	−40 °C to +85 °C

[1] While the USB DMA is the primary user of the additional 8 kB RAM, this RAM is also accessible at any time by the CPU as a general purpose RAM for data and code storage.

4. Block diagram



(1) Pins shared with GPIO.

(2) LPC2144/46/48 only.

(3) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2146/48 only.

(4) LPC2142/44/46/48 only.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning

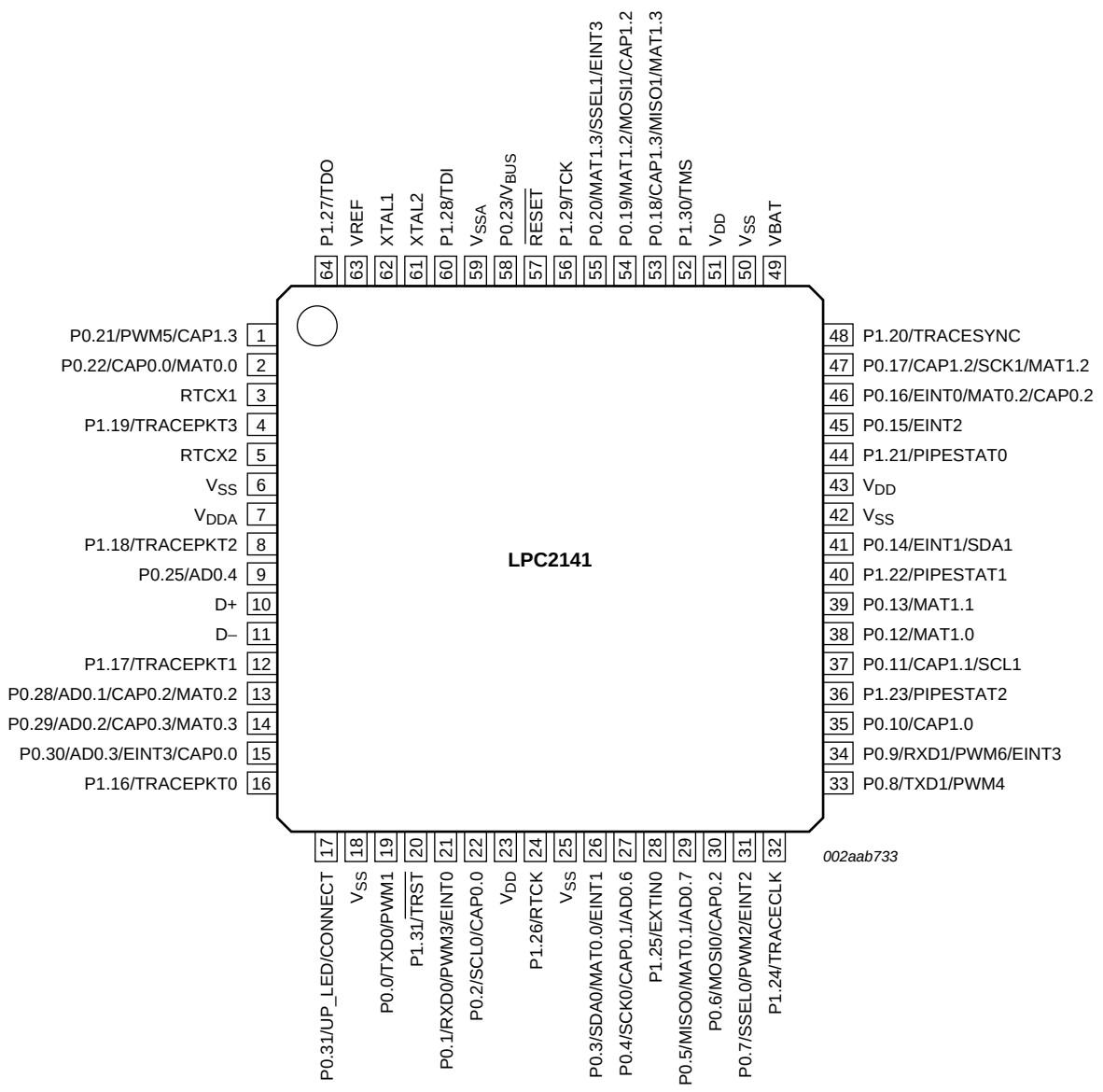


Fig 2. LPC2141 pinning

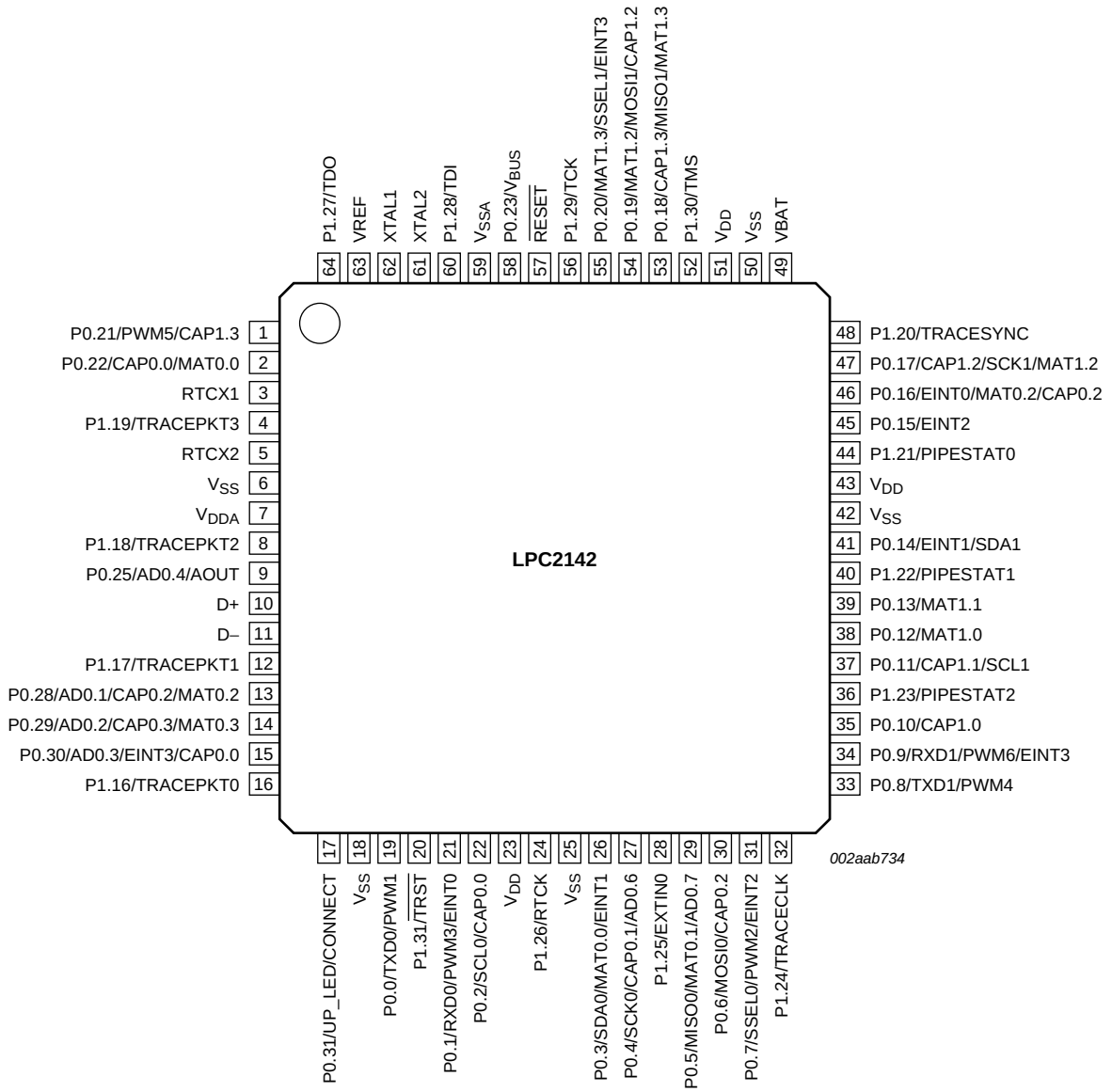


Fig 3. LPC2142 pinning

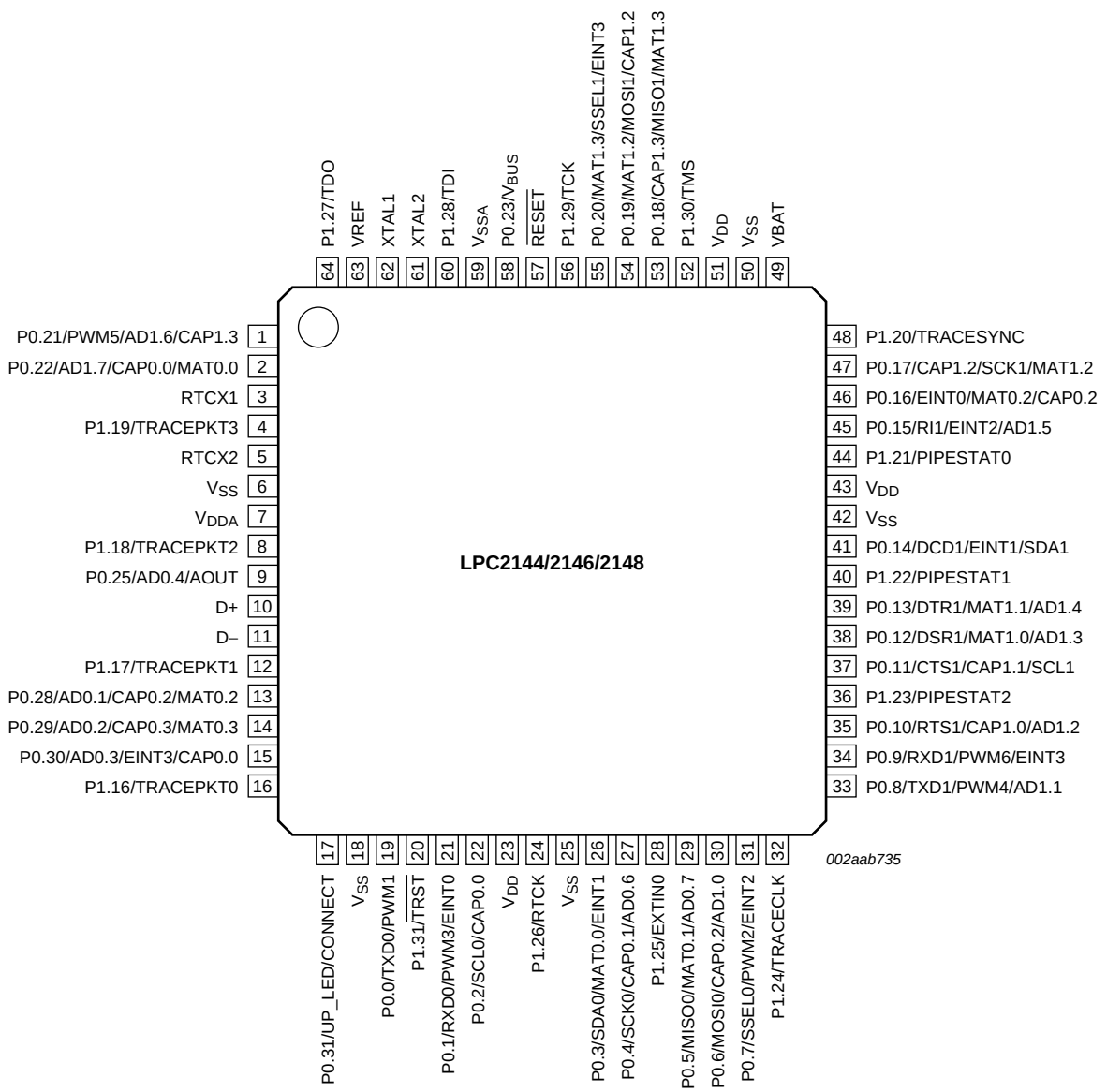


Fig 4. LPC2144/46/48 pinning

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description
P0.0 to P0.31		I/O	**Port 0:** Port 0 is a 32-bit I/O port with individual direction controls for each bit. Total of 31 pins of the Port 0 can be used as a general purpose bidirectional digital I/Os while P0.31 is output only pin. The operation of port 0 pins depends upon the pin function selected via the pin connect block. Pins P0.24, P0.26 and P0.27 are not available.
P0.0/TXD0/ PWM1	19[1]	I/O	**P0.0 —** General purpose input/output digital pin (GPIO).
		O	**TXD0 —** Transmitter output for UART0.
		O	**PWM1 —** Pulse Width Modulator output 1.
P0.1/RXD0/ PWM3/EINT0	21[2]	I/O	**P0.1 —** General purpose input/output digital pin (GPIO).
		I	**RXD0 —** Receiver input for UART0.
		O	**PWM3 —** Pulse Width Modulator output 3.
		I	**EINT0 —** External interrupt 0 input.
P0.2/SCL0/ CAP0.0	22[3]	I/O	**P0.2 —** General purpose input/output digital pin (GPIO).
		I/O	**SCL0 —** I^2C0 clock input/output. Open-drain output (for I^2C-bus compliance).
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
P0.3/SDA0/ MAT0.0/EINT1	26[3]	I/O	**P0.3 —** General purpose input/output digital pin (GPIO).
		I/O	**SDA0 —** I^2C0 data input/output. Open-drain output (for I^2C-bus compliance).
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
		I	**EINT1 —** External interrupt 1 input.
P0.4/SCK0/ CAP0.1/AD0.6	27[4]	I/O	**P0.4 —** General purpose input/output digital pin (GPIO).
		I/O	**SCK0 —** Serial clock for SPI0. SPI clock output from master or input to slave.
		I	**CAP0.1 —** Capture input for Timer 0, channel 1.
		I	**AD0.6 —** ADC 0, input 6.
P0.5/MISO0/ MAT0.1/AD0.7	29[4]	I/O	**P0.5 —** General purpose input/output digital pin (GPIO).
		I/O	**MISO0 —** Master In Slave Out for SPI0. Data input to SPI master or data output from SPI slave.
		O	**MAT0.1 —** Match output for Timer 0, channel 1.
		I	**AD0.7 —** ADC 0, input 7.
P0.6/MOSI0/ CAP0.2/AD1.0	30[4]	I/O	**P0.6 —** General purpose input/output digital pin (GPIO).
		I/O	**MOSI0 —** Master Out Slave In for SPI0. Data output from SPI master or data input to SPI slave.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		I	**AD1.0 —** ADC 1, input 0. Available in LPC2144/46/48 only.
P0.7/SSEL0/ PWM2/EINT2	31[2]	I/O	**P0.7 —** General purpose input/output digital pin (GPIO).
		I	**SSEL0 —** Slave Select for SPI0. Selects the SPI interface as a slave.
		O	**PWM2 —** Pulse Width Modulator output 2.
		I	**EINT2 —** External interrupt 2 input.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.8/TXD1/ PWM4/AD1.1	33[4]	I/O	**P0.8 —** General purpose input/output digital pin (GPIO).
		O	**TXD1 —** Transmitter output for UART1.
		O	**PWM4 —** Pulse Width Modulator output 4.
		I	**AD1.1 —** ADC 1, input 1. Available in LPC2144/46/48 only.
P0.9/RXD1/ PWM6/EINT3	34[2]	I/O	**P0.9 —** General purpose input/output digital pin (GPIO).
		I	**RXD1 —** Receiver input for UART1.
		O	**PWM6 —** Pulse Width Modulator output 6.
		I	**EINT3 —** External interrupt 3 input.
P0.10/RTS1/ CAP1.0/AD1.2	35[4]	I/O	**P0.10 —** General purpose input/output digital pin (GPIO).
		O	**RTS1 —** Request to Send output for UART1. LPC2144/46/48 only.
		I	**CAP1.0 —** Capture input for Timer 1, channel 0.
		I	**AD1.2 —** ADC 1, input 2. Available in LPC2144/46/48 only.
P0.11/CTS1/ CAP1.1/SCL1	37[3]	I/O	**P0.11 —** General purpose input/output digital pin (GPIO).
		I	**CTS1 —** Clear to Send input for UART1. Available in LPC2144/46/48 only.
		I	**CAP1.1 —** Capture input for Timer 1, channel 1.
		I/O	**SCL1 —** I^2C1 clock input/output. Open-drain output (for I^2C-bus compliance)
P0.12/DSR1/ MAT1.0/AD1.3	38[4]	I/O	**P0.12 —** General purpose input/output digital pin (GPIO).
		I	**DSR1 —** Data Set Ready input for UART1. Available in LPC2144/46/48 only.
		O	**MAT1.0 —** Match output for Timer 1, channel 0.
		I	**AD1.3 —** ADC 1 input 3. Available in LPC2144/46/48 only.
P0.13/DTR1/ MAT1.1/AD1.4	39[4]	I/O	**P0.13 —** General purpose input/output digital pin (GPIO).
		O	**DTR1 —** Data Terminal Ready output for UART1. LPC2144/46/48 only.
		O	**MAT1.1 —** Match output for Timer 1, channel 1.
		I	**AD1.4 —** ADC 1 input 4. Available in LPC2144/46/48 only.
P0.14/DCD1/ EINT1/SDA1	41[3]	I/O	**P0.14 —** General purpose input/output digital pin (GPIO).
		I	**DCD1 —** Data Carrier Detect input for UART1. LPC2144/46/48 only.
		I	**EINT1 —** External interrupt 1 input.
		I/O	**SDA1 —** I^2C1 data input/output. Open-drain output (for I^2C-bus compliance). **Note:** LOW on this pin while $\overline{\text{RESET}}$ is LOW forces on-chip boot loader to take over control of the part after reset.
P0.15/RI1/ EINT2/AD1.5	45[4]	I/O	**P0.15 —** General purpose input/output digital pin (GPIO).
		I	**RI1 —** Ring Indicator input for UART1. Available in LPC2144/46/48 only.
		I	**EINT2 —** External interrupt 2 input.
		I	**AD1.5 —** ADC 1, input 5. Available in LPC2144/46/48 only.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P0.16/EINT0/ MAT0.2/CAP0.2	46[2]	I/O	**P0.16 —** General purpose input/output digital pin (GPIO).
		I	**EINT0 —** External interrupt 0 input.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
P0.17/CAP1.2/ SCK1/MAT1.2	47[1]	I/O	**P0.17 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
		I/O	**SCK1 —** Serial Clock for SSP. Clock output from master or input to slave.
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
P0.18/CAP1.3/ MISO1/MAT1.3	53[1]	I/O	**P0.18 —** General purpose input/output digital pin (GPIO).
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
		I/O	**MISO1 —** Master In Slave Out for SSP. Data input to SPI master or data output from SSP slave.
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
P0.19/MAT1.2/ MOSI1/CAP1.2	54[1]	I/O	**P0.19 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.2 —** Match output for Timer 1, channel 2.
		I/O	**MOSI1 —** Master Out Slave In for SSP. Data output from SSP master or data input to SSP slave.
		I	**CAP1.2 —** Capture input for Timer 1, channel 2.
P0.20/MAT1.3/ SSEL1/EINT3	55[2]	I/O	**P0.20 —** General purpose input/output digital pin (GPIO).
		O	**MAT1.3 —** Match output for Timer 1, channel 3.
		I	**SSEL1 —** Slave Select for SSP. Selects the SSP interface as a slave.
		I	**EINT3 —** External interrupt 3 input.
P0.21/PWM5/ AD1.6/CAP1.3	1[4]	I/O	**P0.21 —** General purpose input/output digital pin (GPIO).
		O	**PWM5 —** Pulse Width Modulator output 5.
		I	**AD1.6 —** ADC 1, input 6. Available in LPC2144/46/48 only.
		I	**CAP1.3 —** Capture input for Timer 1, channel 3.
P0.22/AD1.7/ CAP0.0/MAT0.0	2[4]	I/O	**P0.22 —** General purpose input/output digital pin (GPIO).
		I	**AD1.7 —** ADC 1, input 7. Available in LPC2144/46/48 only.
		I	**CAP0.0 —** Capture input for Timer 0, channel 0.
		O	**MAT0.0 —** Match output for Timer 0, channel 0.
P0.23/V_{BUS}	58[1]	I/O	**P0.23 —** General purpose input/output digital pin (GPIO).
		I	**V_{BUS} —** Indicates the presence of USB bus power. **Note:** This signal must be HIGH for USB reset to occur.
P0.25/AD0.4/ AOUT	9[5]	I/O	**P0.25 —** General purpose input/output digital pin (GPIO).
		I	**AD0.4 —** ADC 0, input 4.
		O	**AOUT —** DAC output. Available in LPC2142/44/46/48 only.
P0.28/AD0.1/ CAP0.2/MAT0.2	13[4]	I/O	**P0.28 —** General purpose input/output digital pin (GPIO).
		I	**AD0.1 —** ADC 0, input 1.
		I	**CAP0.2 —** Capture input for Timer 0, channel 2.
		O	**MAT0.2 —** Match output for Timer 0, channel 2.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
P1.23/ PIPESTAT2	36[6]	I/O	**P1.23 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**PIPESTAT2 —** Pipeline Status, bit 2.
P1.24/ TRACECLK	32[6]	I/O	**P1.24 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		O	**TRACECLK —** Trace Clock.
P1.25/EXTIN0	28[6]	I/O	**P1.25 —** General purpose input/output digital pin (GPIO). Standard I/O port with internal pull-up.
		I	**EXTIN0 —** External Trigger Input.
P1.26/RTCK	24[6]	I/O	**P1.26 —** General purpose input/output digital pin (GPIO).
		I/O	**RTCK —** Returned Test Clock output. Extra signal added to the JTAG port. Assists debugger synchronization when processor frequency varies. Bidirectional pin with internal pull-up. **Note:** LOW on RTCK while $\overline{\text{RESET}}$ is LOW enables pins P1[31:26] to operate as Debug port after reset.
P1.27/TDO	64[6]	I/O	**P1.27 —** General purpose input/output digital pin (GPIO).
		O	**TDO —** Test Data out for JTAG interface.
P1.28/TDI	60[6]	I/O	**P1.28 —** General purpose input/output digital pin (GPIO).
		I	**TDI —** Test Data in for JTAG interface.
P1.29/TCK	56[6]	I/O	**P1.29 —** General purpose input/output digital pin (GPIO).
		I	**TCK —** Test Clock for JTAG interface. This clock must be slower than $^{1}?_{6}$ of the CPU clock (CCLK) for the JTAG interface to operate.
P1.30/TMS	52[6]	I/O	**P1.30 —** General purpose input/output digital pin (GPIO).
		I	**TMS —** Test Mode Select for JTAG interface.
P1.31/$\overline{\text{TRST}}$	20[6]	I/O	**P1.31 —** General purpose input/output digital pin (GPIO).
		I	**$\overline{\text{TRST}}$ —** Test Reset for JTAG interface.
D+	10[7]	I/O	USB bidirectional D+ line.
D−	11[7]	I/O	USB bidirectional D− line.
$\overline{\text{RESET}}$	57[8]	I	**External reset input:** A LOW on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. TTL with hysteresis, 5 V tolerant.
XTAL1	62[9]	I	Input to the oscillator circuit and internal clock generator circuits.
XTAL2	61[9]	O	Output from the oscillator amplifier.
RTCX1	3[9][10]	I	Input to the RTC oscillator circuit.
RTCX2	5[9][10]	O	Output from the RTC oscillator circuit.
V_{SS}	6, 18, 25, 42, 50	I	**Ground:** 0 V reference.
V_{SSA}	59	I	**Analog ground:** 0 V reference. This should nominally be the same voltage as V_{SS}, but should be isolated to minimize noise and error.
V_{DD}	23, 43, 51	I	**3.3 V power supply:** This is the power supply voltage for the core and I/O ports.

Table 3. Pin description *…continued*

Symbol	Pin	Type	Description
V_{DDA}	7	I	**Analog 3.3 V power supply:** This should be nominally the same voltage as V_{DD} but should be isolated to minimize noise and error. This voltage is only used to power the on-chip ADC(s) and DAC.
VREF	63	I	**ADC reference voltage:** This should be nominally less than or equal to the V_{DD} voltage but should be isolated to minimize noise and error. Level on this pin is used as a reference for ADC(s) and DAC.
VBAT	49	I	**RTC power supply voltage:** 3.3 V on this pin supplies the power to the RTC.

[1] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control.

[2] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns.

[3] Open-drain 5 V tolerant digital I/O I^2C-bus 400 kHz specification compatible pad. It requires external pull-up to provide an output functionality.

[4] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog input function. If configured for an input function, this pad utilizes built-in glitch filter that blocks pulses shorter than 3 ns. When configured as an ADC input, digital section of the pad is disabled.

[5] 5 V tolerant pad (no built-in pull-up resistor) providing digital I/O (with TTL levels and hysteresis and 10 ns slew rate control) and analog output function. When configured as the DAC output, digital section of the pad is disabled.

[6] 5 V tolerant pad with built-in pull-up resistor providing digital I/O functions with TTL levels and hysteresis and 10 ns slew rate control. The pull-up resistor's value typically ranges from 60 kΩ to 300 kΩ.

[7] Pad is designed in accordance with the Universal Serial Bus (USB) specification, revision 2.0 (Full-speed and Low-speed mode only).

[8] 5 V tolerant pad providing digital input (with TTL levels and hysteresis) function only.

[9] Pad provides special analog functionality.

[10] When unused, the RTCX1 pin can be grounded or left floating. For lowest power leave it floating.
The other RTC pin, RTCX2, should be left floating.

6. Functional description

6.1 Architectural overview

The ARM7TDMI-S is a general purpose 32-bit microprocessor, which offers high performance and very low power consumption. The ARM architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed Complex Instruction Set Computers (CISC). This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI-S processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI-S processor has two instruction sets:

- The standard 32-bit ARM set.
- A 16-bit Thumb set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide up to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The particular flash implementation in the LPC2141/42/44/46/48 allows for full speed execution also in ARM mode. It is recommended to program performance critical and short code sections (such as interrupt service routines and DSP algorithms) in ARM mode. The impact on the overall code size will be minimal but the speed can be increased by 30 % over Thumb mode.

6.2 On-chip flash program memory

The LPC2141/42/44/46/48 incorporate a 32 kB, 64 kB, 128 kB, 256 kB and 512 kB flash memory system respectively. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the serial port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc. Due to the architectural solution chosen for an on-chip boot loader, flash memory available for user's code on LPC2141/42/44/46/48 is 32 kB, 64 kB, 128 kB, 256 kB and 500 kB respectively.

The LPC2141/42/44/46/48 flash memory provides a minimum of 100000 erase/write cycles and 20 years of data-retention.

6.3 On-chip static RAM

On-chip static RAM may be used for code and/or data storage. The SRAM may be accessed as 8-bit, 16-bit, and 32-bit. The LPC2141, LPC2142/44 and LPC2146/48 provide 8 kB, 16 kB and 32 kB of static RAM respectively.

In case of LPC2146/48 only, an 8 kB SRAM block intended to be utilized mainly by the USB can also be used as a general purpose RAM for data storage and code storage and execution.

6.4 Memory map

The LPC2141/42/44/46/48 memory map incorporates several distinct regions, as shown in Figure 5.

In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash memory (the default) or on-chip static RAM. This is described in Section 6.19 “System control”.

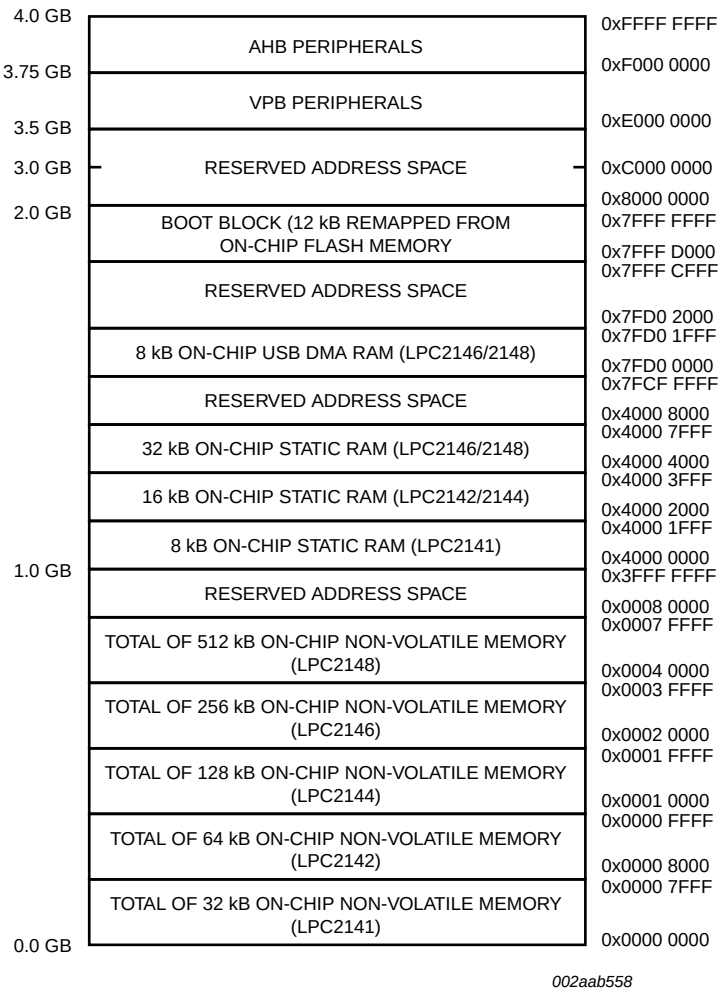


Fig 5. LPC2141/42/44/46/48 memory map

6.5 Interrupt controller

The Vectored Interrupt Controller (VIC) accepts all of the interrupt request inputs and categorizes them as Fast Interrupt reQuest (FIQ), vectored Interrupt ReQuest (IRQ), and non-vectored IRQ as defined by programmable settings. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the VIC combines the requests to produce the FIQ signal to the ARM processor. The fastest possible FIQ latency is achieved when only one request is classified as FIQ, because then the FIQ service routine does not need to branch into the interrupt service routine but can run from the interrupt vector location. If more than one request is assigned to the FIQ class, the FIQ service routine will read a word from the VIC that identifies which FIQ source(s) is (are) requesting an interrupt.

Vectored IRQs have the middle priority. Sixteen of the interrupt requests can be assigned to this category. Any of the interrupt requests can be assigned to any of the 16 vectored IRQ slots, among which slot 0 has the highest priority and slot 15 has the lowest.

Non-vectored IRQs have the lowest priority.

The VIC combines the requests from all the vectored and non-vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the VIC and jumping there. If any of the vectored IRQs are pending, the VIC provides the address of the highest-priority requesting IRQs service routine, otherwise it provides the address of a default routine that is shared by all the non-vectored IRQs. The default routine can read another VIC register to see what IRQs are active.

6.5.1 Interrupt sources

Each peripheral device has one interrupt line connected to the Vectored Interrupt Controller, but may have several internal interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

6.6 Pin connect block

The pin connect block allows selected pins of the microcontroller to have more than one function. Configuration registers control the multiplexers to allow connection between the pin and the on chip peripherals. Peripherals should be connected to the appropriate pins prior to being activated, and prior to any related interrupt(s) being enabled. Activity of any enabled peripheral function that is not mapped to a related pin should be considered undefined.

The Pin Control Module with its pin select registers defines the functionality of the microcontroller in a given hardware environment.

After reset all pins of Port 0 and Port 1 are configured as input with the following exceptions: If debug is enabled, the JTAG pins will assume their JTAG functionality; if trace is enabled, the Trace pins will assume their trace functionality. The pins associated with the I^2C0 and I^2C1 interface are open drain.

6.7 Fast general purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The value of the output register may be read back, as well as the current state of the port pins.

LPC2141/42/44/46/48 introduce accelerated GPIO functions over prior LPC2000 devices:

- GPIO registers are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask registers allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO registers are byte addressable.
- Entire port value can be written in one instruction.

6.7.1 Features

- Bit-level set and clear registers allow a single instruction set or clear of any number of bits in one port.
- Direction control of individual bits.
- Separate control of output set and clear.
- All I/O default to inputs after reset.

6.8 10-bit ADC

The LPC2141/42 contain one and the LPC2144/46/48 contain two analog to digital converters. These converters are single 10-bit successive approximation analog to digital converters. While ADC0 has six channels, ADC1 has eight channels. Therefore, total number of available ADC inputs for LPC2141/42 is 6 and for LPC2144/46/48 is 14.

6.8.1 Features

- 10 bit successive approximation analog to digital converter.
- Measurement range of 0 V to VREF (2.5 V $\leq$ VREF $\leq$ V_{DDA}).
- Each converter capable of performing more than 400000 10-bit samples per second.
- Every analog input has a dedicated result register to reduce interrupt overhead.
- Burst conversion mode for single or multiple inputs.
- Optional conversion on transition on input pin or timer match signal.
- Global Start command for both converters (LPC2142/44/46/48 only).

6.9 10-bit DAC

The DAC enables the LPC2141/42/44/46/48 to generate a variable analog output. The maximum DAC output voltage is the VREF voltage.

6.9.1 Features

- 10-bit DAC.
- Buffered output.
- Power-down mode available.

6.11.1 Features

- 16 B Receive and Transmit FIFOs.
- Register locations conform to 16C550 industry standard.
- Receiver FIFO trigger points at 1 B, 4 B, 8 B, and 14 B
- Built-in fractional baud rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of software (XON/XOFF) flow control on both UARTs.
- LPC2144/46/48 UART1 equipped with standard modem interface signals. This module also provides full support for hardware flow control (auto-CTS/RTS).

6.12 I^2C-bus serial I/O controller

The LPC2141/42/44/46/48 each contain two I^2C-bus controllers.

The I^2C-bus is bidirectional, for inter-IC control using only two wires: a Serial Clock Line (SCL), and a Serial DAta line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver or a transmitter with the capability to both receive and send information (such as memory)). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C-bus is a multi-master bus, it can be controlled by more than one bus master connected to it.

The I^2C-bus implemented in LPC2141/42/44/46/48 supports bit rates up to 400 kbit/s (Fast I^2C-bus).

6.12.1 Features

- Compliant with standard I^2C-bus interface.
- Easy to configure as master, slave, or master/slave.
- Programmable clocks allow versatile rate control.
- Bidirectional data transfer between masters and slaves.
- Multi-master bus (no central master).
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- The I^2C-bus can be used for test and diagnostic purposes.

6.13 SPI serial I/O controller

The LPC2141/42/44/46/48 each contain one SPI controller. The SPI is a full duplex serial interface, designed to handle multiple masters and slaves connected to a given bus. Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master.

9. Dynamic characteristics

Table 6. Dynamic characteristics of USB pins (full-speed)

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to V_{DD}, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	10 % to 90 %	4	-	20	ns
t_f	fall time	10 % to 90 %	4	-	20	ns
t_{FRFM}	differential rise and fall time matching	(t_r/t_f)	90	-	110	%
V_{CRS}	output signal crossover voltage		1.3	-	2.0	V
t_{FEOPT}	source SE0 interval of EOP	see Figure 7	160	-	175	ns
t_{FDEOP}	source jitter for differential transition to SE0 transition	see Figure 7	−2	-	+5	ns
t_{JR1}	receiver jitter to next transition		−18.5	-	+18.5	ns
t_{JR2}	receiver jitter for paired transitions	10 % to 90 %	−9	-	+9	ns
t_{EOPR1}	EOP width at receiver	must reject as EOP; see Figure 7	[1] 40	-	-	ns
t_{EOPR2}	EOP width at receiver	must accept as EOP; see Figure 7	[1] 82	-	-	ns

[1] Characterized but not implemented as production test. Guaranteed by design.

Table 7. Dynamic characteristics

T_{amb} = −40 °C to +85 °C for commercial applications, V_{DD} over specified ranges[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
External clock						
f_{osc}	oscillator frequency		10	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	100	ns
t_{CHCX}	clock HIGH time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCX}	clock LOW time		$T_{cy(clk)} \times 0.4$	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns
Port pins (except P0.2, P0.3, P0.11, and P0.14)						
$t_{r(o)}$	output rise time		-	10	-	ns
$t_{f(o)}$	output fall time		-	10	-	ns
I^2C-bus pins (P0.2, P0.3, P0.11, and P0.14)						
$t_{f(o)}$	output fall time	V_{IH} to V_{IL}	$20 + 0.1 \times C_b$[3]	-	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[3] Bus capacitance C_b in pF, from 10 pF to 400 pF.

10. ADC electrical characteristics

Table 8. ADC static characteristics

V_{DDA} = 2.5 V to 3.6 V; T_{amb} = −40 °C to +85 °C unless otherwise specified; ADC frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	V_{DDA}	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[1][2]	-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[3]	-	-	±2	LSB
E_O	offset error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[4]	-	-	±3	LSB
E_G	gain error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[5]	-	-	±0.5	%
E_T	absolute error	V_{SSA} = 0 V, V_{DDA} = 3.3 V	[6]	-	-	±4	LSB
R_{vsi}	voltage source interface resistance		[7]	-	-	40	kΩ

[1] The ADC is monotonic, there are no missing codes.

[2] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 8.

[3] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 8.

[4] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 8.

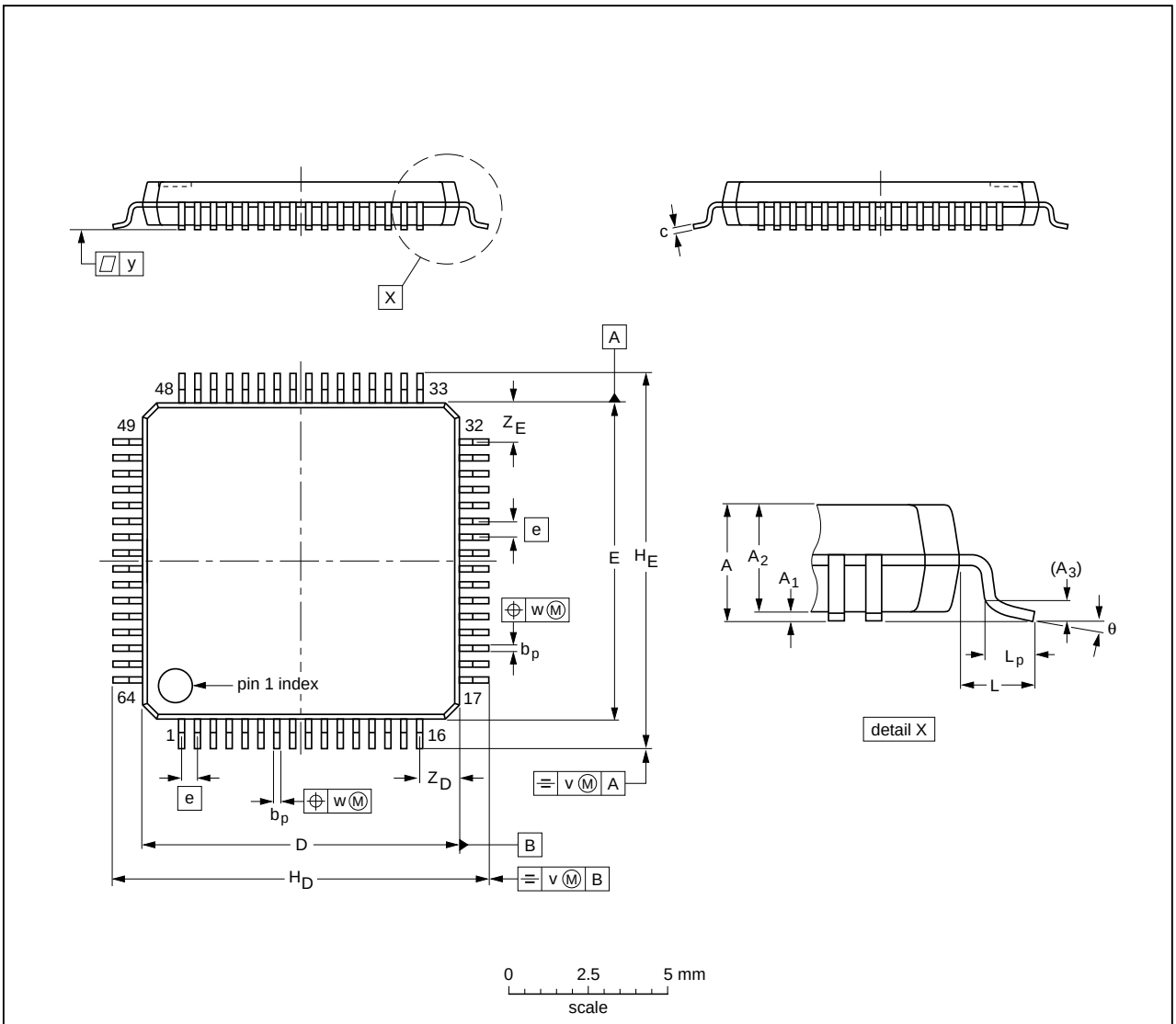
[5] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 8.

[6] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 8.

[7] See Figure 9.

13. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 15. Package outline SOT314-2 (LQFP64)

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2141_42_44_46_48 v.5	20110812	Product data sheet	-	LPC2141_42_44_46_48 v.4
Modifications:	• Table 3 “Pin description”: Added Table note [10] to RTCX1 and RTCX2 pins. • Table 4 “Limiting values”: Added parameter I_{sink}. • Table 5 “Static characteristics”, I^2C-bus pins: Changed typical hysteresis voltage from $0.5V_{DD}$ to $0.05V_{DD}$. • Table 5 “Static characteristics”: Updated min, typical and max values for oscillator pins $V_{i(XTAL1)}$, $V_{o(XTAL2)}$, $V_{i(RTCX1)}$, and $V_{o(RTCX2)}$. • Table 5 “Static characteristics”: Updated Table note [15]. • Added Section 11 “DAC electrical characteristics”. • Added Section 12.2 “Crystal oscillator XTAL input and component selection”. • Added Section 12.3 “RTC 32 kHz oscillator component selection”. • Added Section 12.4 “XTAL and RTCX Printed Circuit Board (PCB) layout guidelines”. • Updated Figure 8 “ADC characteristics”.			
LPC2141_42_44_46_48 v.4	20081117	Product data sheet	-	LPC2141_42_44_46_48 v.3
Modifications:	• Replaced all occurrences of VPB with APB. • Table 3: clarified which pins do/don’t have internal pull-ups. • Table 4: changed storage temperature range from −40 °C/125 °C to −65 °C/150 °C. • Table 5: added Table note 7 to input voltage spec. • Table 5: modified Table note 9. • Table 5: moved hysteresis voltage (0.4 V) from typ to min column. • Figure 8: updated figure and figure title, removed note			
LPC2141_42_44_46_48 v.3	20071019	Product data sheet	-	LPC2141_42_44_46_48 v.2
LPC2141_42_44_46_48 v.2	20060828	Product data sheet	-	LPC2141_42_44_46_48 v.1
LPC2141_42_44_46_48 v.1	20051003	Preliminary data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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