Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z0h
Core Size	32-Bit
Speed	32MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b SAR
Oscillator Type	External, Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1clh3

Table 1. MPC5602D device comparison (continued)

Feature	Device			
	MPC5601DxLH	MPC5601DxLL	MPC5602DxLH	MPC5602DxLL
Debug	JTAG			
Package	64 LQFP	100 LQFP	64 LQFP	100 LQFP

1 Refer to eMIOS chapter of device reference manual for information on the channel configuration and functions.
2 Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC
3 Type Y = OPWMT + OPWMB + SAIC + SAOC
4 Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC
5 Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC
6 I/O count based on multiplexing with peripherals

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602D device series.

Table 2. MPC5602D series block summary

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 12-bit analog-to-digital converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called "power domains" which are controlled by the PCU

Table 3. Voltage supply pin descriptions

Port pin	Function	Pin number	
		64 LQFP	100 LQFP
VDD_HV	Digital supply voltage	7, 28, 34, 56	15, 37, 52, 70, 84
VSS_HV	Digital ground	6, 8, 26, 33, 55	14, 16, 35, 51, 69, 83
VDD_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{SS_LV} pin.[1]	11, 23, 57	19, 32, 85
VSS_LV	1.2V decoupling pins. Decoupling capacitor must be connected between these pins and the nearest V_{DD_LV} pin.[1]	10, 24, 58	18, 33, 86
VDD_BV	Internal regulator supply voltage	12	20

[1] A decoupling capacitor must be placed between each of the three VDD_LV/VSS_LV supply pairs to ensure stable voltage (see the recommended operating conditions in the device datasheet for details).

3.4 Pad types

In the device the following types of pads are available for system pins and functional port pins:

S = Slow[1]
M = Medium[1 2]
F = Fast[1 2]
I = Input only with analog feature[1]
J = Input/Output ('S' pad) with analog feature
X = Oscillator

3.5 System pins

The system pins are listed in Table 4.

Table 4. System pin descriptions

Port pin	Function	I/O direction	Pad type	RESET configuration	Pin number	
					64 LQFP	100 LQFP
$\overline{\text{RESET}}$	Bidirectional reset with Schmitt-Trigger characteristics and noise filter.	I/O	M	Input, weak pull-up only after PHASE2	9	17
EXTAL	Analog output of the oscillator amplifier circuit, when the oscillator is not in bypass mode. Analog input for the clock generator when the oscillator is in bypass mode.[1]	I/O	X	Tristate	27	36
XTAL	Analog input of the oscillator amplifier circuit. Needs to be grounded if oscillator is used in bypass mode.[1]	I	X	Tristate	25	34

[1] Refer to the relevant section of the device datasheet.

1. See the I/O pad electrical characteristics in the device datasheet for details.
2. All medium and fast pads are in slow configuration by default at reset and can be configured as fast or medium (see the PCR[SRC] description in the device reference manual).

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ADC1_X[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	67
Port C									
PC[0][6]	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	87
PC[1][6]	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO —	SIUL — JTAGC —	I/O — O —	F	Tristate	54	82
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 — — EIRQ[5]	SIUL DSPI_1 — — SIUL	I/O I/O — — I	M	Tristate	50	78
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 —	GPIO[35] CS0_1 MA[0] — EIRQ[6]	SIUL DSPI_1 ADC — SIUL	I/O I/O O — I	S	Tristate	49	77
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 EIRQ[18]	SIUL — — — DSPI_1 SIUL	I/O — — — I I	M	Tristate	62	92
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 — — EIRQ[7]	SIUL DSPI_1 — — SIUL	I/O O — — I	M	Tristate	61	91
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	25

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlex_2 eMIOS_0 —	I/O O I/O —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13][3]	SIUL — eMIOS_0 — LINFlex_2 WKPU	I/O — I/O — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKPU[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 —	GPIO[73] — E0UC[23] — WKPU[7][3]	SIUL — eMIOS_0 — WKPU	I/O — I/O — I	S	Tristate	—	10
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] — CS3_1 — EIRQ[10]	SIUL — DSPI_1 — SIUL	I/O — O — I	S	Tristate	—	11
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 —	GPIO[75] E0UC[24] CS4_1 — WKPU[14][3]	SIUL eMIOS_0 DSPI_1 — WKPU	I/O I/O O — I	S	Tristate	—	13
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — — — ADC1_S[7] EIRQ[11]	SIUL — — — ADC SIUL	I/O — — — I I	S	Tristate	—	76
Port H									
PH[9][6]	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	60	88
PH[10][6]	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	53	81

1 Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 → AF0; PCR.PA = 01 → AF1; PCR.PA = 10 → AF2; PCR.PA = 11 → AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

2 Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

3 All WKPU pins also support external interrupt capability. See "wakeup unit" chapter of the device reference manual for further details.

4 NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

5 "Not applicable" because these functions are available only while the device is booting. Refer to "BAM" chapter of the device reference manual for details.

4.7.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 19. I/O supply segment

Package	Supply segment			
	1	2	3	4
100 LQFP	pin 16 – pin 35	pin 37 – pin 69	pin 70 – pin 83	pin 84 – pin 15
64 LQFP	pin 8 – pin 26	pin 28 – pin 55	pin 56 – pin 7	—

Table 21. I/O weight[1] (continued)

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%
PE[3]	7%	10%	9%	9%
PC[5]	8%	11%	9%	10%
PC[4]	8%	11%	9%	10%
PE[4]	8%	12%	10%	10%
PE[5]	8%	12%	10%	11%
PE[6]	9%	12%	10%	11%
PE[7]	9%	12%	10%	11%
PC[12]	9%	13%	11%	11%
PC[13]	9%	9%	11%	11%
PC[8]	9%	9%	11%	11%
PB[2]	9%	13%	11%	12%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2 SRC: “Slew Rate Control” bit in SIU_PCR

4.8 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

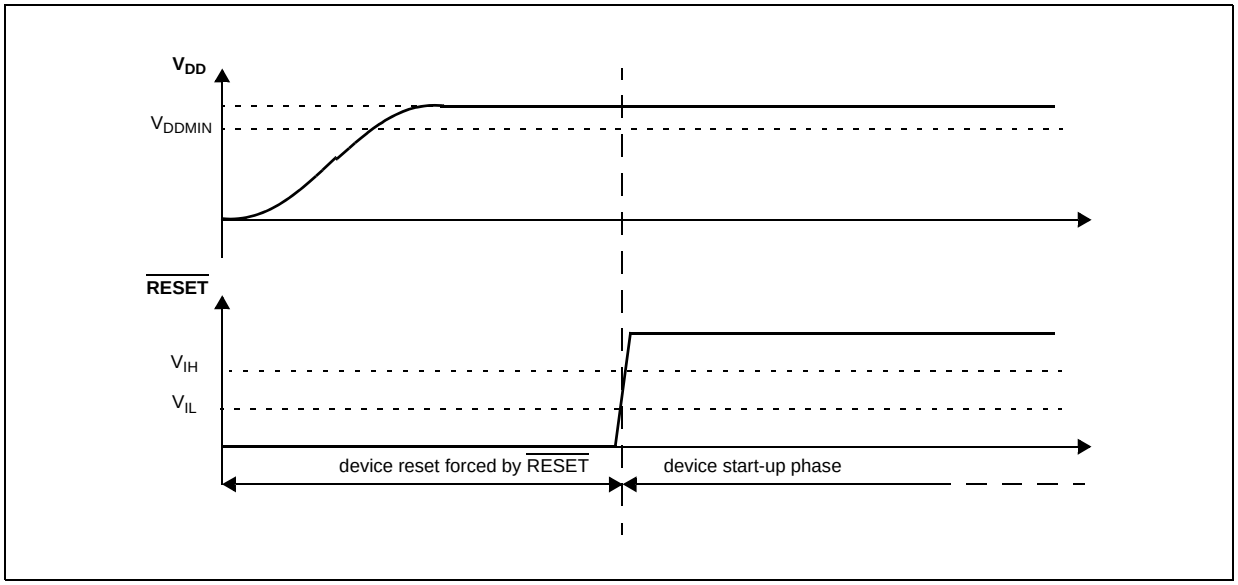

Figure 5. Start-up reset requirements

— LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
— LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
— LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

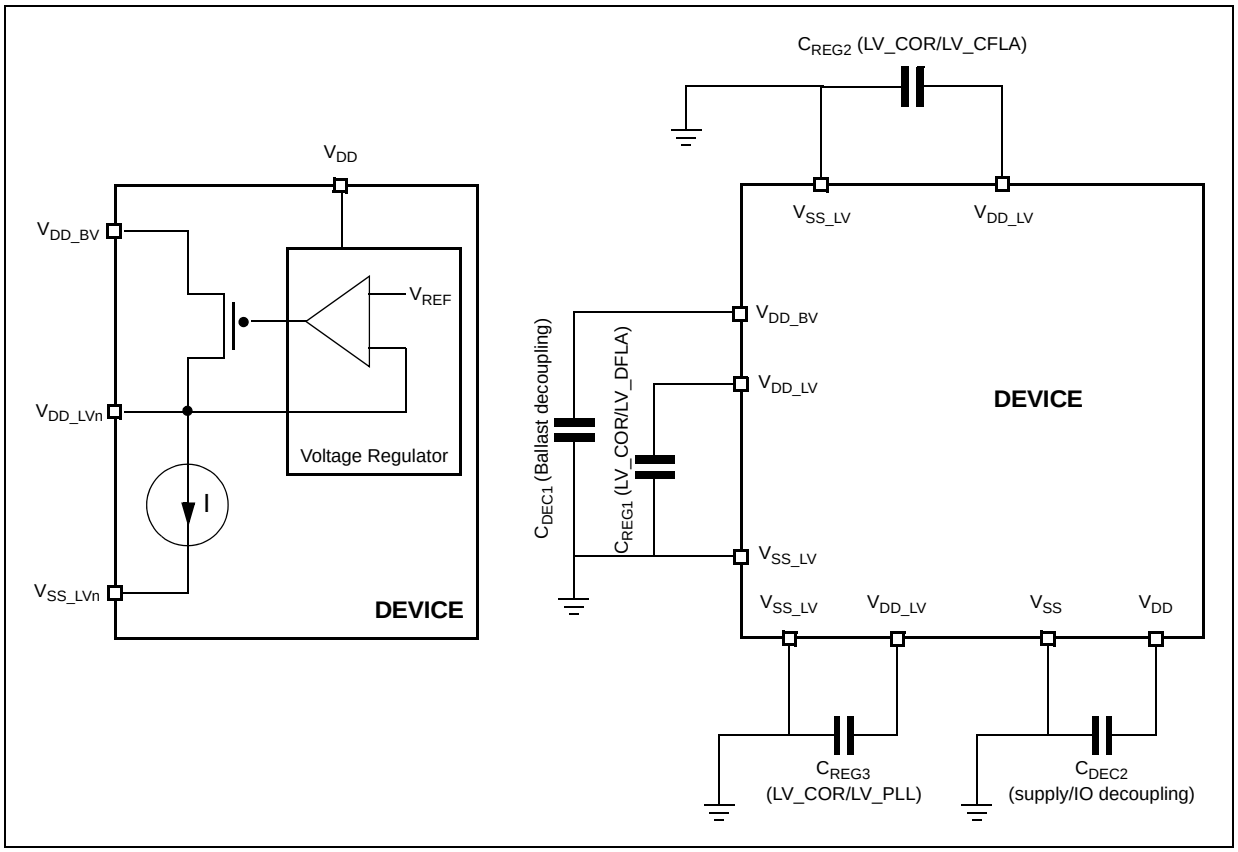

Figure 7. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 4.5, Recommended operating conditions).

Table 23. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V.

4 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

5 In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

Table 28. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	cycles
				128 KB blocks	1,000	100,000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

1 Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{CFREAD}	CC	P	Maximum working frequency for reading code flash memory at given number of wait states in worst conditions	2 wait states	48	MHz
		C		0 wait states	20	
f_{DFREAD}	CC	P	Maximum working frequency for reading data flash memory at given number of wait states in worst conditions	6 wait states	48	MHz

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 30 shows the power supply DC characteristics on external supply.

NOTE

Power supply for data flash is actually provided by code flash; this means that data flash cannot work if code flash is not powered.

Table 30. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{CFREAD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFREAD}	CC	D			Data flash	—	—	4	mA
I_{CFMOD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/Erase on-going while reading flash registers, f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFMOD}	CC	D			Data flash	—	—	6	mA

4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 9 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 35 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

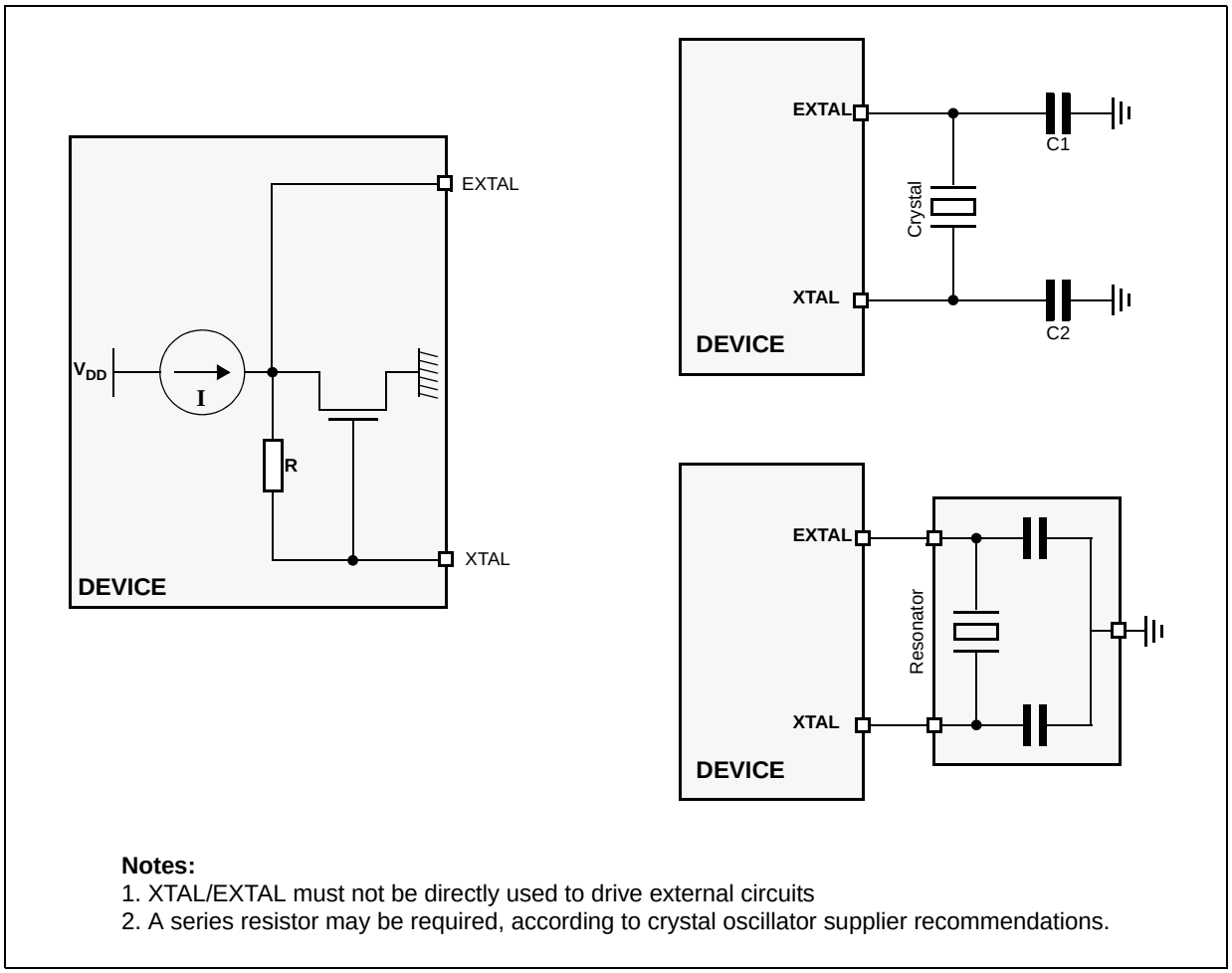

Figure 9. Crystal oscillator and resonator connection scheme

4.17 ADC electrical characteristics

4.17.1 Introduction

The device provides a 12-bit Successive Approximation Register (SAR) analog-to-digital converter.

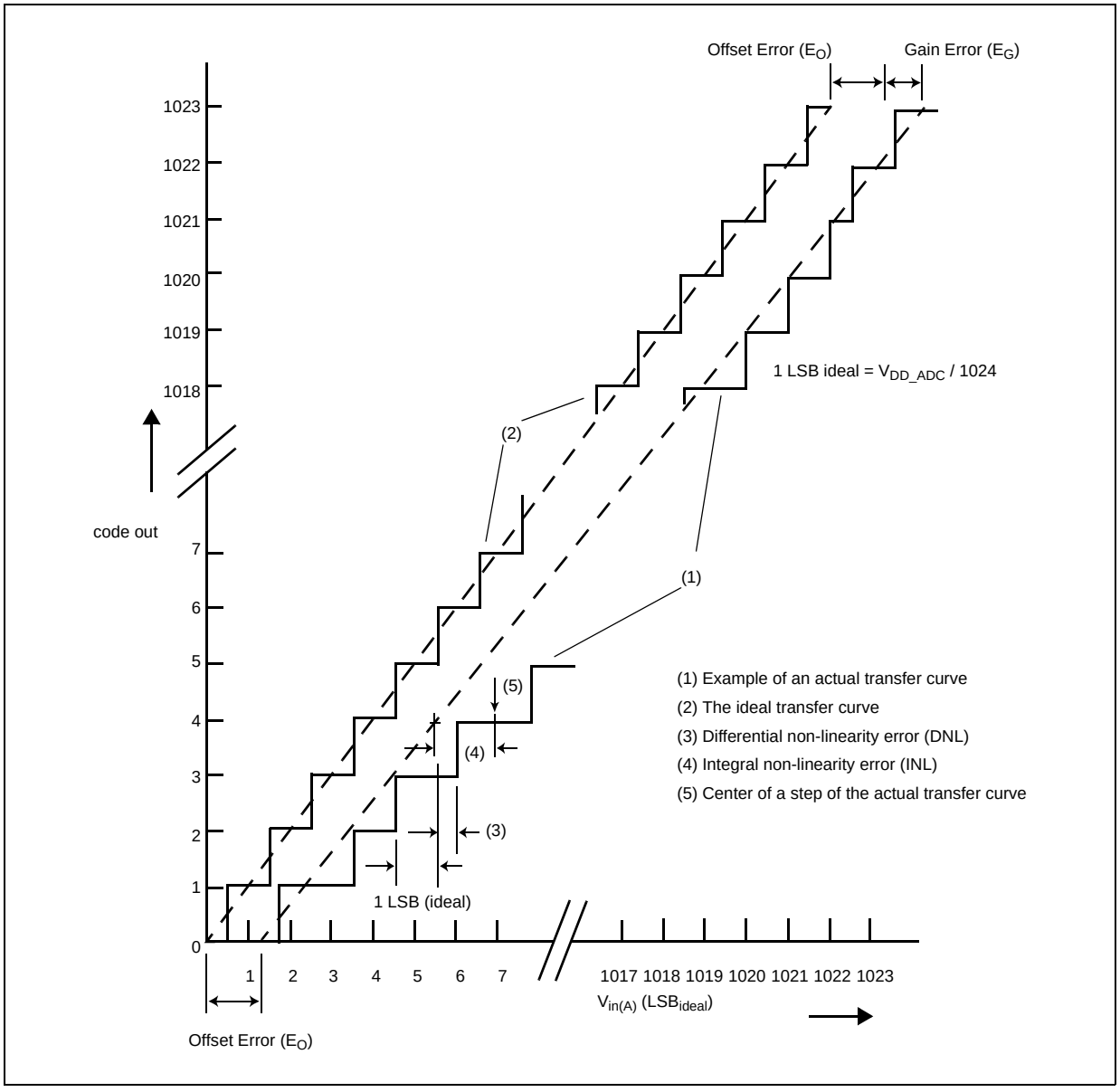

Figure 11. ADC characteristics and error definitions

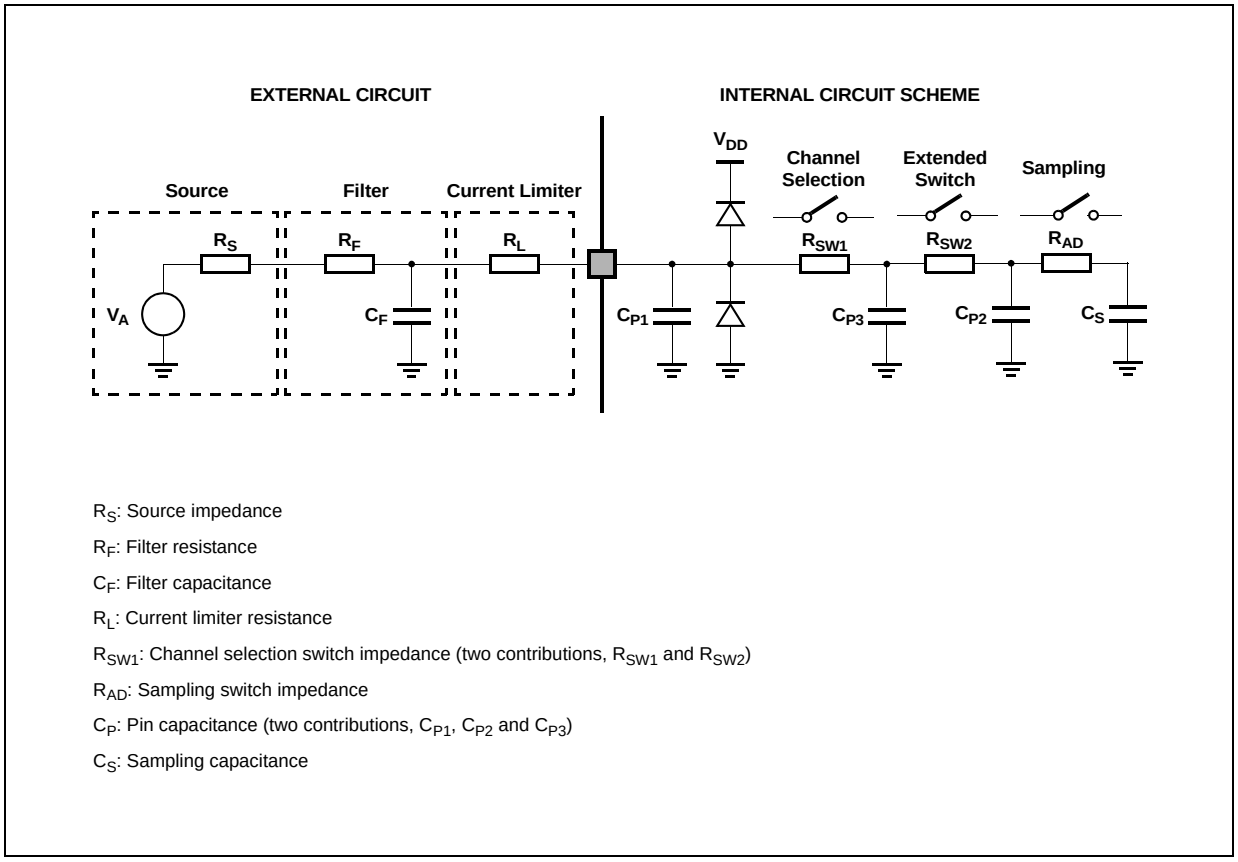

Figure 13. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

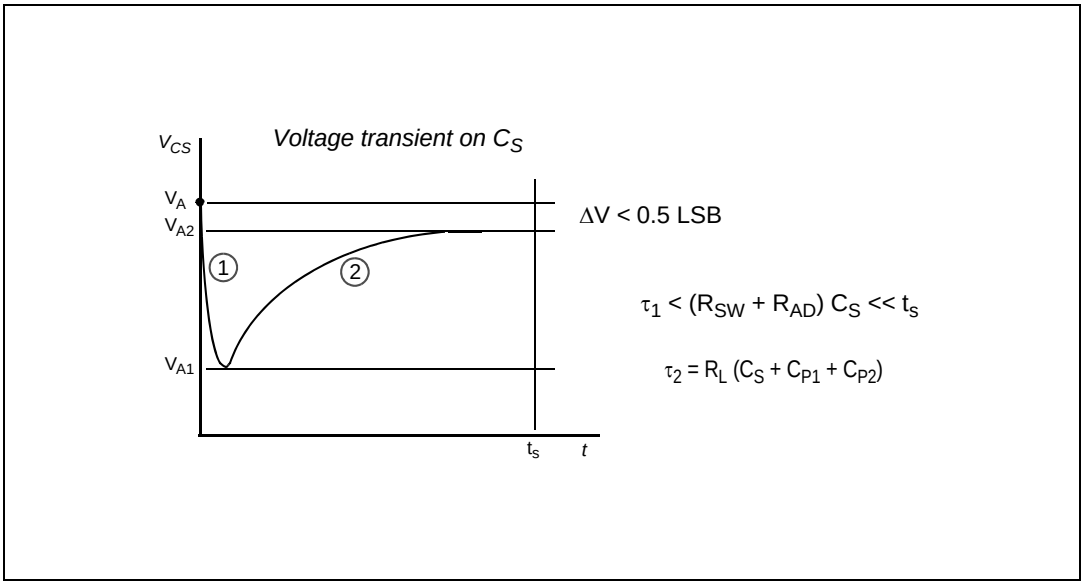

Figure 14. Transient behavior during sampling phase

Table 43. DSPI characteristics[1] (continued)

No.	Symbol		C	Parameter		DSPI0/DSPI1			Unit
						Min	Typ	Max	
—	Δt_{CSC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode	Master mode	—	—	130[2]	ns
—	Δt_{ASC}	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1→1	Master mode	—	—	130(2)	ns
2	t_{CSCext}[3]	SR	D	CS to SCK delay	Slave mode	32	—	—	ns
3	t_{ASCext}[4]	SR	D	After SCK delay	Slave mode	$1/f_{DSPI}$ + 5	—	—	ns
4	t_{SDC}	CC	D	SCK duty cycle	Master mode	—	$t_{SCK}/2$	—	ns
		SR	D		Slave mode	$t_{SCK}/2$	—	—	
5	t_A	SR	D	Slave access time	—	$1/f_{DSPI}$ + 70	—	—	ns
6	t_{DI}	SR	D	Slave SOUT disable time	—	7	—	—	ns
7	t_{PCSC}	SR	D	PCS*x* to $\overline{\text{PCSS}}$ time	—	0	—	—	ns
8	t_{PASC}	SR	D	$\overline{\text{PCSS}}$ to PCS*x* time	—	0	—	—	ns
9	t_{SUI}	SR	D	Data setup time for inputs	Master mode	43	—	—	ns
					Slave mode	5	—	—	
10	t_{HI}	SR	D	Data hold time for inputs	Master mode	0	—	—	ns
					Slave mode	2[5]	—	—	
11	t_{SUO}[6]	CC	D	Data valid after SCK edge	Master mode	—	—	32	ns
					Slave mode	—	—	52	
12	t_{HO}(6)	CC	D	Data hold time for outputs	Master mode	0	—	—	ns
					Slave mode	8	—	—	

1 Operating conditions: C_{OUT} = 10 to 50 pF, $Slew_{IN}$ = 3.5 to 15 ns

2 Maximum is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM pad

3 The t_{CSC} delay value is configurable through a register. When configuring t_{CSC} (using PCSSCK and CSSCK fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{CSC} to ensure positive t_{CSCext}.

4 The t_{ASC} delay value is configurable through a register. When configuring t_{ASC} (using PASC and ASC fields in DSPI_CTARx registers), delay between internal CS and internal SCK must be higher than Δt_{ASC} to ensure positive t_{ASCext}.

5 This delay value corresponds to SMPL_PT = 00b which is bit field 9 and 8 of DSPI_MCR.

6 SCK and SOUT configured as MEDIUM pad

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3

Figure 28. 100 LQFP package mechanical drawing (Part 3 of 3)

5.1.2 64 LQFP

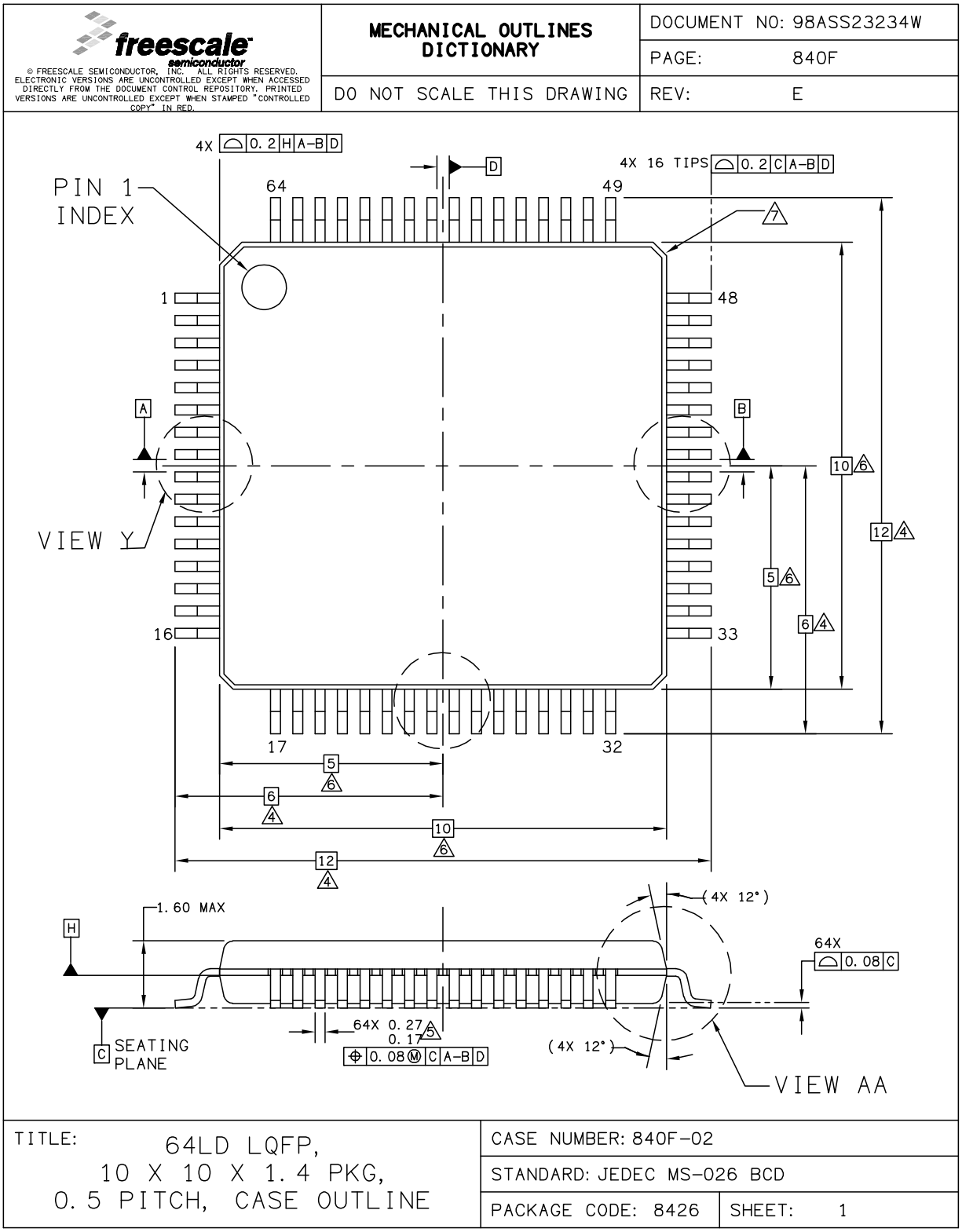

Figure 29. 64 LQFP mechanical drawing (part 1 of 3)

Table 45. Revision history (continued)

Revision	Date	Description of Changes
4	14 Jul 2011	Formatting and editorial changes throughout Device comparison table: for the “Total timer I/O eMIOS”, changed “13 ch” to “14 ch” Features: Replaced “e200z0“ with “e200z0h”; added an explanation of which LINFlex modules support master mode and slave MPC5601D/MPC5602D series block summary: • added definition for “AUTOSAR” acronym changed “System watchdog timer” to “Software watchdog timer”64 LQFP pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV Added section “Pad configuration during reset phases” Added section “Voltage supply pins” Added section “Pad types” Added section “System pins” Renamed and updated section “Functional ports” (was previously section “Pin muxing”); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit) Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality Added section “NVUSRO[WATCHDOG_EN] field description” Absolute maximum ratings: Removed “C” column from table Replaced “TBD” with “—” in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4 I/O input DC electrical characteristics: removed footnote “All values need to be confirmed during device validation”; updated I_{LKG} characteristics MEDIUM configuration output buffer electrical characteristics: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O consumption: replaced instances of “Root medium square” with “Root mean square” Updated section “Voltage regulator electrical characteristics” Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section “Power consumption” (was previously section “Low voltage domain power consumption”) Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 13 ADC conversion characteristics: • updated conditions for sampling time V_{DD} = 5.0 V • updated conditions for conversion time V_{DD} = 5.0 V Commercial product code structure: added character for frequency; updated optional fields character and description Restored the revision history table and added an entry for Rev. 3.1 Updated Abbreviations

Table 45. Revision history (continued)

Revision	Date	Description of Changes
5	—	Rev. 5 not published.
6	29 Jan 2013	Removed all instances of table footnote “All values need to be confirmed during device validation” Section 4.1, “Introduction, removed Caution note. In Table 42, On-chip peripherals current consumption, replaced “TBD” with “8.21 mA” in $I_{DD\_HV(FLASH)}$ cell. Updated Section 4.17.2, “Input impedance and ADC accuracy In Table 24, changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ from 2.7 V to 2.6 V. Revised the Table 28 (Flash module life) Updated Table 43, DSPI characteristics, to add specifications 7 and 8, t_{PCSC} and t_{PASC}. Inserted Figure 24, DSPI PCS strobe (PCSS) timing.

Appendix A Abbreviations

Table A-1 lists abbreviations used in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
APU	Auxilliary processing unit
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DAOC	Double action output compare
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input/output
IPM	Input period measurement
IPWM	Input pulse width measurement
MB	Message buffer
MC	Modulus counter
MCB	Modulus counter buffered (up / down)
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NVUSRO	Non-volatile user options register
OPWFMB	Output pulse width and frequency modulation buffered
OPWMB	Output pulse width modulation buffered

Table A-1. Abbreviations (continued)

Abbreviation	Meaning
OPWMCB	Center aligned output pulse width modulation buffered with dead time
OPWMT	Output pulse width modulation trigger
PWM	Pulse width modulation
SAIC	Single action input capture
SAOC	Single action output compare
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select