Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1mll4r

Table 1. MPC5602D device comparison (continued)

Feature	Device			
	MPC5601DxLH	MPC5601DxLL	MPC5602DxLH	MPC5602DxLL
Debug	JTAG			
Package	64 LQFP	100 LQFP	64 LQFP	100 LQFP

1 Refer to eMIOS chapter of device reference manual for information on the channel configuration and functions.
2 Type X = MC + MCB + OPWMT + OPWMB + OPWFMB + SAIC + SAOC
3 Type Y = OPWMT + OPWMB + SAIC + SAOC
4 Type G = MCB + IPWM + IPM + DAOC + OPWMT + OPWMB + OPWFMB + OPWMCB + SAIC + SAOC
5 Type H = IPWM + IPM + DAOC + OPWMT + OPWMB + SAIC + SAOC
6 I/O count based on multiplexing with peripherals

2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5602D device series.

Table 2. MPC5602D series block summary (continued)

Block	Function
Real-time counter (RTC)	Provides a free-running counter and interrupt generation capability that can be used for timekeeping applications
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	Supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

3 Package pinouts and signal descriptions

3.1 Package pinouts

The available LQFP pinouts are provided in the following figures. For pin signal descriptions, please refer to Table 5.

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlex_2 eMIOS_0 —	I/O O I/O —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13][3]	SIUL — eMIOS_0 — LINFlex_2 WKPU	I/O — I/O — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKPU[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — ADC1_P[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	49
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — ADC1_P[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	56
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — ADC1_P[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	57
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — ADC1_P[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	58
PD[12]	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ADC1_S[8]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	60
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ADC1_S[9]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	62
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ADC1_S[10]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	64
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ADC1_S[11]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	66
Port E									

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 —	GPIO[64] E0UC[16] — — WKPU[6][3]	SIUL eMIOS_0 — — WKPU	I/O I/O — — I	S	Tristate	—	6
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	8
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 — —	GPIO[66] E0UC[18] — — EIRQ[21] SIN_1	SIUL eMIOS_0 — — SIUL DSPI_1	I/O I/O — — I I	M	Tristate	—	89
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS_0 DSPI_1 —	I/O I/O O —	M	Tristate	—	90
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS_0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	93
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	94
PE[6]	PCR[70]	AF0 AF1 AF2 AF3 —	GPIO[70] E0UC[22] CS3_0 MA[1] EIRQ[22]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	95
PE[7]	PCR[71]	AF0 AF1 AF2 AF3 —	GPIO[71] E0UC[23] CS2_0 MA[0] EIRQ[23]	SIUL eMIOS_0 DSPI_0 ADC SIUL	I/O I/O O O I	M	Tristate	—	96
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] — E0UC[22] —	SIUL — eMIOS_0 —	I/O — I/O —	M	Tristate	—	9

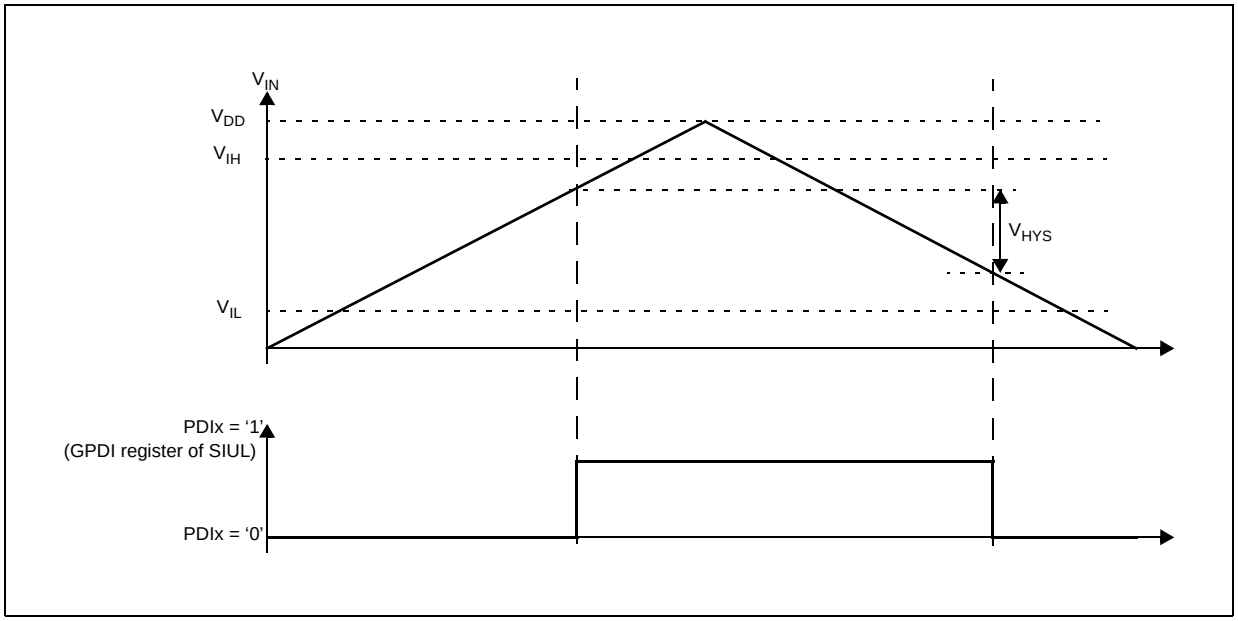


Figure 4. Input DC electrical characteristics definition

Table 14. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	V
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Digital input filtered pulse	—		—	—	40	ns
W_{NFI}[(2)]	SR	P	Digital input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 15 provides weak pull figures. Both pull-up and pull-down resistances are supported.

Table 20. I/O consumption

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{SWTSLW}[2]	CC	D	Dynamic I/O current for SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	20	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	16	
I_{SWTMED}(2)	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	29	mA
					V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	17	
I_{RMSSLW}	CC	D	Root mean square I/O current for SLOW configuration	C_L = 25 pF, 2 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C_L = 25 pF, 4 MHz		—	—	3.2	
				C_L = 100 pF, 2 MHz		—	—	6.6	
				C_L = 25 pF, 2 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C_L = 25 pF, 4 MHz		—	—	2.3	
				C_L = 100 pF, 2 MHz		—	—	4.7	
I_{RMSMED}	CC	D	Root mean square I/O current for MEDIUM configuration	C_L = 25 pF, 13 MHz	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C_L = 25 pF, 40 MHz		—	—	13.4	
				C_L = 100 pF, 13 MHz		—	—	18.3	
				C_L = 25 pF, 13 MHz	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C_L = 25 pF, 40 MHz		—	—	8.5	
				C_L = 100 pF, 13 MHz		—	—	11	
I_{AVGSEG}	SR	D	Sum of all the static I/O current within a supply segment	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V_{DD} = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 21 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below 100%.

Table 21. I/O weight[1] (continued)

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PC[0]	6%	9%	7%	8%
PE[2]	7%	10%	8%	9%
PE[3]	7%	10%	9%	9%
PC[5]	8%	11%	9%	10%
PC[4]	8%	11%	9%	10%
PE[4]	8%	12%	10%	10%
PE[5]	8%	12%	10%	11%
PE[6]	9%	12%	10%	11%
PE[7]	9%	12%	10%	11%
PC[12]	9%	13%	11%	11%
PC[13]	9%	9%	11%	11%
PC[8]	9%	9%	11%	11%
PB[2]	9%	13%	11%	12%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified
2 SRC: “Slew Rate Control” bit in SIU_PCR

4.8 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional $\overline{\text{RESET}}$ pin.

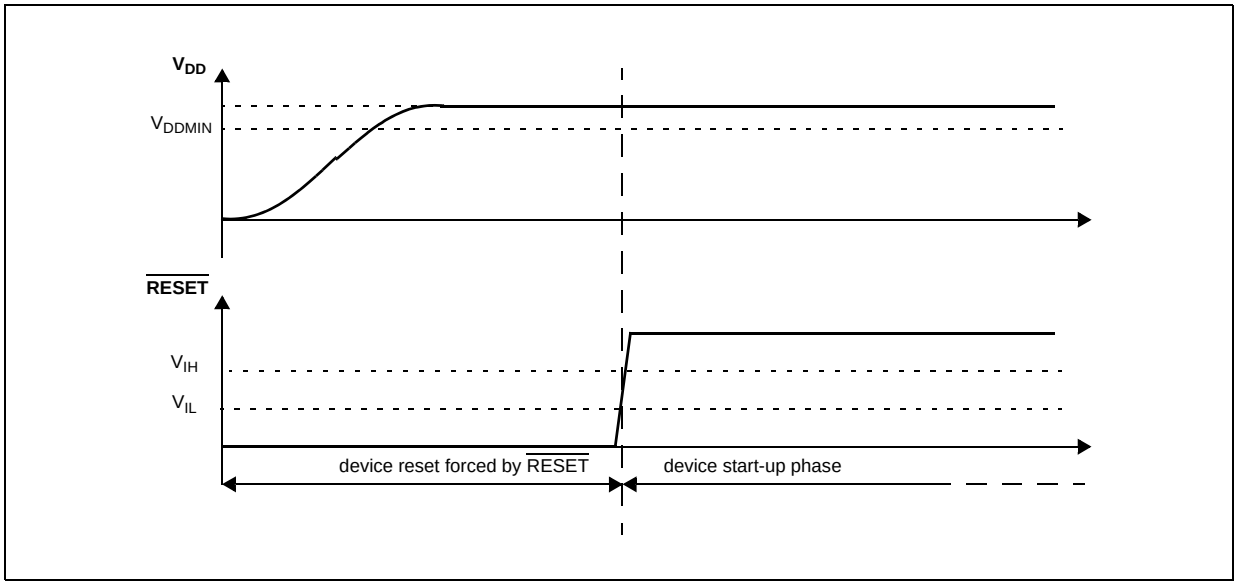


Figure 5. Start-up reset requirements

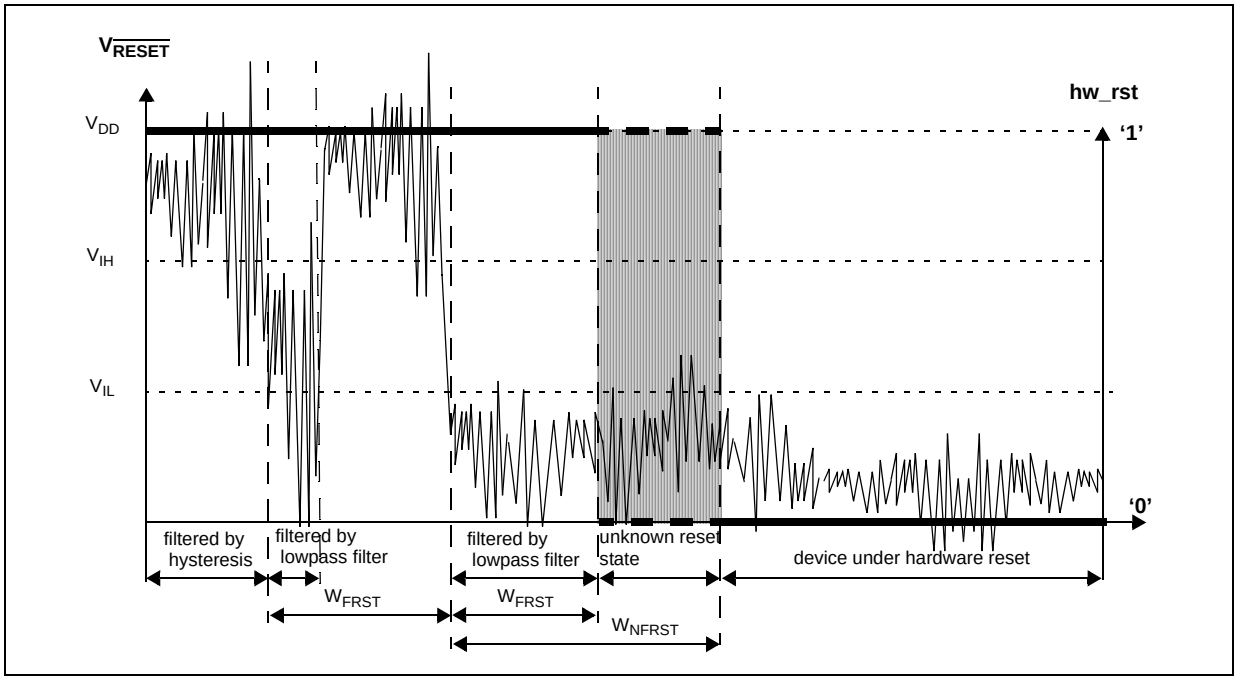


Figure 6. Noise filtering on reset signal

Table 22. Reset electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{IH}	SR	P	Input High Level CMOS (Schmitt Trigger)	—	$0.65V_{DD}$	—	V_{DD} + 0.4	V
V_{IL}	SR	P	Input low Level CMOS (Schmitt Trigger)	—	–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	$0.1V_{DD}$	—	—	V
V_{OL}	CC	P	Output low level	Push Pull, I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	$0.1V_{DD}$	V
				Push Pull, I_{OL} = 1 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	—	—	$0.1V_{DD}$	
				Push Pull, I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

Table 26. Program and erase specifications (code flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	300	500	5000	ms
$t_{32Kpperase}$	CC	C	32 KB block preprogram and erase time	—	400	600	5000	ms
$t_{128Kpperase}$	CC	C	128 KB block preprogram and erase time	—	800	1300	7500	ms
t_{esus}	CC	C	Erase suspend latency	—	—	30	30	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 27. Program and erase specifications (data flash)

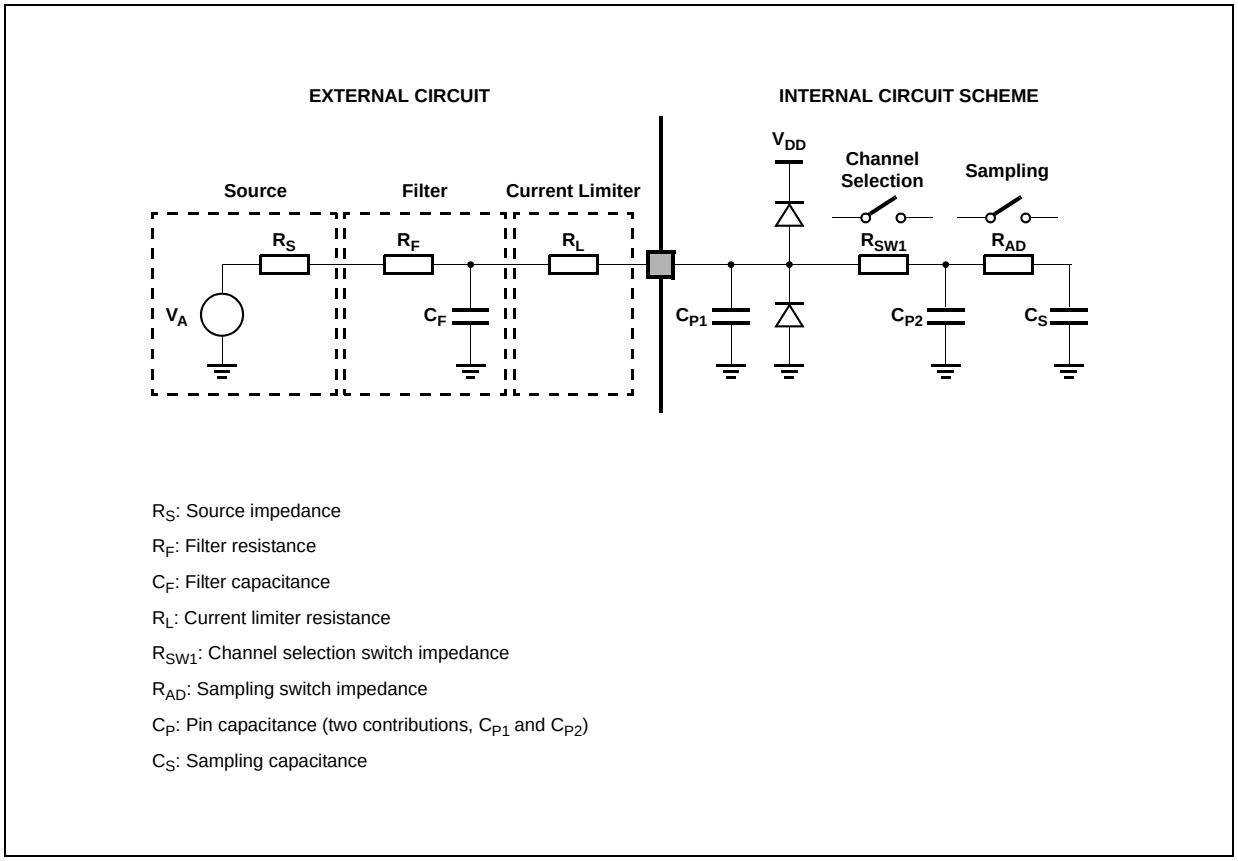
Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$t_{swprogram}$	CC	C	Single word (32 bits) program time[4]	—	30	70	300	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	700	800	1500	ms
t_{Bank_D}	CC	C	64 KB block preprogram and erase time	—	1900	2300	4800	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.



R_S: Source impedance

R_F: Filter resistance

C_F: Filter capacitance

R_L: Current limiter resistance

R_{SW1}: Channel selection switch impedance

R_{AD}: Sampling switch impedance

C_P: Pin capacitance (two contributions, C_{P1} and C_{P2})

C_S: Sampling capacitance

Figure 12. Input equivalent circuit (precise channels)

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

Table 41. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_c	CC	P	Conversion time[6] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPCMP = 0		2.4	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
		P	Conversion time[(6)] V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPCMP = 0		1.5	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
C_S	CC	D	ADC input sampling capacitance	—		5			pF
C_{P1}	CC	D	ADC input pin capacitance 1	—		3			pF
C_{P2}	CC	D	ADC input pin capacitance 2	—		1			pF
C_{P3}	CC	D	ADC input pin capacitance 3	—		1.5			pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
E_O	CC	T	Absolute Offset error	—		—	2	—	LSB
E_G	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	

Table 41. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10		10	LSB
		T		With current injection	–12		12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sampling time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

6 This parameter does not include the sampling time t_S, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 42. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 × f_{periph} + 85	µA
				125 Kbyte/s		8 × f_{periph} + 27	µA
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 × f_{periph}	µA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	µA
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 × f_{periph} + 31	µA

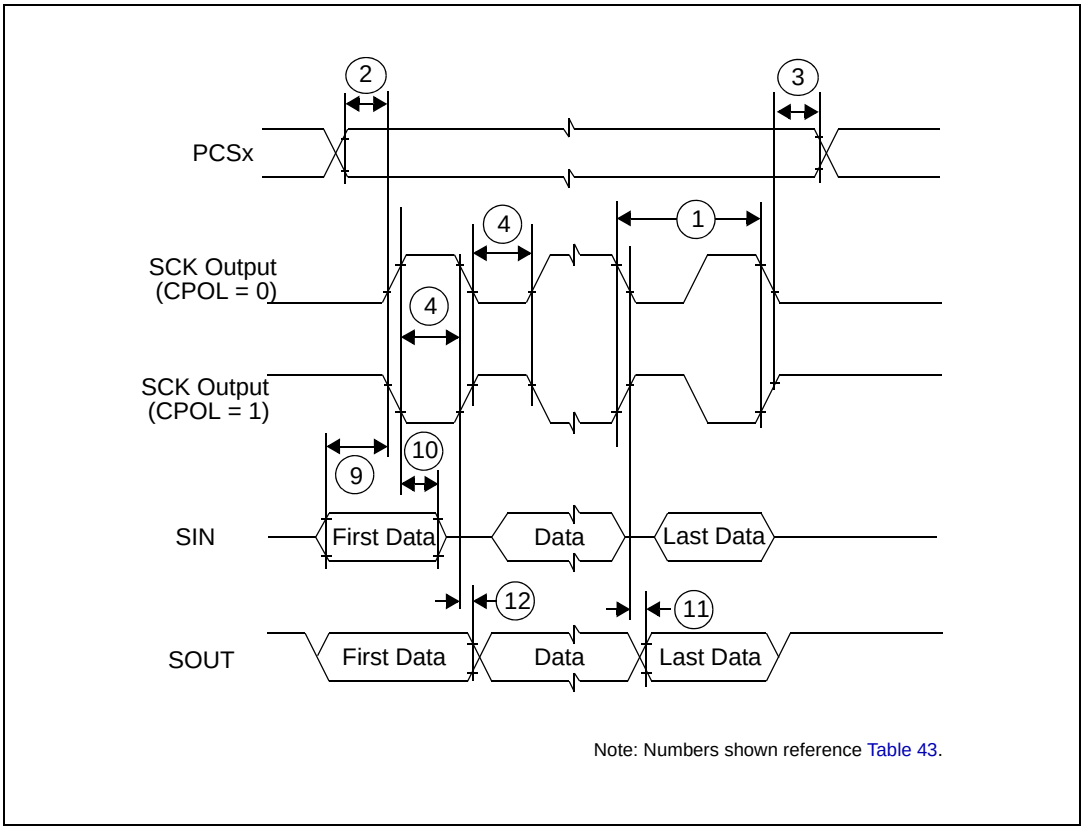


Figure 16. DSPI classic SPI timing – master, CPHA = 0

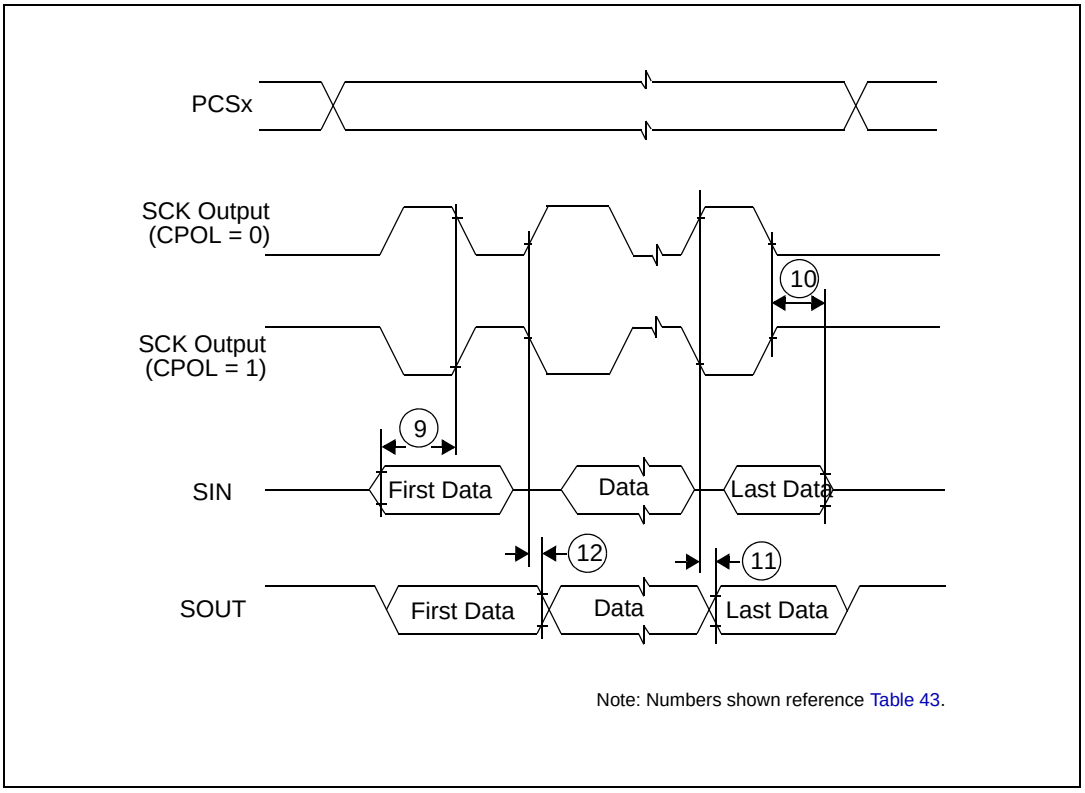


Figure 17. DSPI classic SPI timing – master, CPHA = 1

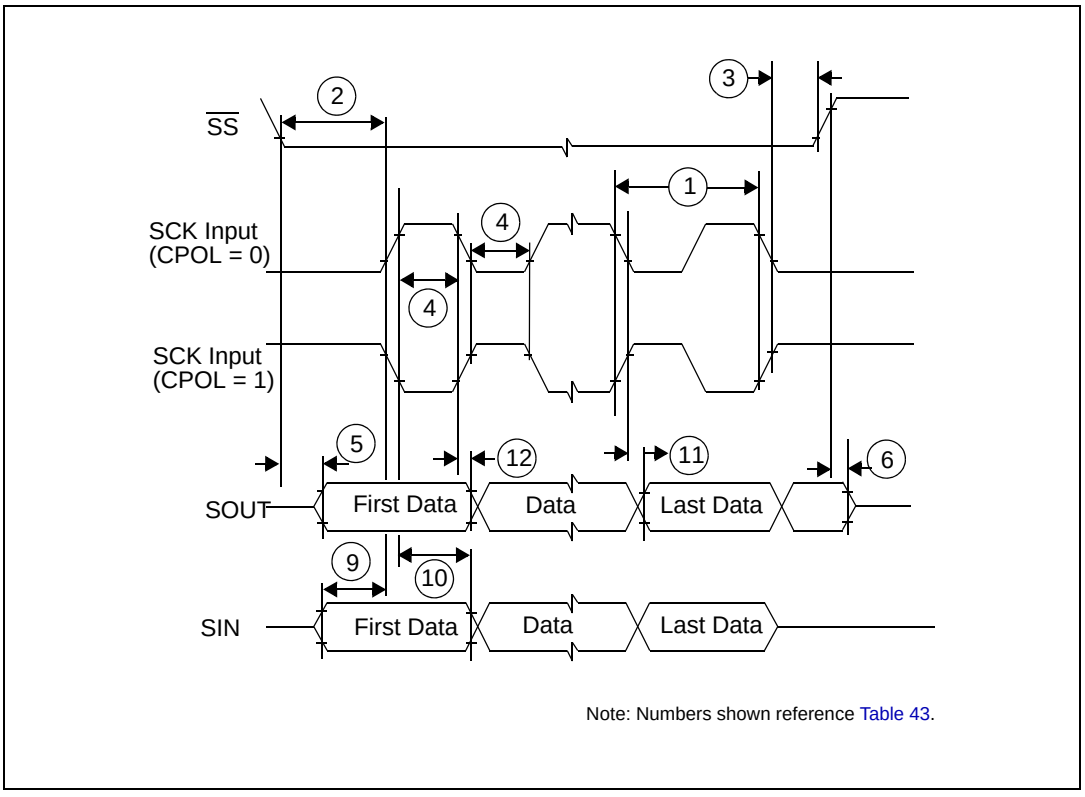


Figure 18. DSPI classic SPI timing – slave, CPHA = 0

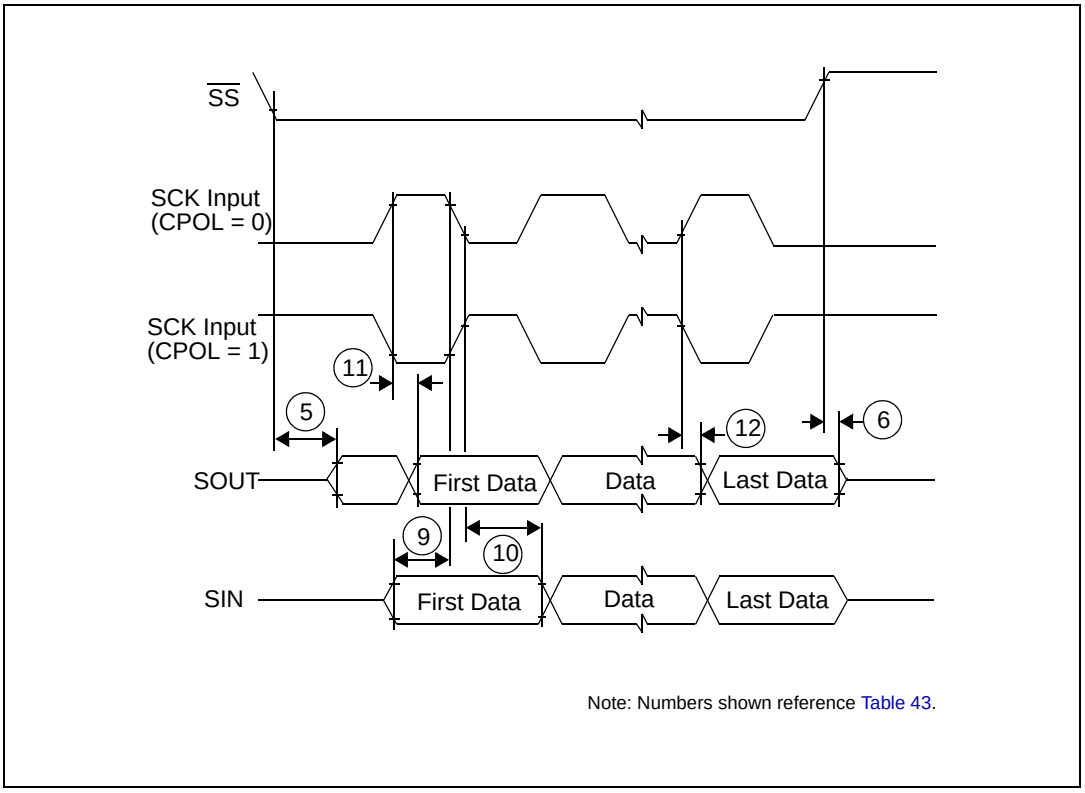


Figure 19. DSPI classic SPI timing – slave, CPHA = 1

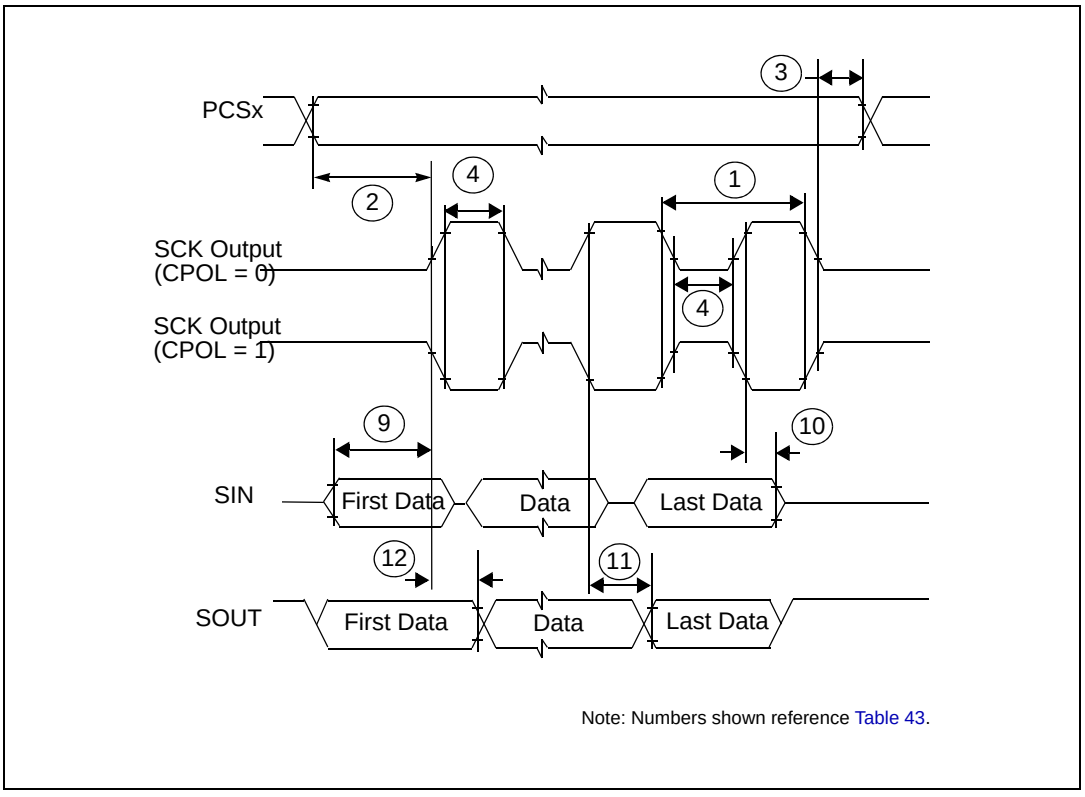


Figure 20. DSPI modified transfer format timing – master, CPHA = 0

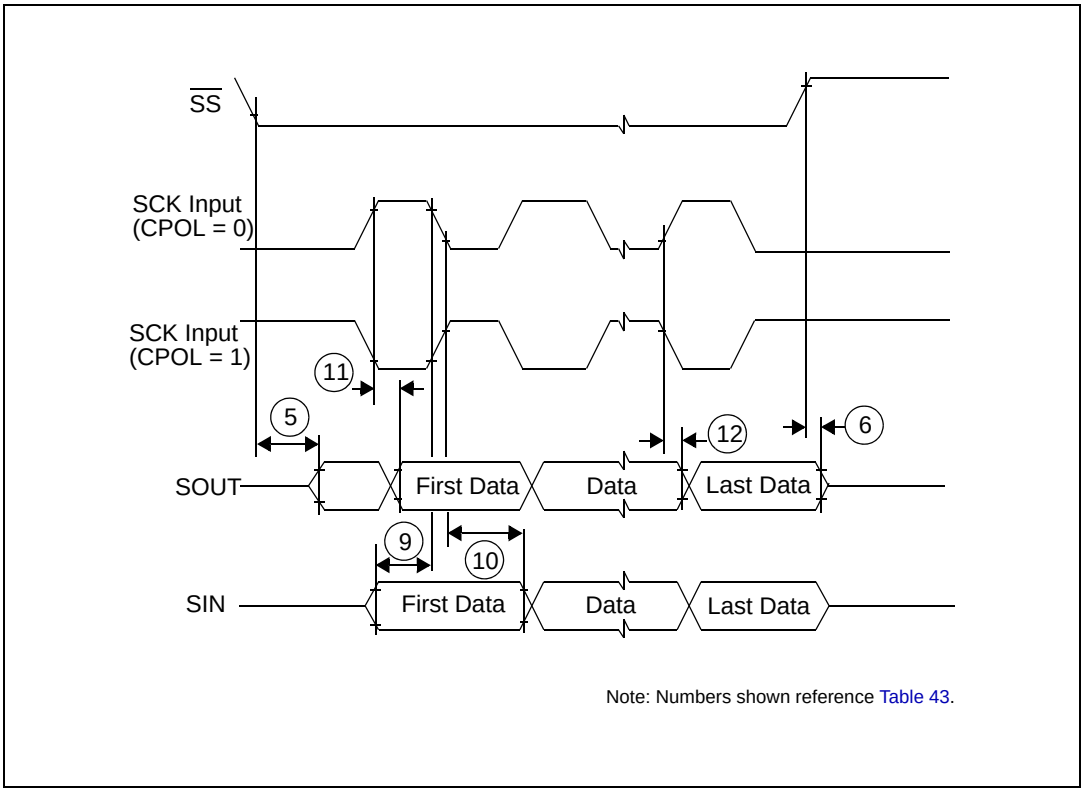


Figure 23. DSPI modified transfer format timing – slave, CPHA = 1

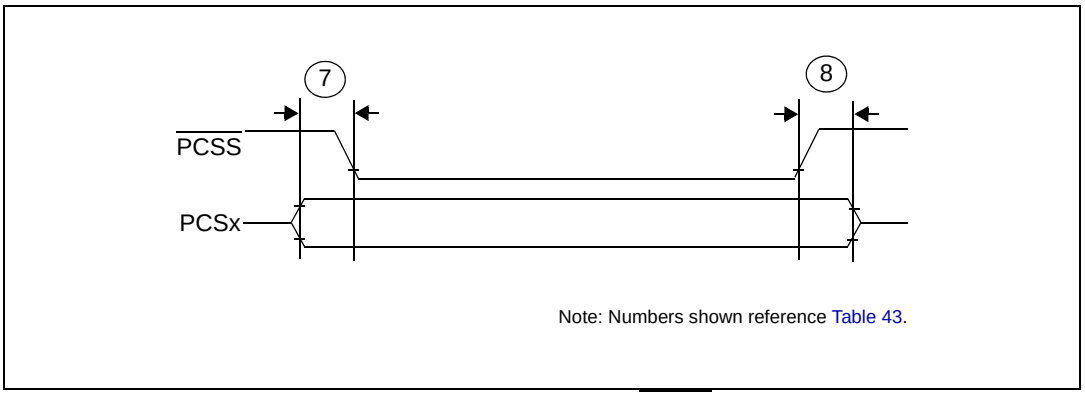


Figure 24. DSPI PCS strobe (PCSS) timing

Table 45. Revision history (continued)

Revision	Date	Description of Changes
3.1	23 Feb 2011	Deleted the “Freescale Confidential Proprietary” label (the document is public)

Table 45. Revision history (continued)

Revision	Date	Description of Changes
4	14 Jul 2011	Formatting and editorial changes throughout Device comparison table: for the “Total timer I/O eMIOS”, changed “13 ch” to “14 ch” Features: Replaced “e200z0“ with “e200z0h”; added an explanation of which LINFlex modules support master mode and slave MPC5601D/MPC5602D series block summary: • added definition for “AUTOSAR” acronym changed “System watchdog timer” to “Software watchdog timer”64 LQFP pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV Added section “Pad configuration during reset phases” Added section “Voltage supply pins” Added section “Pad types” Added section “System pins” Renamed and updated section “Functional ports” (was previously section “Pin muxing”); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit) Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality Added section “NVUSRO[WATCHDOG_EN] field description” Absolute maximum ratings: Removed “C” column from table Replaced “TBD” with “—” in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4 I/O input DC electrical characteristics: removed footnote “All values need to be confirmed during device validation”; updated I_{LKG} characteristics MEDIUM configuration output buffer electrical characteristics: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O consumption: replaced instances of “Root medium square” with “Root mean square” Updated section “Voltage regulator electrical characteristics” Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section “Power consumption” (was previously section “Low voltage domain power consumption”) Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 13 ADC conversion characteristics: • updated conditions for sampling time V_{DD} = 5.0 V • updated conditions for conversion time V_{DD} = 5.0 V Commercial product code structure: added character for frequency; updated optional fields character and description Restored the revision history table and added an entry for Rev. 3.1 Updated Abbreviations