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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	45
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1vlh4r

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 — —	GPIO[7] E0UC[7] — — EIRQ[2] ADC1_S[1]	SIUL eMIOS_0 — — SIUL ADC	I/O I/O — — I I	S	Tristate	44	71
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A[5]	GPIO[8] E0UC[8] E0UC[14] — EIRQ[3] ABS[0]	SIUL eMIOS_0 eMIOS_0 — SIUL BAM	I/O I/O — — I I	S	Input, weak pull-up	45	72
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A[5]	GPIO[9] E0UC[9] — CS2_1 FAB	SIUL eMIOS_0 — DSPI_1 BAM	I/O I/O — I/O I	S	Pull-down	46	73
PA[10]	PCR[10]	AF0 AF1 AF2 AF3 —	GPIO[10] E0UC[10] — LIN2TX ADC1_S[2]	SIUL eMIOS_0 — LINFlex_2 ADC	I/O I/O — O I	S	Tristate	47	74
PA[11]	PCR[11]	AF0 AF1 AF2 AF3 — — —	GPIO[11] E0UC[11] — — EIRQ[16] ADC1_S[3] LIN2RX	SIUL eMIOS_0 — — SIUL ADC LINFlex_2	I/O I/O — — I I I	S	Tristate	48	75
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 — —	GPIO[12] — — — EIRQ[17] SIN_0	SIUL — — — SIUL DSPI_0	I/O — — — I I	S	Tristate	22	31
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — CS3_1	SIUL DSPI_0 — DSPI_1	I/O O — I/O	M	Tristate	21	30
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 E0UC[0] EIRQ[4]	SIUL DSPI_0 DSPI_0 eMIOS_0 SIUL	I/O I/O I/O I/O I	M	Tristate	19	28

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 E0UC[1] WKPU[10][3]	SIUL DSPI_0 DSPI_0 eMIOS_0 WKPU	I/O I/O I/O I/O I	M	Tristate	18	27
Port B									
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — LIN2TX	SIUL FlexCAN_0 — LINFlex_2	I/O O — O	M	Tristate	14	23
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — LIN0RX WKPU[4][3] CAN0RX	SIUL — — LINFlex_0 WKPU FlexCAN_0	I/O — — I I I	S	Tristate	15	24
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX — —	SIUL LINFlex_0 — —	I/O O — —	M	Tristate	64	100
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — — — WKPU[11][3] LIN0RX	SIUL — — — WKPU LINFlex_0	I/O — — — I I	S	Tristate	1	1
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ADC1_P[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	50
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ADC1_P[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	53
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ADC1_P[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	54

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ADC1_P[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	55
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — ADC1_S[4] WKPU[25][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	30	39
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — ADC1_S[5] WKPU[26][3]	SIUL — — — ADC WKPU	I — — — I I	I	Tristate	29	38
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — ADC1_S[6] WKPU[8][3]	SIUL — — — ADC WKPU	I/O — — — I I	J	Tristate	31	40
PB[11]	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ADC1_S[12]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	59
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ADC1_X[0]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	61
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ADC1_X[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	63
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ADC1_X[2]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	65

Table 10. Absolute maximum ratings (continued)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V_{DD_BV}	SR	Voltage on VDD_BV (regulator supply) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{SS_ADC}	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V
V_{DD_ADC}	SR	Voltage on VDD_HV_ADC (ADC reference) pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
V_{IN}	SR	Voltage on any GPIO pin with respect to ground (V_{SS})	—	–0.3	6.0	V
			Relative to V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	
I_{INJPAD}	SR	Injected input current on any pin during overload condition	—	–10	10	mA
I_{INJSUM}	SR	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
I_{AVGSEG}	SR	Sum of all the static I/O current within a supply segment[1]	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I_{CORELV}	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
$T_{STORAGE}$	SR	Storage temperature	—	–55	150	°C

1 Supply segments are described in Section 4.7.5, I/O pad current specification.

NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$), the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

4.5 Recommended operating conditions

Table 11. Recommended operating conditions (3.3 V)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{SS}	SR	—	Digital ground on VSS_HV pins	—	0	0	V
V_{DD}[1]	SR	—	Voltage on VDD_HV pins with respect to ground (V_{SS})	—	3.0	3.6	V
V_{SS_LV}[2]	SR	—	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V_{SS})	—	V_{SS} – 0.1	V_{SS} + 0.1	V

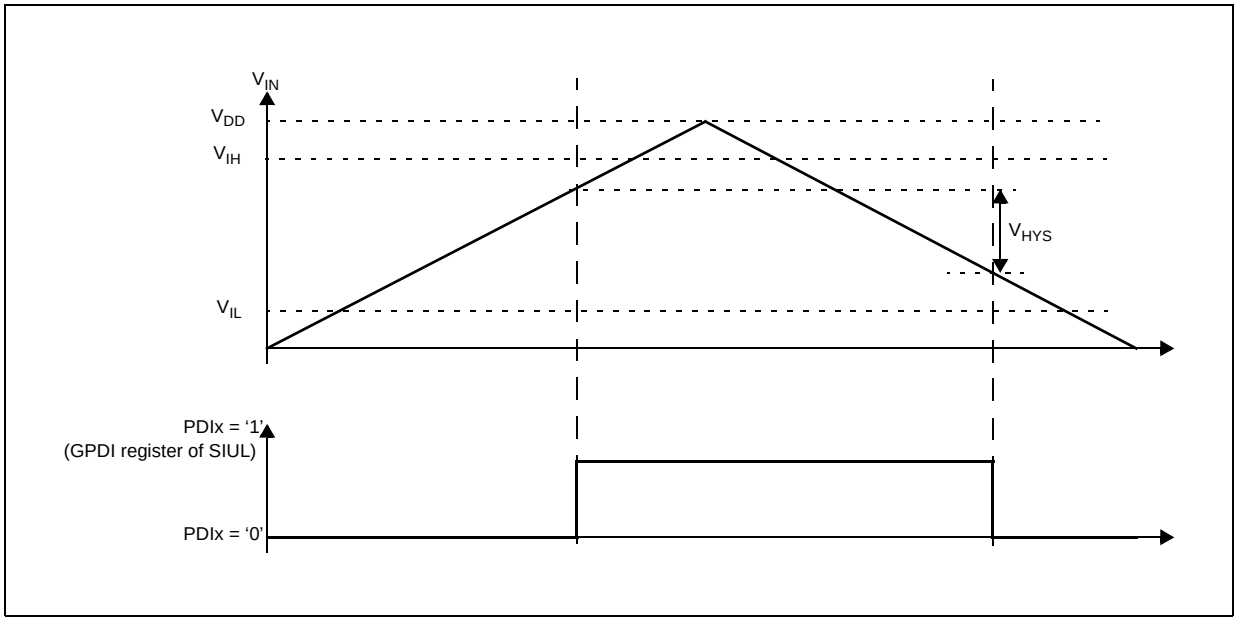

Figure 4. Input DC electrical characteristics definition

Table 14. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{IH}	SR	P	Input high level CMOS (Schmitt Trigger)	—		$0.65V_{DD}$	—	$V_{DD}+0.4$	V
V_{IL}	SR	P	Input low level CMOS (Schmitt Trigger)	—		–0.4	—	$0.35V_{DD}$	V
V_{HYS}	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		$0.1V_{DD}$	—	—	V
I_{LKG}	CC	D	Digital input leakage	No injection on adjacent pin	T_A = –40 °C	—	2	200	nA
		D			T_A = 25 °C	—	2	200	
		D			T_A = 85 °C	—	5	300	
		D			T_A = 105 °C	—	12	500	
		P			T_A = 125 °C	—	70	1000	
W_{FI}[2]	SR	P	Digital input filtered pulse	—		—	—	40	ns
W_{NFI}[(2)]	SR	P	Digital input not filtered pulse	—		1000	—	—	ns

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 15 provides weak pull figures. Both pull-up and pull-down resistances are supported.

- Table 16 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 17 provides output driver characteristics for I/O pads when in MEDIUM configuration.

Table 15. I/O pull-up/pull-down DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
$\|I_{WPU}\|$	CC	P	Weak pull-up current absolute value	$V_{IN} = V_{IL}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1[2]	10	—	250	
		P		$V_{IN} = V_{IL}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
$\|I_{WPD}\|$	CC	P	Weak pull-down current absolute value	$V_{IN} = V_{IH}$, V_{DD} = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	µA
		C			PAD3V5V = 1(2)	10	—	250	
		P		$V_{IN} = V_{IH}$, V_{DD} = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

Table 16. SLOW configuration output buffer electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
V_{OH}	CC	P	Output high level SLOW configuration	Push Pull	I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V_{DD}	—	—	V
		C			I_{OH} = –2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1[2]	0.8V_{DD}	—	—	
		C			I_{OH} = –1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V_{DD} – 0.8	—	—	
V_{OL}	CC	P	Output low level SLOW configuration	Push Pull	I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V_{DD}	V
		C			I_{OL} = 2 mA, V_{DD} = 5.0 V ± 10%, PAD3V5V = 1(2)	—	—	0.1V_{DD}	
		C			I_{OL} = 1 mA, V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 The configuration PAD3V5 = 1 when V_{DD} = 5 V is only a transient configuration during power-up. All pads but RESET are configured in input or in high impedance state.

4.7.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 19. I/O supply segment

Package	Supply segment			
	1	2	3	4
100 LQFP	pin 16 – pin 35	pin 37 – pin 69	pin 70 – pin 83	pin 84 – pin 15
64 LQFP	pin 8 – pin 26	pin 28 – pin 55	pin 56 – pin 7	—

Table 21. I/O weight[1]

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PB[3]	9%	9%	10%	10%
PC[9]	8%	8%	10%	10%
PC[14]	8%	8%	10%	10%
PC[15]	8%	11%	9%	10%
PA[2]	8%	8%	9%	9%
PE[0]	7%	7%	9%	9%
PA[1]	7%	7%	8%	8%
PE[1]	7%	10%	8%	8%
PE[8]	6%	9%	8%	8%
PE[9]	6%	6%	7%	7%
PE[10]	6%	6%	7%	7%
PA[0]	5%	7%	6%	7%
PE[11]	5%	5%	6%	6%
PC[11]	7%	7%	9%	9%
PC[10]	8%	11%	9%	10%
PB[0]	8%	11%	9%	10%
PB[1]	8%	8%	10%	10%
PC[6]	8%	8%	10%	10%
PC[7]	8%	8%	10%	10%
PA[15]	8%	11%	9%	10%
PA[14]	7%	11%	9%	9%
PA[4]	7%	7%	8%	8%
PA[13]	7%	10%	8%	9%
PA[12]	7%	7%	8%	8%
PB[9]	1%	1%	1%	1%
PB[8]	1%	1%	1%	1%
PB[10]	5%	5%	6%	6%
PD[0]	1%	1%	1%	1%
PD[1]	1%	1%	1%	1%
PD[2]	1%	1%	1%	1%
PD[3]	1%	1%	1%	1%
PD[4]	1%	1%	1%	1%

Table 21. I/O weight[1] (continued)

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PD[5]	1%	1%	1%	1%
PD[6]	1%	1%	1%	1%
PD[7]	1%	1%	1%	1%
PD[8]	1%	1%	1%	1%
PB[4]	1%	1%	1%	1%
PB[5]	1%	1%	1%	1%
PB[6]	1%	1%	1%	1%
PB[7]	1%	1%	1%	1%
PD[9]	1%	1%	1%	1%
PD[10]	1%	1%	1%	1%
PD[11]	1%	1%	1%	1%
PB[11]	9%	9%	11%	11%
PD[12]	8%	8%	10%	10%
PB[12]	8%	8%	10%	10%
PD[13]	8%	8%	9%	9%
PB[13]	8%	8%	9%	9%
PD[14]	7%	7%	9%	9%
PB[14]	7%	7%	8%	8%
PD[15]	7%	7%	8%	8%
PB[15]	6%	6%	7%	7%
PA[3]	6%	6%	7%	7%
PA[7]	4%	4%	5%	5%
PA[8]	4%	4%	5%	5%
PA[9]	4%	4%	5%	5%
PA[10]	5%	5%	6%	6%
PA[11]	5%	5%	6%	6%
PE[12]	5%	5%	6%	6%
PC[3]	5%	5%	6%	6%
PC[2]	5%	7%	6%	6%
PA[5]	5%	6%	5%	6%
PA[6]	4%	4%	5%	5%
PC[1]	5%	17%	4%	12%

Table 23. Voltage regulator electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{DEC1}	SR	—	Decoupling capacitance[2] ballast	V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 4.5 V to 5.5 V	100[3]	470[4]	—	nF
				V_{DD_BV}/V_{SS_LV} pair: V_{DD_BV} = 3 V to 3.6 V	400		—	
C_{DEC2}	SR	—	Decoupling capacitance regulator supply	V_{DD}/V_{SS} pair	10	100	—	nF
V_{MREG}	CC	T	Main regulator output voltage	Before exiting from reset	—	1.32	—	V
		P		After trimming	1.16	1.28	—	
I_{MREG}	SR	—	Main regulator current provided to V_{DD_LV} domain	—	—	—	150	mA
$I_{MREGINT}$	CC	D	Main regulator module current consumption	I_{MREG} = 200 mA	—	—	2	mA
				I_{MREG} = 0 mA	—	—	1	
V_{LPREG}	CC	P	Low-power regulator output voltage	After trimming	1.16	1.28	—	V
I_{LPREG}	SR	—	Low power regulator current provided to V_{DD_LV} domain	—	—	—	15	mA
$I_{LPREGINT}$	CC	D	Low-power regulator module current consumption	I_{LPREG} = 15 mA; T_A = 55 °C	—	—	600	µA
		—		I_{LPREG} = 0 mA; T_A = 55 °C	—	5	—	
V_{ULPREG}	CC	P	Ultra low power regulator output voltage	After trimming	1.16	1.28	—	V
I_{ULPREG}	SR	—	Ultra low power regulator current provided to V_{DD_LV} domain	—	—	—	5	mA
$I_{ULPREGINT}$	CC	D	Ultra low power regulator module current consumption	I_{ULPREG} = 5 mA; T_A = 55 °C	—	—	100	µA
				I_{ULPREG} = 0 mA; T_A = 55 °C	—	2	—	
I_{DD_BV}	CC	D	In-rush average current on V_{DD_BV} during power-up[5]	—	—	—	300[6]	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This capacitance value is driven by the constraints of the external voltage regulator supplying the V_{DD_BV} voltage. A typical value is in the range of 470 nF.

3 This value is acceptable to guarantee operation from 4.5 V to 5.5 V.

4 External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in operating range.

5 In-rush average current is seen only for short time during power-up and on standby exit (maximum 20 µs, depending on external capacitances to be loaded).

6 The duration of the in-rush current depends on the capacitance placed on LV pins. BV decoupling capacitors must be sized accordingly. Refer to I_{MREG} value for minimum amount of current to be provided in cc.

Table 26. Program and erase specifications (code flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$t_{dwprogram}$	CC	C	Double word (64 bits) program time[4]	—	22	50	500	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	300	500	5000	ms
$t_{32Kpperase}$	CC	C	32 KB block preprogram and erase time	—	400	600	5000	ms
$t_{128Kpperase}$	CC	C	128 KB block preprogram and erase time	—	800	1300	7500	ms
t_{esus}	CC	C	Erase suspend latency	—	—	30	30	µs

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 27. Program and erase specifications (data flash)

Symbol		C	Parameter	Value				Unit
				Min	Typ[1]	Initial max[2]	Max[3]	
$t_{swprogram}$	CC	C	Single word (32 bits) program time[4]	—	30	70	300	µs
$t_{16Kpperase}$	CC	C	16 KB block preprogram and erase time	—	700	800	1500	ms
t_{Bank_D}	CC	C	64 KB block preprogram and erase time	—	1900	2300	4800	ms

1 Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

2 Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

3 The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

4 Actual hardware programming times. This does not include software overhead.

Table 28. Flash module life

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block over the operating temperature range (T_J)	16 KB blocks	100,000	—	—	cycles
				32 KB blocks	10,000	100,000	—	cycles
				128 KB blocks	1,000	100,000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature[1]	Blocks with 0–1,000 P/E cycles	20	—	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	—	
				Blocks with 10,001–100,000 P/E cycles	5	—	—	

1 Ambient temperature averaged over application duration. It is recommended not to exceed the product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 29. Flash memory read access timing

Symbol		C	Parameter	Conditions[1]	Max	Unit
f_{CFREAD}	CC	P	Maximum working frequency for reading code flash memory at given number of wait states in worst conditions	2 wait states	48	MHz
		C		0 wait states	20	
f_{DFREAD}	CC	P	Maximum working frequency for reading data flash memory at given number of wait states in worst conditions	6 wait states	48	MHz

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.11.2 Flash power supply DC characteristics

Table 30 shows the power supply DC characteristics on external supply.

NOTE

Power supply for data flash is actually provided by code flash; this means that data flash cannot work if code flash is not powered.

Table 30. Flash power supply DC electrical characteristics

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{CFREAD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on read access	Flash module read f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFREAD}	CC	D			Data flash	—	—	4	mA
I_{CFMOD}	CC	D	Sum of the current consumption on V_{DDHV} and V_{DDBV} on matrix modification (program/erase)	Program/Erase on-going while reading flash registers, f_{CPU} = 48 MHz	Code flash	—	—	33	mA
I_{DFMOD}	CC	D			Data flash	—	—	6	mA

— Corrupted program counter
— Unexpected reset
— Critical data corruption (control registers...)

- Prequalification trials – Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.

  To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

Table 32. EMI radiated emission measurement[1] [2]

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
—	SR	—	Scan range	—		0.150	—	1000	MHz
f_{CPU}	SR	—	Operating frequency	—		—	48	—	MHz
V_{DD_LV}	SR	—	LV operating voltages	—		—	1.28	—	V
S_{EMI}	CC	T	Peak level	V_{DD} = 5 V, T_A = 25 °C, 100 LQFP package Test conforming to IEC 61967-2, f_{OSC} = 8 MHz/f_{CPU} = 48 MHz	No PLL frequency modulation	—	—	18	dBµV
					± 2% PLL frequency modulation	—	—	14	dBµV

1 EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

2 For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance C_{P1} and C_{P2} to the sampling capacitance C_S occurs (C_S is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which C_{P2} is reported in parallel to C_{P1} (call $C_P = C_{P1} + C_{P2}$), the two capacitances C_P and C_S are in series, and the time constant is

Eqn. 5

$$\tau_1 = (R_{SW} + R_{AD}) \bullet \frac{C_P \bullet C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only C_S as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time t_s is always much longer than the internal time constant:

Eqn. 6

$$\tau_1 < (R_{SW} + R_{AD}) \bullet C_S \ll t_s$$

The charge of C_{P1} and C_{P2} is redistributed also on C_S, determining a new value of the voltage V_{A1} on the capacitance according to Equation 7:

Eqn. 7

$$V_{A1} \bullet (C_S + C_{P1} + C_{P2}) = V_A \bullet (C_{P1} + C_{P2})$$

2. A second charge transfer involves also C_F (that is typically bigger than the on-chip capacitance) through the resistance R_L: again considering the worst case in which C_{P2} and C_S were in parallel to C_{P1} (since the time constant in reality would be faster), the time constant is:

Eqn. 8

$$\tau_2 < R_L \bullet (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time t_s, a constraints on R_L sizing is obtained:

Eqn. 9

$$10 \bullet \tau_2 = 10 \bullet R_L \bullet (C_S + C_{P1} + C_{P2}) < t_s$$

Of course, R_L shall be sized also according to the current limitation constraints, in combination with R_S (source impedance) and R_F (filter resistance). Being C_F definitively bigger than C_{P1}, C_{P2} and C_S, then the final voltage V_{A2} (at the end of the charge transfer transient) will be much higher than V_{A1}. Equation 10 must be respected (charge balance assuming now C_S already charged at V_{A1}):

Eqn. 10

$$V_{A2} \bullet (C_S + C_{P1} + C_{P2} + C_F) = V_A \bullet C_F + V_{A1} \bullet (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the $R_F C_F$ filter, is not able to provide the extra charge to compensate the voltage drop on C_S with respect to the ideal source V_A; the time constant $R_F C_F$ of the filter is very high with respect to the sampling time (t_s). The filter is typically designed to act as anti-aliasing.

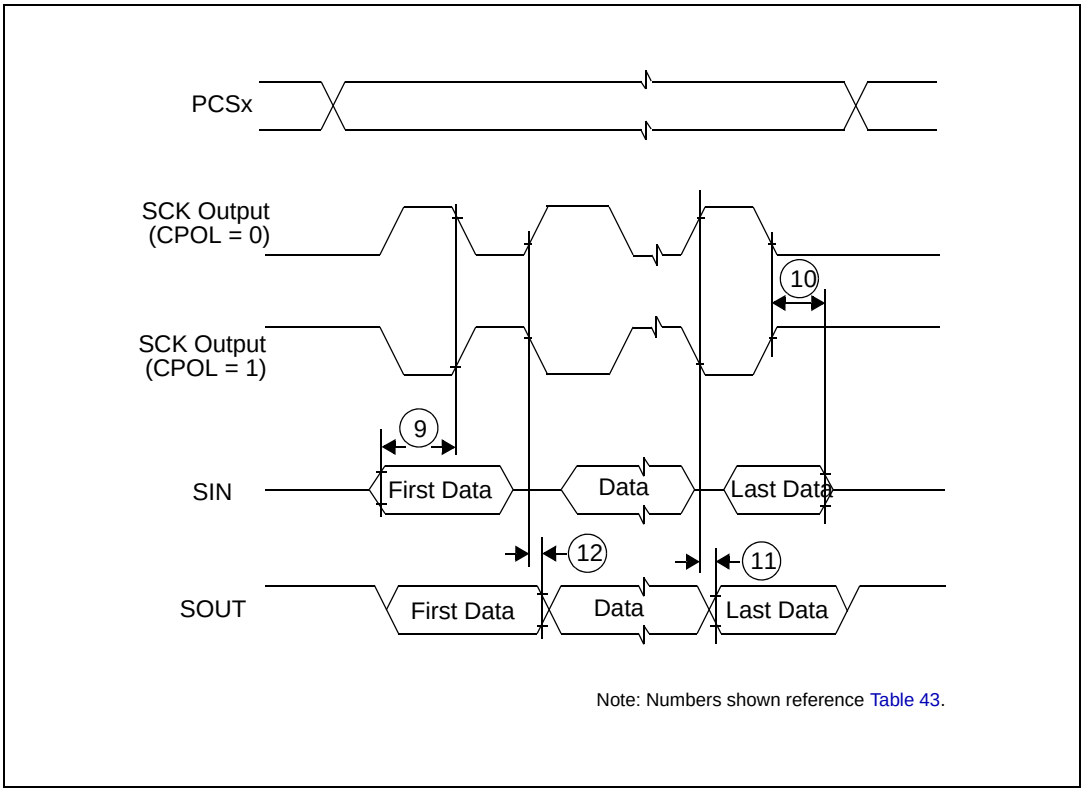

Figure 17. DSPI classic SPI timing – master, CPHA = 1

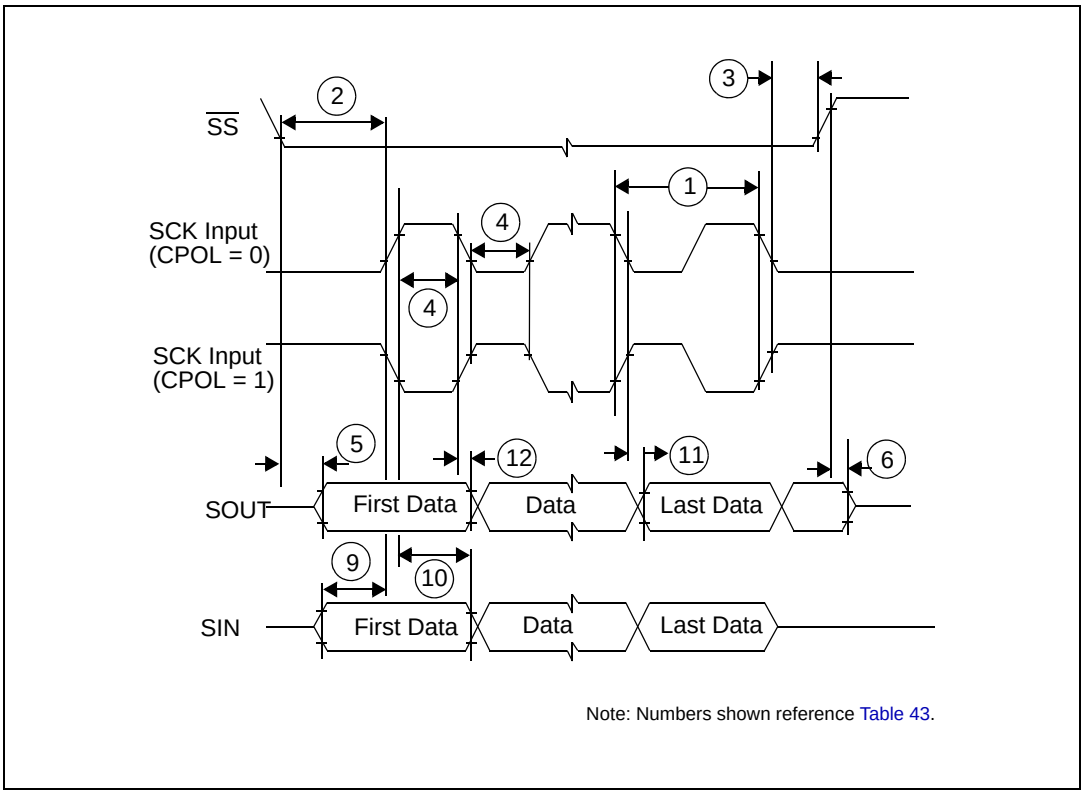

Figure 18. DSPI classic SPI timing – slave, CPHA = 0

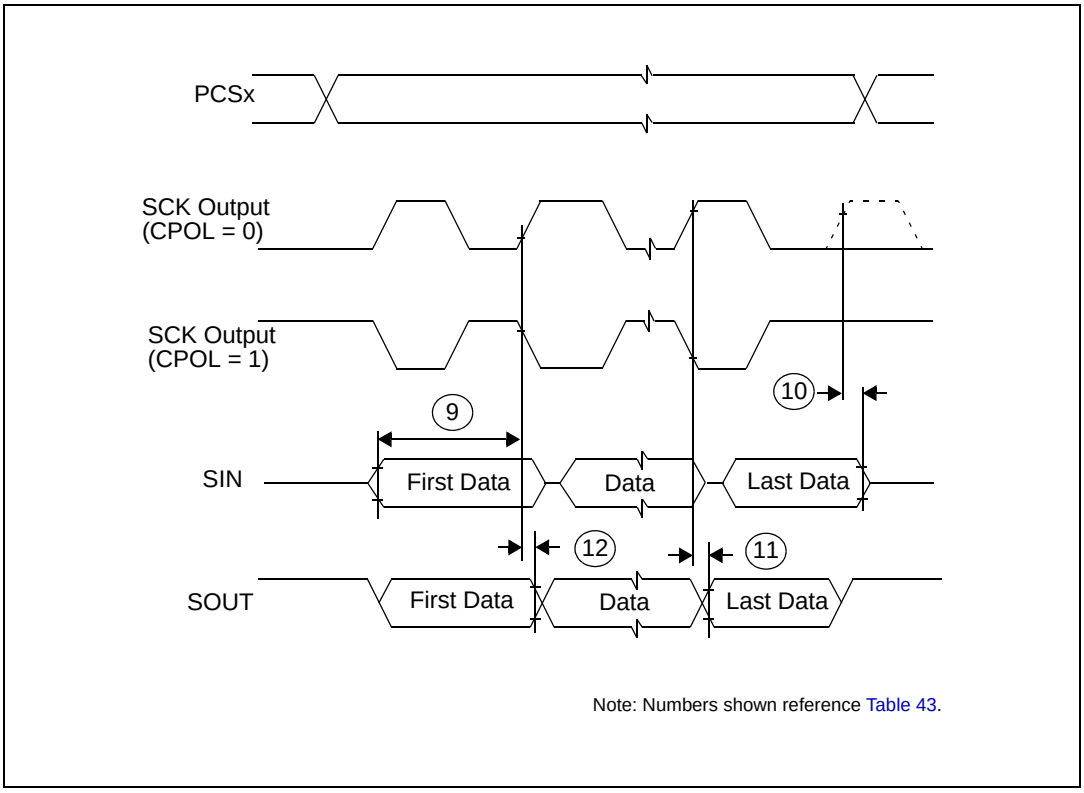

Figure 21. DSPI modified transfer format timing – master, CPHA = 1

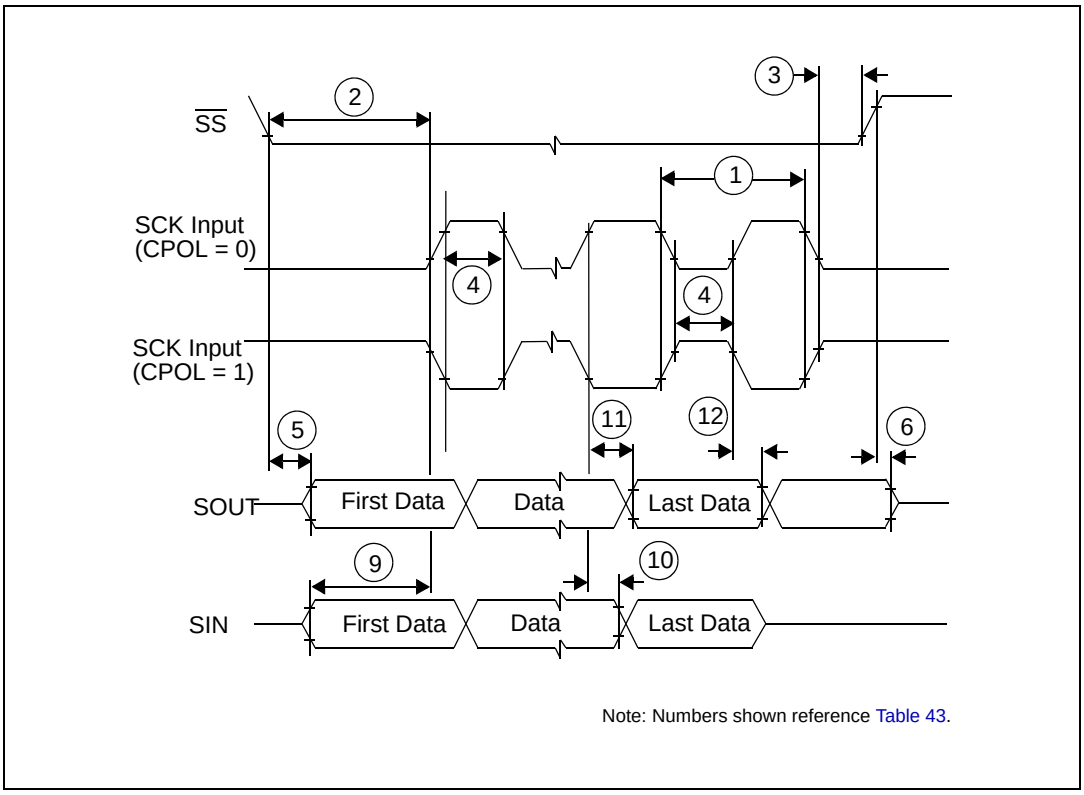

Figure 22. DSPI modified transfer format timing – slave, CPHA = 0

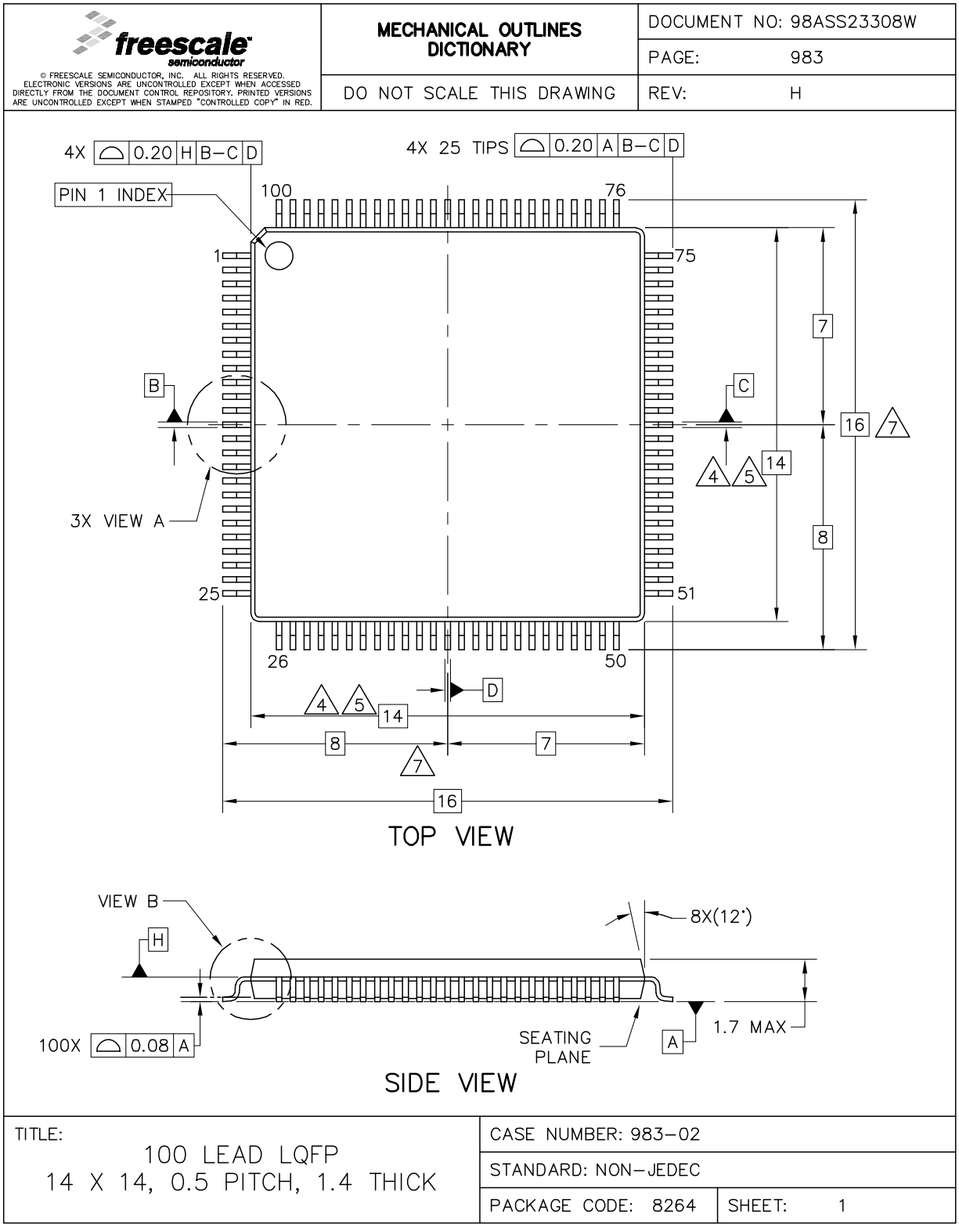

Figure 26. 100 LQFP package mechanical drawing (Part 1 of 3)

5.1.2 64 LQFP

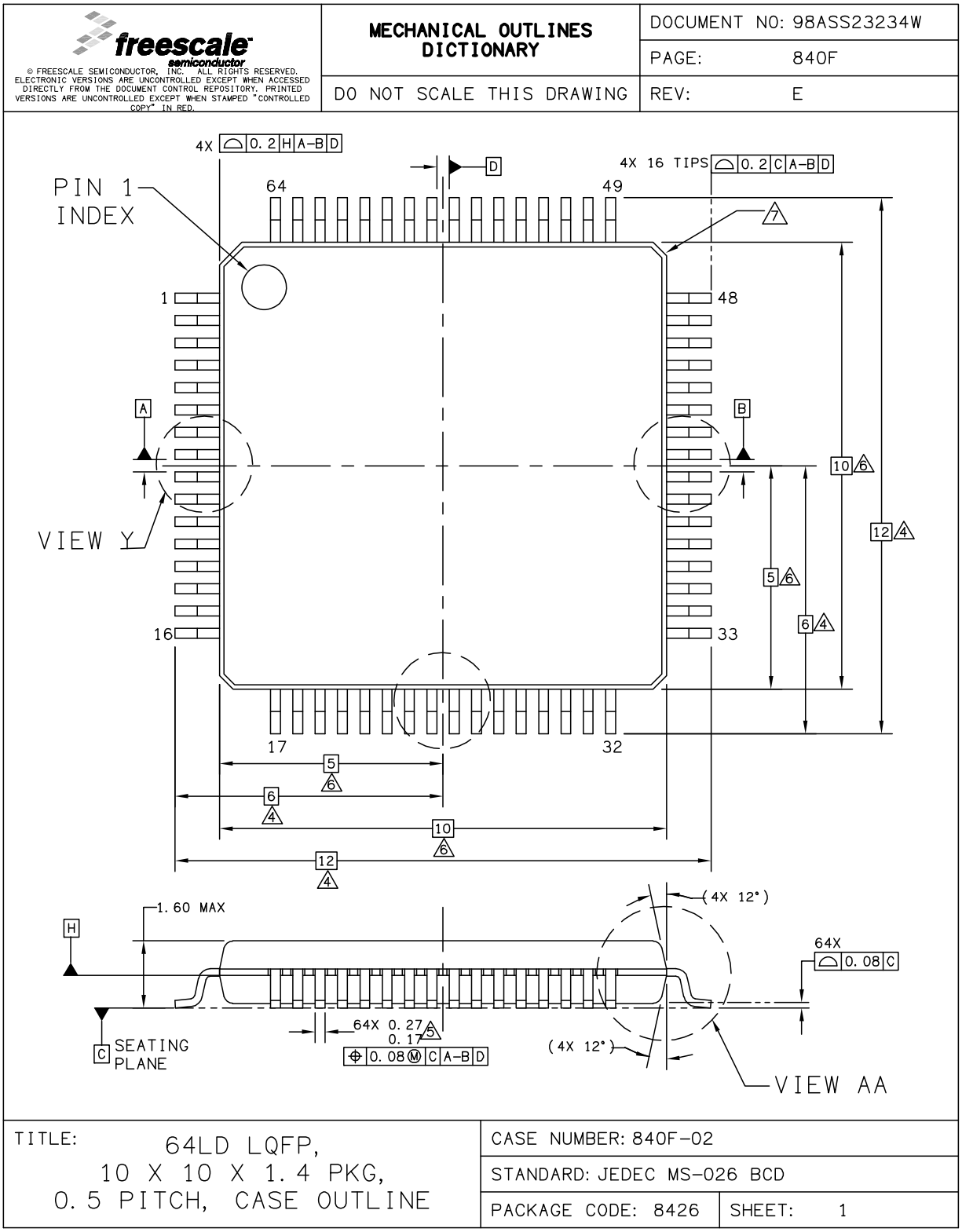

Figure 29. 64 LQFP mechanical drawing (part 1 of 3)

6 Ordering information

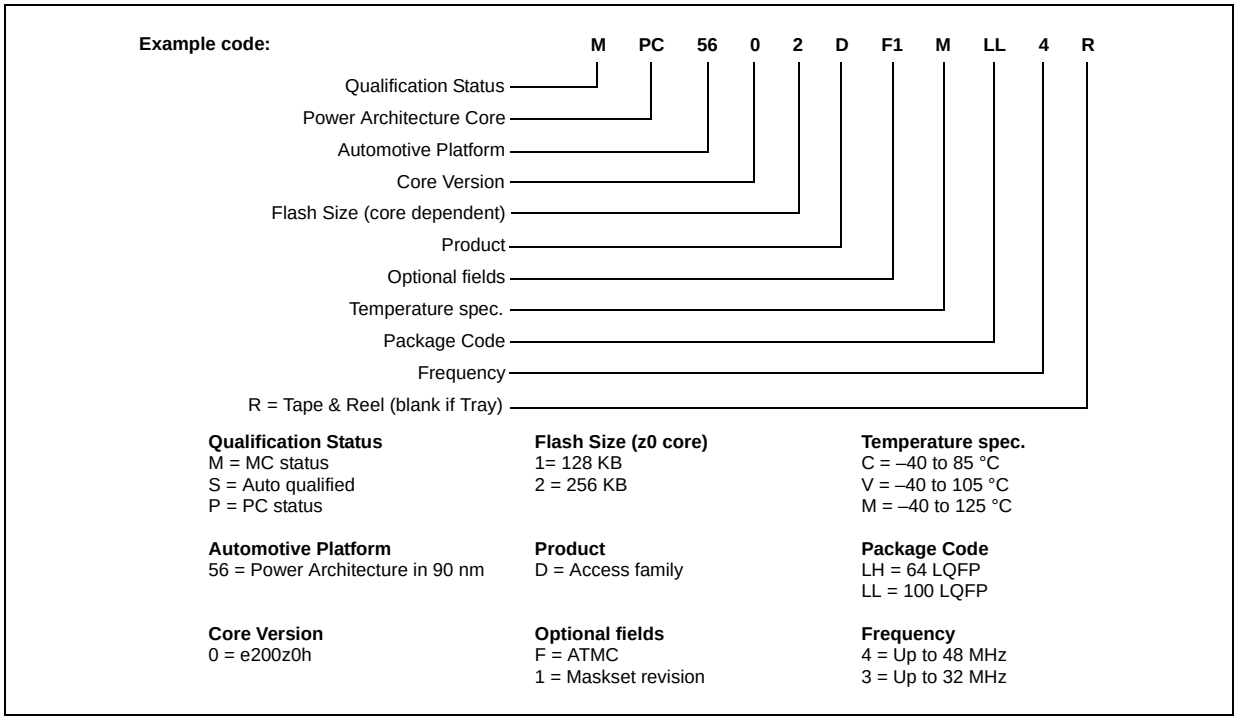

Figure 32. Commercial product code structure

Table 45. Revision history (continued)

Revision	Date	Description of Changes
4	14 Jul 2011	Formatting and editorial changes throughout Device comparison table: for the “Total timer I/O eMIOS”, changed “13 ch” to “14 ch” Features: Replaced “e200z0“ with “e200z0h”; added an explanation of which LINFlex modules support master mode and slave MPC5601D/MPC5602D series block summary: • added definition for “AUTOSAR” acronym changed “System watchdog timer” to “Software watchdog timer”64 LQFP pin configuration (top view): changed pin 6 from VPP_TEST to VSS_HV Added section “Pad configuration during reset phases” Added section “Voltage supply pins” Added section “Pad types” Added section “System pins” Renamed and updated section “Functional ports” (was previously section “Pin muxing”); update includes replacing all instances of WKUP with WKPU (WKPU is the correct abbreviation for Wakeup Unit) Section “NVUSRO register”: edited content to separate configuration into electrical parameters and digital functionality Added section “NVUSRO[WATCHDOG_EN] field description” Absolute maximum ratings: Removed “C” column from table Replaced “TBD” with “—” in T_{VDD} min value cell of 3.3 V and 5 V recommended operating conditions tables LQFP thermal characteristics: removed $R_{\theta JB}$ single layer board conditions; updated footnote 4 I/O input DC electrical characteristics: removed footnote “All values need to be confirmed during device validation”; updated I_{LKG} characteristics MEDIUM configuration output buffer electrical characteristics: changed “I_{OH} = 100 µA” to “I_{OL} = 100 µA” in V_{OL} conditions I/O consumption: replaced instances of “Root medium square” with “Root mean square” Updated section “Voltage regulator electrical characteristics” Section “Low voltage detector electrical characteristics”: changed title (was “Voltage monitor electrical characteristics”); added a fifth LVD (LVDHV3B); added event status flag names found in RGM chapter of device reference manual to POR module and LVD descriptions; replaced instances of “Low voltage monitor” with “Low voltage detector”; deleted note referencing power domain No. 2 (this domain is not present on the device); updated electrical characteristics table Updated and renamed section “Power consumption” (was previously section “Low voltage domain power consumption”) Program and erase specifications (code flash): updated symbols; updated t_{esus} values Updated Flash memory read access timing EMI radiated emission measurement: updated S_{EMI} values Updated FMPLL electrical characteristics Crystal oscillator and resonator connection scheme: inserted footnote about possibly requiring a series resistor Fast internal RC oscillator (16 MHz) electrical characteristics: updated t_{FIRCSU} values Section “Input impedance and ADC accuracy”: changed “V_A/V_{A2}” to “V_{A2}/V_A” in Equation 13 ADC conversion characteristics: • updated conditions for sampling time V_{DD} = 5.0 V • updated conditions for conversion time V_{DD} = 5.0 V Commercial product code structure: added character for frequency; updated optional fields character and description Restored the revision history table and added an entry for Rev. 3.1 Updated Abbreviations