Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z0h
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	79
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 16
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 33x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5602df1vll4r

Table of Contents

1 Introduction 3
1.1 Document overview 3
1.2 Description 3
2 Block diagram 4
3 Package pinouts and signal descriptions 7
3.1 Package pinouts 7
3.2 Pad configuration during reset phases 9
3.3 Voltage supply pins 9
3.4 Pad types 10
3.5 System pins 10
3.6 Functional ports 11
4 Electrical characteristics 21
4.1 Introduction 21
4.2 Parameter classification 21
4.3 NVUSRO register 21
4.3.1 NVUSRO[PAD3V5V] field description 22
4.3.2 NVUSRO[OSCILLATOR_MARGIN] field description 22
4.3.3 NVUSRO[WATCHDOG_EN] field description . . 22
4.4 Absolute maximum ratings 22
4.5 Recommended operating conditions 23
4.6 Thermal characteristics 26
4.6.1 Package thermal characteristics 26
4.6.2 Power considerations 26
4.7 I/O pad electrical characteristics 27
4.7.1 I/O pad types 27
4.7.2 I/O input DC characteristics 27
4.7.3 I/O output DC characteristics 28
4.7.4 Output pin transition times 31
4.7.5 I/O pad current specification 31
4.8 RESET electrical characteristics 35
4.9 Power management electrical characteristics 37
4.9.1 Voltage regulator electrical characteristics 37
4.9.2 Low voltage detector electrical characteristics . 40
4.10 Power consumption 41
4.11 Flash memory electrical characteristics 42
4.11.1 Program/Erase characteristics 42
4.11.2 Flash power supply DC characteristics 44
4.11.3 Start-up/Switch-off timings 45
4.12 Electromagnetic compatibility (EMC) characteristics . . 45
4.12.1 Designing hardened software to avoid noise problems 45
4.12.2 Electromagnetic interference (EMI) 46
4.12.3 Absolute maximum ratings (electrical sensitivity) 46
4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics 48
4.14 FMPLL electrical characteristics 51
4.15 Fast internal RC oscillator (16 MHz) electrical characteristics 51
4.16 Slow internal RC oscillator (128 kHz) electrical characteristics 52
4.17 ADC electrical characteristics 54
4.17.1 Introduction 54
4.17.2 Input impedance and ADC accuracy 55
4.17.3 ADC electrical characteristics 60
4.18 On-chip peripherals 62
4.18.1 Current consumption 62
4.18.2 DSPI characteristics 63
4.18.3 JTAG characteristics 70
5 Package characteristics 70
5.1 Package mechanical data 70
5.1.1 100 LQFP 70
5.1.2 64 LQFP 74
6 Ordering information 77
7 Document revision history 78

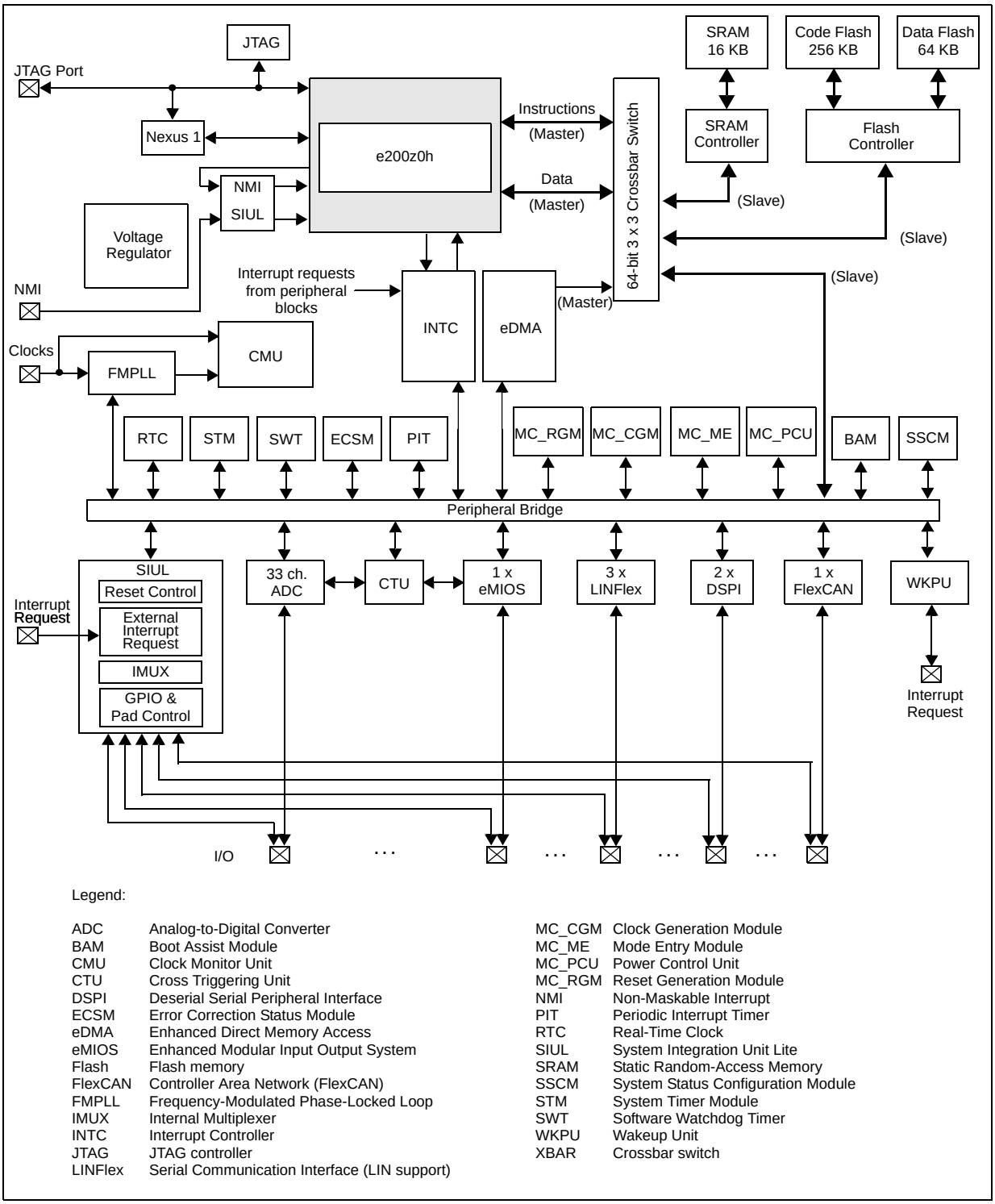

Figure 1. MPC5602D series block diagram

Table 2 summarizes the functions of all blocks present in the MPC5602D series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

Figure 3 shows the MPC5602D in the 64 LQFP package.

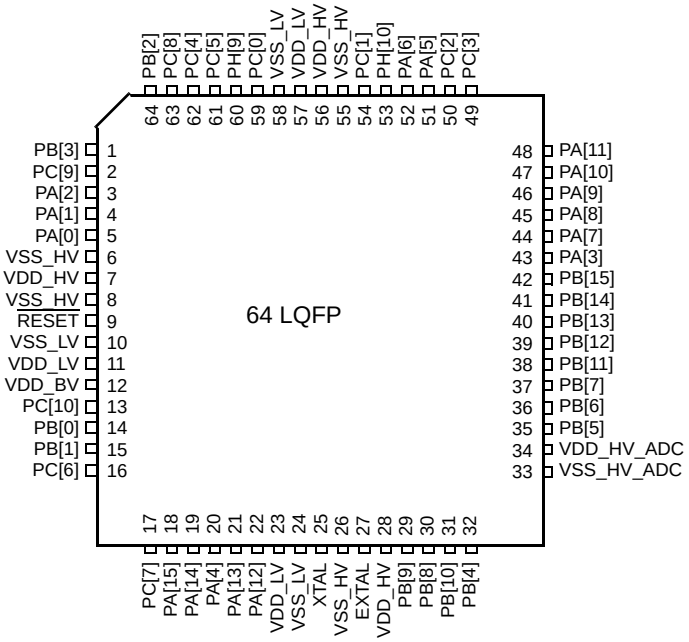

Figure 3. 64 LQFP pin configuration (top view)

3.2 Pad configuration during reset phases

All pads have a fixed configuration under reset.

During the power-up phase, all pads are forced to tristate.

After power-up phase, all pads are forced to tristate with the following exceptions:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS[0]) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS and TDI) are pull-up while TDO remains tristate.
- Precise ADC pads (PB[7:4] and PD[11:0]) are left tristate (no output buffer available).
- Main oscillator pads (EXTAL, XTAL) are tristate.

3.3 Voltage supply pins

Voltage supply pins are used to provide power to the device. Two dedicated pins are used for 1.2 V regulator stabilization.

Table 5. Functional port pin descriptions (continued)

Port pin	PCR	Alternate function[1]	Function	Peripheral	I/O direction[2]	Pad type	RESET configuration	Pin number	
								64 LQFP	100 LQFP
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKPU[12][3]	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	26
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX E0UC[3] —	SIUL LINFlex_2 eMIOS_0 —	I/O O I/O —	S	Tristate	63	99
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — E0UC[7] — LIN2RX WKPU[13][3]	SIUL — eMIOS_0 — LINFlex_2 WKPU	I/O — I/O — I I	S	Tristate	2	2
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] — — MA[1]	SIUL — — ADC	I/O — — O	M	Tristate	13	22
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 —	GPIO[43] — — MA[2] WKPU[5][3]	SIUL — — ADC WKPU	I/O — — O I	S	Tristate	—	21
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — EIRQ[19]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	97
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	98
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] — — EIRQ[8]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	S	Tristate	—	3
PC[15]	PCR[47]	AF0 AF1 AF2 AF3 —	GPIO[47] E0UC[15] — — EIRQ[20]	SIUL eMIOS_0 — — SIUL	I/O I/O — — I	M	Tristate	—	4

NOTE

SRAM data retention is guaranteed with V_{DD_LV} not below 1.08 V.

4.6 Thermal characteristics

4.6.1 Package thermal characteristics

Table 13. LQFP thermal characteristics[1]

Symbol		C	Parameter	Conditions[2]		Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection[3]	Single-layer board —1s	LQFP64	72.1	°C/W
					LQFP100	65.2	
				Four-layer board — 2s2p	LQFP64	57.3	
					LQFP100	51.8	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board[4]	Four-layer board — 2s2p	LQFP64	44.1	°C/W
					LQFP100	41.3	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case[5]	Single-layer board — 1s	LQFP64	26.5	°C/W
					LQFP100	23.9	
				Four-layer board — 2s2p	LQFP64	26.2	
					LQFP100	23.7	
Ψ_{JB}	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	41	°C/W
					LQFP100	41.6	
				Four-layer board — 2s2p	LQFP64	43	
					LQFP100	43.4	
Ψ_{JC}	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board — 1s	LQFP64	11.5	°C/W
					LQFP100	10.4	
				Four-layer board — 2s2p	LQFP64	11.1	
					LQFP100	10.2	

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C

3 Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-7. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as R_{thJA}.

4 Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as R_{thJB}.

5 Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as R_{thJC}.

4.6.2 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using Equation 1:

4.7.4 Output pin transition times

Table 18. Output pin transition times

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_{tr}	CC	D	Output transition time output pin[2] SLOW configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C_L = 50 pF		—	—	100	
		D		C_L = 100 pF		—	—	125	
t_{tr}	CC	D	Output transition time output pin(2) MEDIUM configuration	C_L = 25 pF	V_{DD} = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C_L = 50 pF		—	—	20	
		D		C_L = 100 pF		—	—	40	
		D		C_L = 25 pF	V_{DD} = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C_L = 50 pF		—	—	25	
		D		C_L = 100 pF		—	—	40	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

2 C_L includes device and package capacitances (C_{PKG} < 5 pF).

4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in Table 19.

Table 20 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{AVGSEG} maximum value.

Table 19. I/O supply segment

Package	Supply segment			
	1	2	3	4
100 LQFP	pin 16 – pin 35	pin 37 – pin 69	pin 70 – pin 83	pin 84 – pin 15
64 LQFP	pin 8 – pin 26	pin 28 – pin 55	pin 56 – pin 7	—

Table 21. I/O weight[1] (continued)

Pad	100 LQFP/64 LQFP			
	Weight 5 V		Weight 3.3 V	
	SRC[2] = 0	SRC = 1	SRC = 0	SRC = 1
PD[5]	1%	1%	1%	1%
PD[6]	1%	1%	1%	1%
PD[7]	1%	1%	1%	1%
PD[8]	1%	1%	1%	1%
PB[4]	1%	1%	1%	1%
PB[5]	1%	1%	1%	1%
PB[6]	1%	1%	1%	1%
PB[7]	1%	1%	1%	1%
PD[9]	1%	1%	1%	1%
PD[10]	1%	1%	1%	1%
PD[11]	1%	1%	1%	1%
PB[11]	9%	9%	11%	11%
PD[12]	8%	8%	10%	10%
PB[12]	8%	8%	10%	10%
PD[13]	8%	8%	9%	9%
PB[13]	8%	8%	9%	9%
PD[14]	7%	7%	9%	9%
PB[14]	7%	7%	8%	8%
PD[15]	7%	7%	8%	8%
PB[15]	6%	6%	7%	7%
PA[3]	6%	6%	7%	7%
PA[7]	4%	4%	5%	5%
PA[8]	4%	4%	5%	5%
PA[9]	4%	4%	5%	5%
PA[10]	5%	5%	6%	6%
PA[11]	5%	5%	6%	6%
PE[12]	5%	5%	6%	6%
PC[3]	5%	5%	6%	6%
PC[2]	5%	7%	6%	6%
PA[5]	5%	6%	5%	6%
PA[6]	4%	4%	5%	5%
PC[1]	5%	17%	4%	12%

— LV_CFLA: Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
— LV_DFLA: Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV_COR through double bonding.
— LV_PLL: Low voltage supply for FMPLL. It is shorted to LV_COR through double bonding.

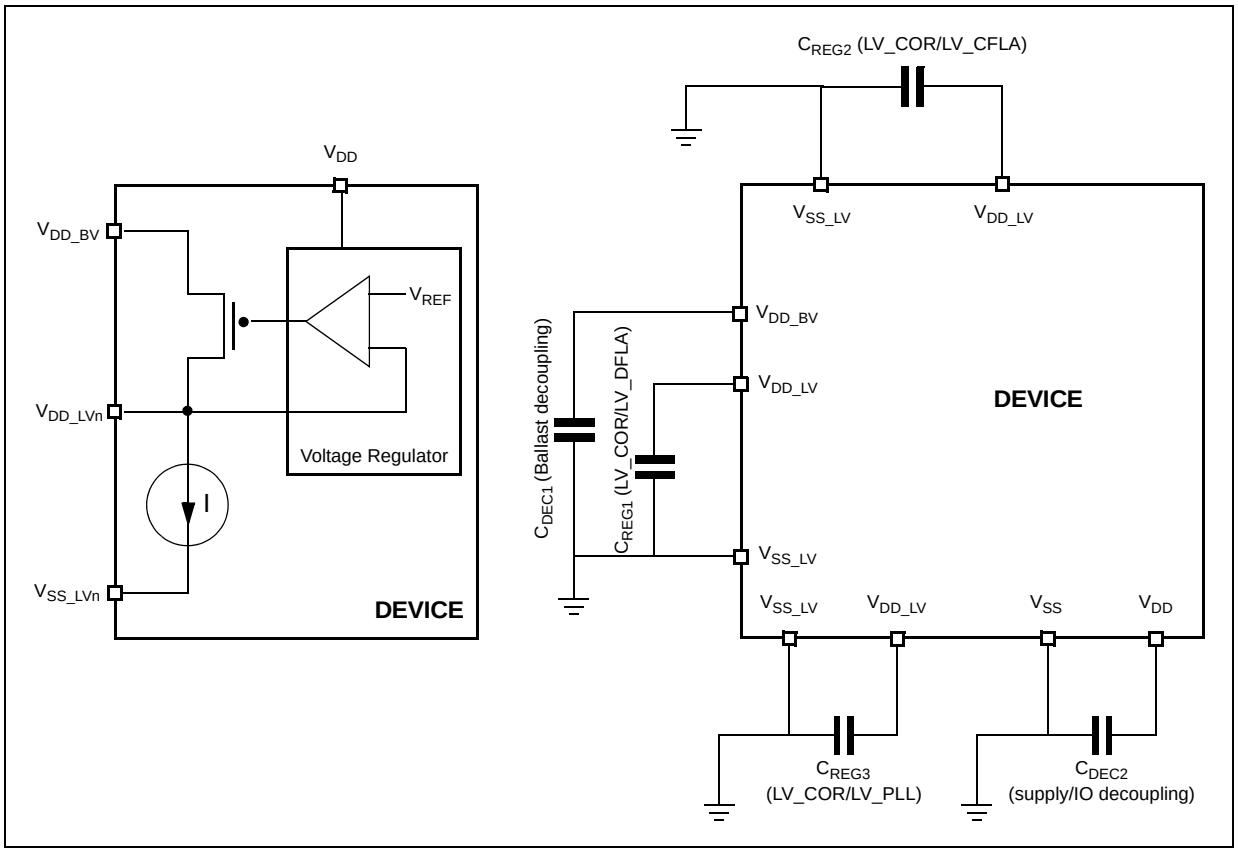

Figure 7. Voltage regulator capacitance connection

The internal voltage regulator requires external capacitance (C_{REGn}) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.

Each decoupling capacitor must be placed between each of the three V_{DD_LV}/V_{SS_LV} supply pairs to ensure stable voltage (see Section 4.5, Recommended operating conditions).

Table 23. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
C_{REGn}	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R_{REG}	SR	—	Stability capacitor equivalent serial resistance	Range: 10 kHz to 20 MHz	—	—	0.2	Ω

Table 24. Low voltage detector electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{PORUP}	SR	P	Supply for functional POR module	T_A = 25 °C, after trimming	1.0	—	5.5	V
V_{PORH}	CC	P	Power-on reset threshold		1.5	—	2.6	V
$V_{LVDHV3H}$	CC	T	LVDHV3 low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3L}$	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV3BH}$	CC	P	LVDHV3B low voltage detector high threshold		—	—	2.95	V
$V_{LVDHV3BL}$	CC	P	LVDHV3B low voltage detector low threshold		2.6	—	2.9	V
$V_{LVDHV5H}$	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	V
$V_{LVDHV5L}$	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	V
$V_{LVDLVCORL}$	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.16	V
$V_{LVDLVBKPL}$	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.16	V

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified

4.10 Power consumption

Table 25 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 25. Power consumption on VDD_BV and VDD_HV

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
I_{DDMAX}[2]	CC	D	RUN mode maximum average current	—		—	90	130[3]	mA
I_{DDRUN}[4]	CC	T	RUN mode typical average current[5]	f_{CPU} = 8 MHz		—	7	—	mA
		T		f_{CPU} = 16 MHz		—	18	—	
		T		f_{CPU} = 32 MHz		—	29	—	
		P		f_{CPU} = 48 MHz		—	40	100	
I_{DDHALT}	CC	C	HALT mode current[6]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	8	15	mA
		P			T_A = 125 °C	—	14	25	
I_{DDSTOP}	CC	P	STOP mode current[7]	Slow internal RC oscillator (128 kHz) running	T_A = 25 °C	—	180	700[8]	µA
		D			T_A = 55 °C	—	500	—	
		D			T_A = 85 °C	—	1	6[(8)]	mA
		D			T_A = 105 °C	—	2	9[(8)]	
		P			T_A = 125 °C	—	4.5	12[(8)]	

4.14 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

Table 37. FMPLL electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{PLLIN}	SR	—	FMPLL reference clock[2]	—	4	—	48	MHz
Δ_{PLLIN}	SR	—	FMPLL reference clock duty cycle[(2)]	—	40	—	60	%
f_{PLLOUT}	CC	D	FMPLL output clock frequency	—	16	—	48	MHz
f_{VCO}[3]	CC	P	VCO frequency without frequency modulation	—	256	—	512	MHz
			VCO frequency with frequency modulation	—	245	—	533	
f_{CPU}	SR	—	System clock frequency	—	—	—	48	MHz
f_{FREE}	CC	P	Free-running frequency	—	20	—	150	MHz
t_{LOCK}	CC	P	FMPLL lock time	Stable oscillator (f_{PLLIN} = 16 MHz)	—	40	100	µs
Δt_{LTJIT}	CC	—	FMPLL long term jitter	f_{PLLIN} = 16 MHz (resonator), f_{PLLCLK} at 48 MHz, 4,000 cycles	—	—	10	ns
I_{PLL}	CC	C	FMPLL consumption	T_A = 25 °C	—	—	4	mA

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f_{PLLIN} and Δ_{PLLIN}.

3 Frequency modulation is considered ±4%.

4.15 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 38. Fast internal RC oscillator (16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
f_{FIRC}	CC	P	Fast internal RC oscillator high frequency	T_A = 25 °C, trimmed	—	16	—	MHz
	SR	—		—	12		20	
$I_{FIRCRUN}$[2],	CC	T	Fast internal RC oscillator high frequency current in running mode	T_A = 25 °C, trimmed	—	—	200	µA
$I_{FIRCPWD}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	T_A = 25 °C	—	—	10	µA

Table 39. Slow internal RC oscillator (128 kHz) electrical characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
$\Delta_{SIRCVAR}$	CC	P	Slow internal RC oscillator variation in temperature and supply with respect to f_{SIRC} at T_A = 55 °C in high frequency configuration	High frequency configuration	–10	—	10	%

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

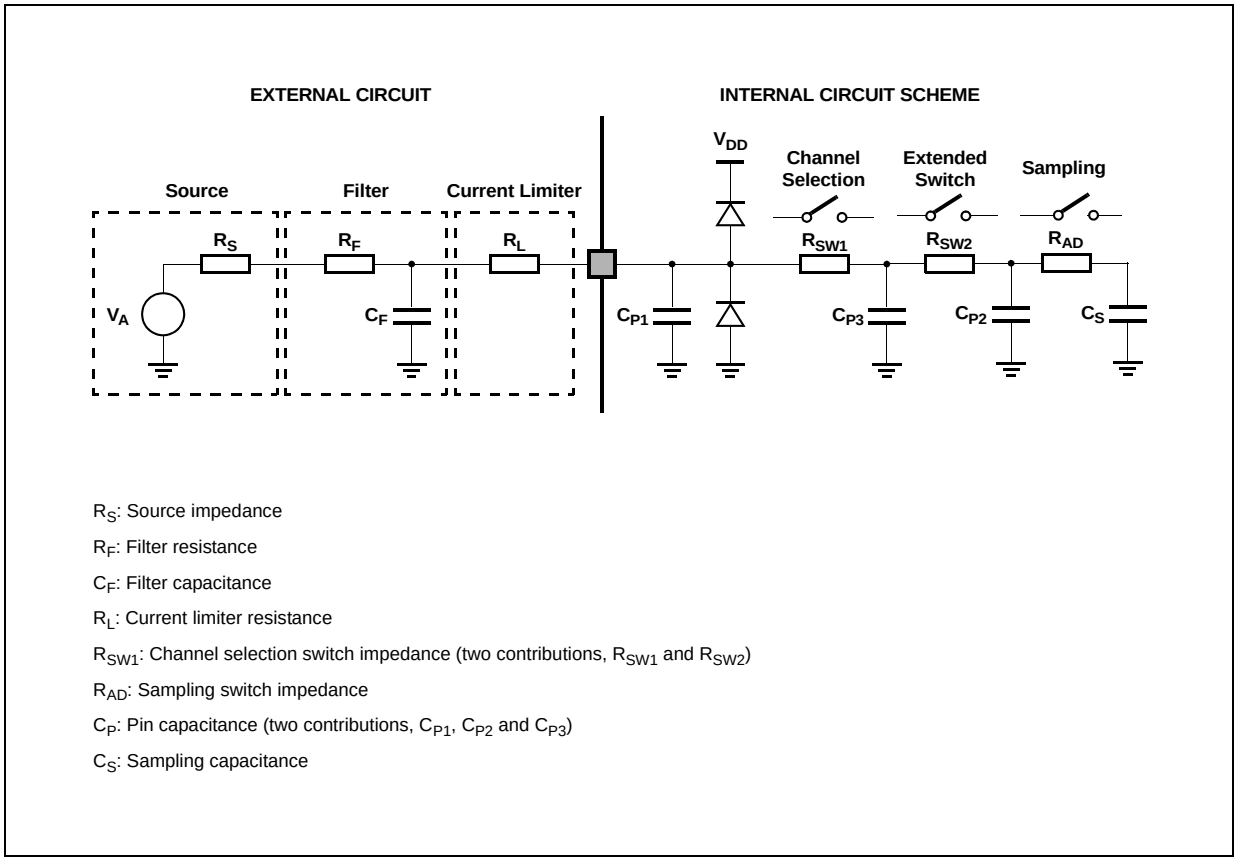

Figure 13. Input equivalent circuit (extended channels)

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances C_F, C_{P1} and C_{P2} are initially charged at the source voltage V_A (refer to the equivalent circuit in Figure 13): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

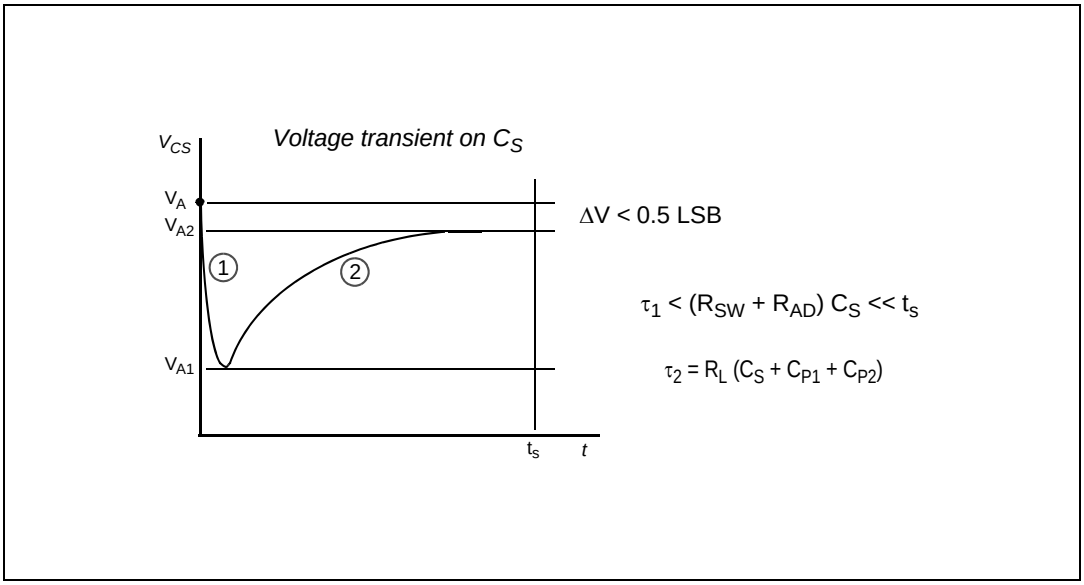

Figure 14. Transient behavior during sampling phase

4.17.3 ADC electrical characteristics

Table 40. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I_{LKG}	CC	C	Input leakage current	T_A = –40 °C	No current injection on adjacent pin	—	1	—	nA
		C		T_A = 25 °C		—	1	—	
		C		T_A = 105 °C		—	8	200	
		P		T_A = 125 °C		—	45	400	

Table 41. ADC conversion characteristics

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
V_{SS_ADC}	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V_{SS})[2]	—	–0.1	—	0.1	V
V_{DD_ADC}	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V_{SS})	—	V_{DD} – 0.1	—	V_{DD} + 0.1	V
V_{AINx}	SR	—	Analog input voltage[3]	—	V_{SS_ADC} – 0.1	—	V_{DD_ADC} + 0.1	V
f_{ADC}	SR	—	ADC analog frequency	V_{DD} = 5.0 V	3.33	—	32 + 4%	MHz
				V_{DD} = 3.3 V	3.33	—	20 + 4%	
Δ_{ADC_SYS}	SR	—	ADC clock duty cycle (ipg_clk)	ADCLKSEL = 1[4]	45	—	55	%
t_{ADC_PU}	SR	—	ADC power up delay	—	—	—	1.5	µs
t_s	CC	T	Sampling time[5] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPSAMP = 12	600	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs
		T	Sampling time(5) V_{DD} = 5.0 V	f_{ADC} = 24 MHz, INPSAMP = 13	500	—	—	ns
				f_{ADC} = 3.33 MHz, INPSAMP = 255	—	—	76.2	µs

Table 41. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]		Value			Unit
						Min	Typ	Max	
t_c	CC	P	Conversion time[6] V_{DD} = 3.3 V	f_{ADC} = 20 MHz, INPCMP = 0		2.4	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
		P	Conversion time[(6)] V_{DD} = 5.0 V	f_{ADC} = 32 MHz, INPCMP = 0		1.5	—	—	µs
				f_{ADC} = 13.33 MHz, INPCMP = 0		—	—	3.6	
C_S	CC	D	ADC input sampling capacitance	—		5			pF
C_{P1}	CC	D	ADC input pin capacitance 1	—		3			pF
C_{P2}	CC	D	ADC input pin capacitance 2	—		1			pF
C_{P3}	CC	D	ADC input pin capacitance 3	—		1.5			pF
R_{SW1}	CC	D	Internal resistance of analog source	—		—	—	1	kΩ
R_{SW2}	CC	D	Internal resistance of analog source	—		—	—	2	kΩ
R_{AD}	CC	D	Internal resistance of analog source	—		—	—	0.3	kΩ
I_{INJ}	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V_{DD} = 3.3 V ± 10%	–5	—	5	mA
					V_{DD} = 5.0 V ± 10%	–5	—	5	
INLP	CC	T	Absolute Integral non-linearity-precise channels	No overload		—	1	3	LSB
INLX	CC	T	Absolute Integral non-linearity-extended channels	No overload		—	1.5	5	LSB
DNL	CC	T	Absolute Differential non-linearity	No overload		—	0.5	1	LSB
E_O	CC	T	Absolute Offset error	—		—	2	—	LSB
E_G	CC	T	Absolute Gain error	—		—	2	—	LSB
TUEP[7]	CC	P	Total unadjusted error for precise channels, input only pins	Without current injection		–6		6	LSB
		T		With current injection		–8		8	

Table 41. ADC conversion characteristics (continued)

Symbol		C	Parameter	Conditions[1]	Value			Unit
					Min	Typ	Max	
TUEX[7]	CC	T	Total unadjusted error for extended channel	Without current injection	–10		10	LSB
		T		With current injection	–12		12	

1 V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_A = –40 to 125 °C, unless otherwise specified.

2 Analog and digital V_{SS} **must** be common (to be tied together externally).

3 V_{AINx} may exceed V_{SS_ADC} and V_{DD_ADC} limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0xFFF.

4 Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

5 During the sampling time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sampling time t_S, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

6 This parameter does not include the sampling time t_S, but only the time for determining the digital result and the time to load the result's register with the conversion result.

7 Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

4.18 On-chip peripherals

4.18.1 Current consumption

Table 42. On-chip peripherals current consumption[1]

Symbol		C	Parameter	Conditions		Typical value[2]	Unit
$I_{DD\_BV(CAN)}$	CC	T	CAN (FlexCAN) supply current on V_{DD_BV}	500 Kbyte/s	Total (static + dynamic) consumption: • FlexCAN in loop-back mode • XTAL at 8 MHz used as CAN engine clock source • Message sending period is 580 µs	8 × f_{periph} + 85	µA
				125 Kbyte/s		8 × f_{periph} + 27	µA
$I_{DD\_BV(eMIOS)}$	CC	T	eMIOS supply current on V_{DD_BV}	Static consumption: • eMIOS channel OFF • Global prescaler enabled		29 × f_{periph}	µA
				Dynamic consumption: • It does not change varying the frequency (0.003 mA)		3	µA
$I_{DD\_BV(SCI)}$	CC	T	SCI (LINFlex) supply current on V_{DD_BV}	Total (static + dynamic) consumption: • LIN mode • Baudrate: 20 Kbyte/s		5 × f_{periph} + 31	µA

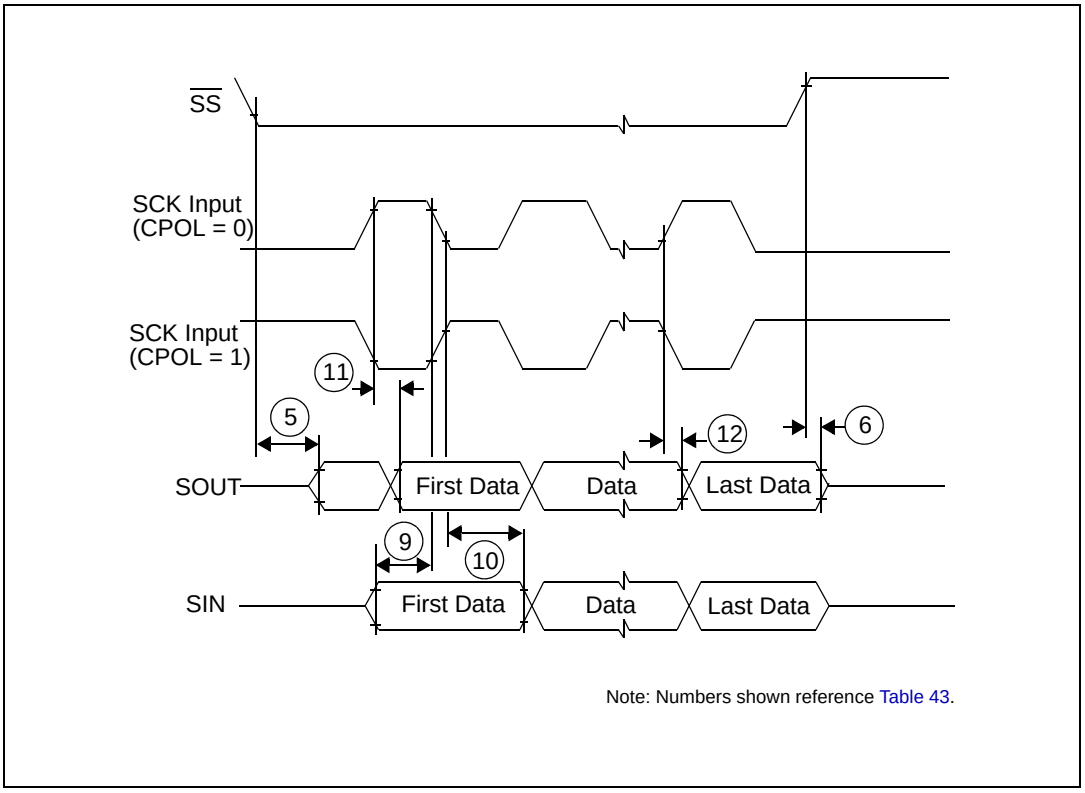

Figure 23. DSPI modified transfer format timing – slave, CPHA = 1

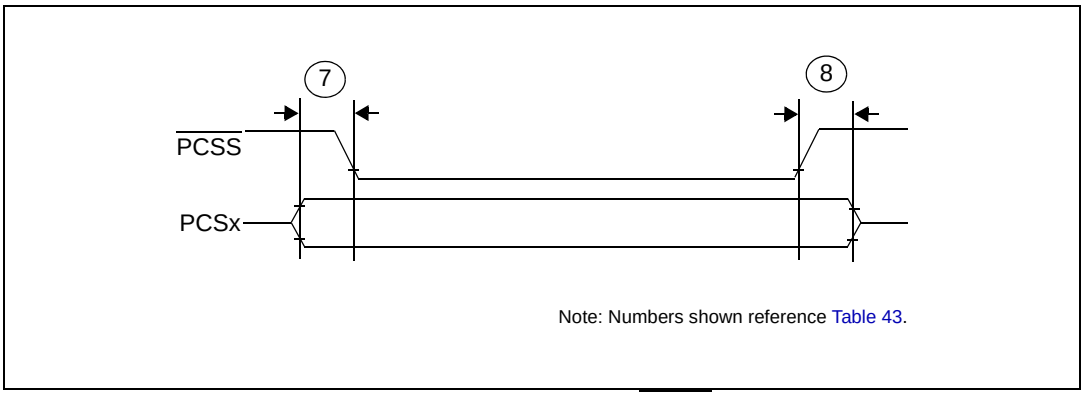

Figure 24. DSPI PCS strobe (PCSS) timing

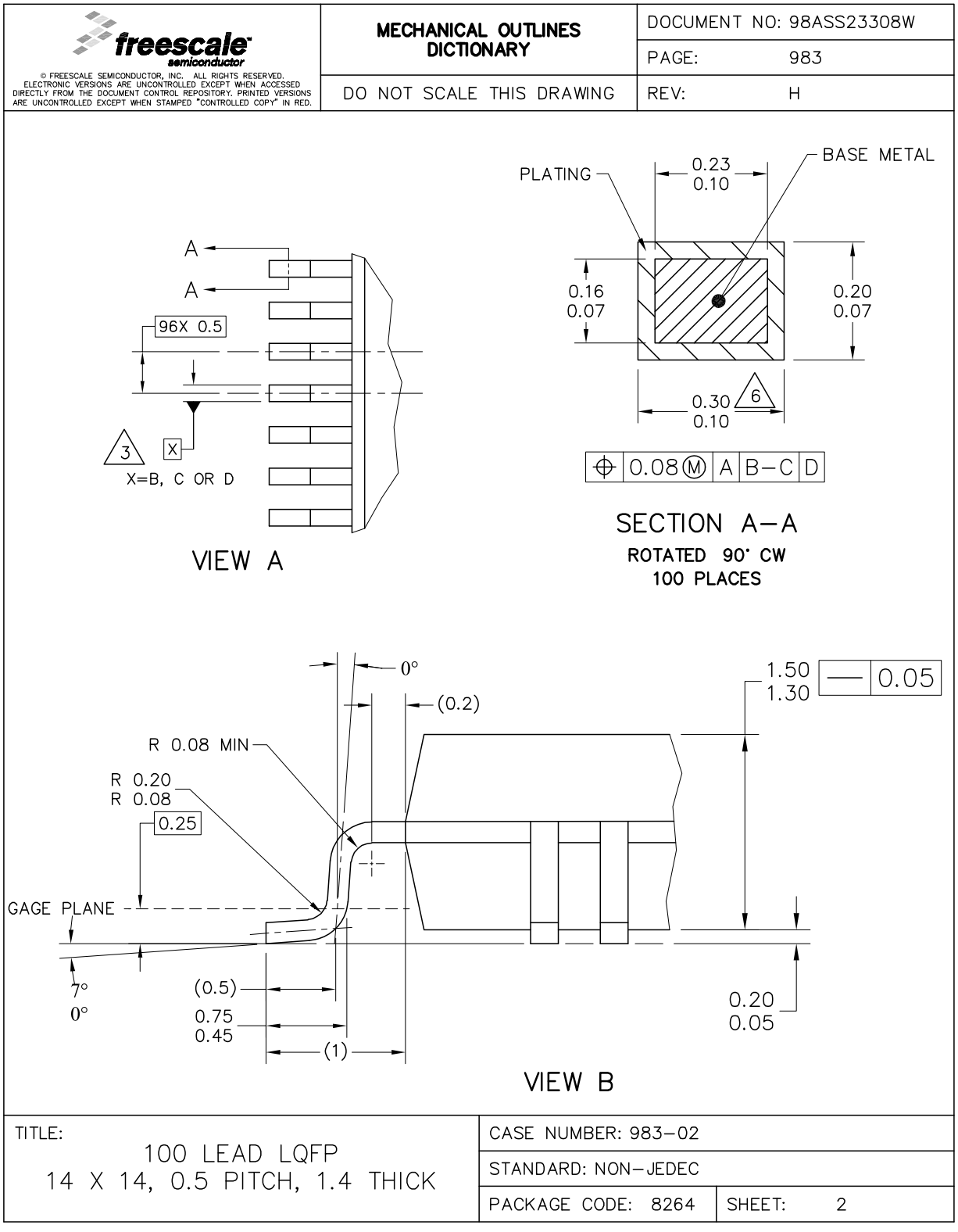

Figure 27. 100 LQFP package mechanical drawing (Part 2 of 3)

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23308W
		PAGE: 983
	DO NOT SCALE THIS DRAWING	REV: H

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.

5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	CASE NUMBER: 983–02	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 8264	SHEET: 3

Figure 28. 100 LQFP package mechanical drawing (Part 3 of 3)

Table 45. Revision history (continued)

Revision	Date	Description of Changes
3.1	23 Feb 2011	Deleted the “Freescale Confidential Proprietary” label (the document is public)

Table 45. Revision history (continued)

Revision	Date	Description of Changes
5	—	Rev. 5 not published.
6	29 Jan 2013	Removed all instances of table footnote “All values need to be confirmed during device validation” Section 4.1, “Introduction, removed Caution note. In Table 42, On-chip peripherals current consumption, replaced “TBD” with “8.21 mA” in $I_{DD\_HV(FLASH)}$ cell. Updated Section 4.17.2, “Input impedance and ADC accuracy In Table 24, changed $V_{LVDHV3L}$, $V_{LVDHV3BL}$ from 2.7 V to 2.6 V. Revised the Table 28 (Flash module life) Updated Table 43, DSPI characteristics, to add specifications 7 and 8, t_{PCSC} and t_{PASC}. Inserted Figure 24, DSPI PCS strobe (PCSS) timing.

Appendix A Abbreviations

Table A-1 lists abbreviations used in this document.

Table A-1. Abbreviations

Abbreviation	Meaning
APU	Auxilliary processing unit
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
DAOC	Double action output compare
ECC	Error code correction
EVTO	Event out
GPIO	General purpose input/output
IPM	Input period measurement
IPWM	Input pulse width measurement
MB	Message buffer
MC	Modulus counter
MCB	Modulus counter buffered (up / down)
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
NVUSRO	Non-volatile user options register
OPWFMB	Output pulse width and frequency modulation buffered
OPWMB	Output pulse width modulation buffered