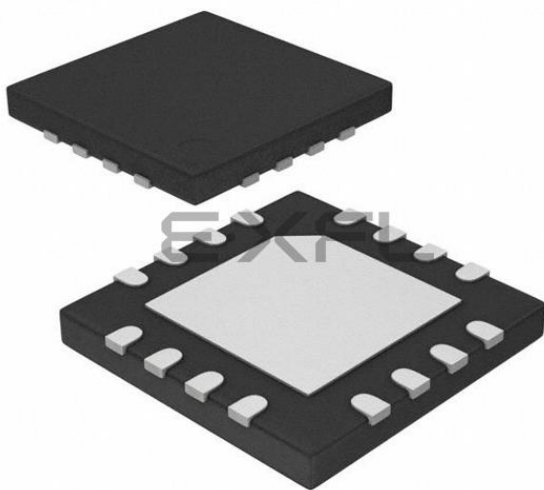




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                       |
|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                |
| Core Processor             | PIC                                                                                                                                                                   |
| Core Size                  | 8-Bit                                                                                                                                                                 |
| Speed                      | 32MHz                                                                                                                                                                 |
| Connectivity               | I <sup>2</sup> C, LINbus, SPI, UART/USART                                                                                                                             |
| Peripherals                | Brown-out Detect/Reset, POR, PWM, WDT                                                                                                                                 |
| Number of I/O              | 12                                                                                                                                                                    |
| Program Memory Size        | 7KB (4K x 14)                                                                                                                                                         |
| Program Memory Type        | FLASH                                                                                                                                                                 |
| EEPROM Size                | 256 x 8                                                                                                                                                               |
| RAM Size                   | 512 x 8                                                                                                                                                               |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V                                                                                                                                                           |
| Data Converters            | A/D 11x10b; D/A 1x5b                                                                                                                                                  |
| Oscillator Type            | Internal                                                                                                                                                              |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                     |
| Mounting Type              | Surface Mount                                                                                                                                                         |
| Package / Case             | 16-UQFN Exposed Pad                                                                                                                                                   |
| Supplier Device Package    | 16-UQFN (4x4)                                                                                                                                                         |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18324-i-jq">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf18324-i-jq</a> |

**TABLE 1: PIC16(L)F183XX Family Types**

| Device         | Data Sheet Index | Program Memory (KB) | Program Memory (KW) | EEPROM (B) | RAM (B) | I/Os <sup>(1)</sup> | 10-bit ADCs | Comparators | 5-bit DAC | Timers 0/1/2 | CCP/PWM | CWG | EUSART | SPI | I <sup>2</sup> C | CLC | NCO | PPS | ICD <sup>(2)</sup> |
|----------------|------------------|---------------------|---------------------|------------|---------|---------------------|-------------|-------------|-----------|--------------|---------|-----|--------|-----|------------------|-----|-----|-----|--------------------|
| PIC16(L)F18313 | (A)              | 3.5                 | 2                   | 256        | 256     | 6                   | 5           | 1           | 1         | 1/1/1        | 2/2     | 1   | 1      | 1   | 1                | 2   | 1   | Y   | I                  |
| PIC16(L)F18323 | (A)              | 3.5                 | 2                   | 256        | 256     | 12                  | 11          | 2           | 1         | 1/1/1        | 2/2     | 1   | 1      | 1   | 1                | 2   | 1   | Y   | I                  |
| PIC16(L)F18324 | (B)              | 7                   | 4                   | 256        | 512     | 12                  | 11          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 1   | 1                | 4   | 1   | Y   | I                  |
| PIC16(L)F18325 | (C)              | 14                  | 8                   | 256        | 1K      | 12                  | 11          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 2   | 2                | 4   | 1   | Y   | I                  |
| PIC16(L)F18326 | (D)              | 28                  | 16                  | 256        | 2K      | 12                  | 11          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 2   | 2                | 4   | 1   | Y   | I                  |
| PIC16(L)F18344 | (B)              | 7                   | 4                   | 256        | 512     | 18                  | 17          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 1   | 1                | 4   | 1   | Y   | I                  |
| PIC16(L)F18345 | (C)              | 14                  | 8                   | 256        | 1K      | 18                  | 17          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 2   | 2                | 4   | 1   | Y   | I                  |
| PIC16(L)F18346 | (D)              | 28                  | 16                  | 256        | 2K      | 18                  | 17          | 2           | 1         | 1/3/3        | 4/2     | 2   | 1      | 2   | 2                | 4   | 1   | Y   | I                  |

**Note 1:** One pin is input-only.**Note 2:** Debugging Methods: (I) – Integrated on Chip; E – using Emulation Header.**Data Sheet Index:** (Unshaded devices are described in this document.)

- A)** DS40001799 PIC16(L)F18313/18323 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP  
**B)** DS40001800 PIC16(L)F18324/18344 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP  
**C)** DS40001795 PIC16(L)F18325/18345 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP  
**D)** Future Release PIC16(L)F18326/18346 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F183XX

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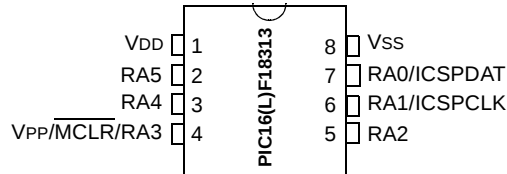
**TABLE 2: PACKAGES**

| Packages       | PDIP | SOIC | UDFN | TSSOP | UQFN | SSOP |
|----------------|------|------|------|-------|------|------|
| PIC16(L)F18313 | X    | X    | X    |       |      |      |
| PIC16(L)F18323 | X    | X    |      | X     | X    |      |
| PIC16(L)F18324 | X    | X    |      | X     | X    |      |
| PIC16(L)F18325 | X    | X    |      | X     | X    |      |
| PIC16(L)F18326 | X    | X    |      | X     | X    |      |
| PIC16(L)F18344 | X    | X    |      |       | X    | X    |
| PIC16(L)F18345 | X    | X    |      |       | X    | X    |
| PIC16(L)F18346 | X    | X    |      |       | X    | X    |

**Note:** Pin details are subject to change.

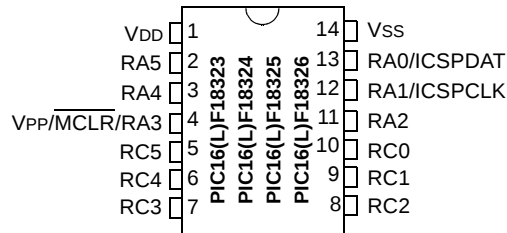
## PIN DIAGRAMS

### Pin Diagram – 8-Pin PDIP, SOIC, UDFN



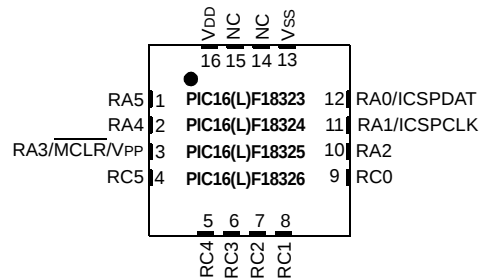
**Note:** See Table 3 for location of all peripheral functions.

### Pin Diagram – 14-Pin PDIP, SOIC, TSSOP



**Note:** See Table 4, Table 5, Table 6 and Table 7 for location of all peripheral functions.

### Pin Diagram – 16-Pin UQFN (4x4)

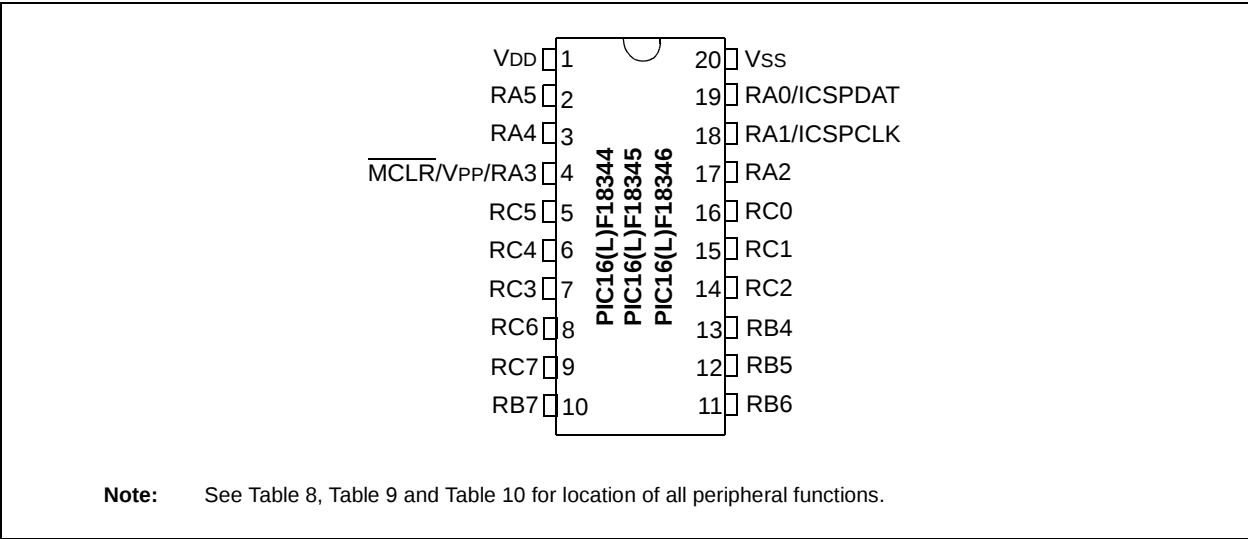


**Note 1:** See Table 4, Table 5, Table 6 and Table 7 for location of all peripheral functions.

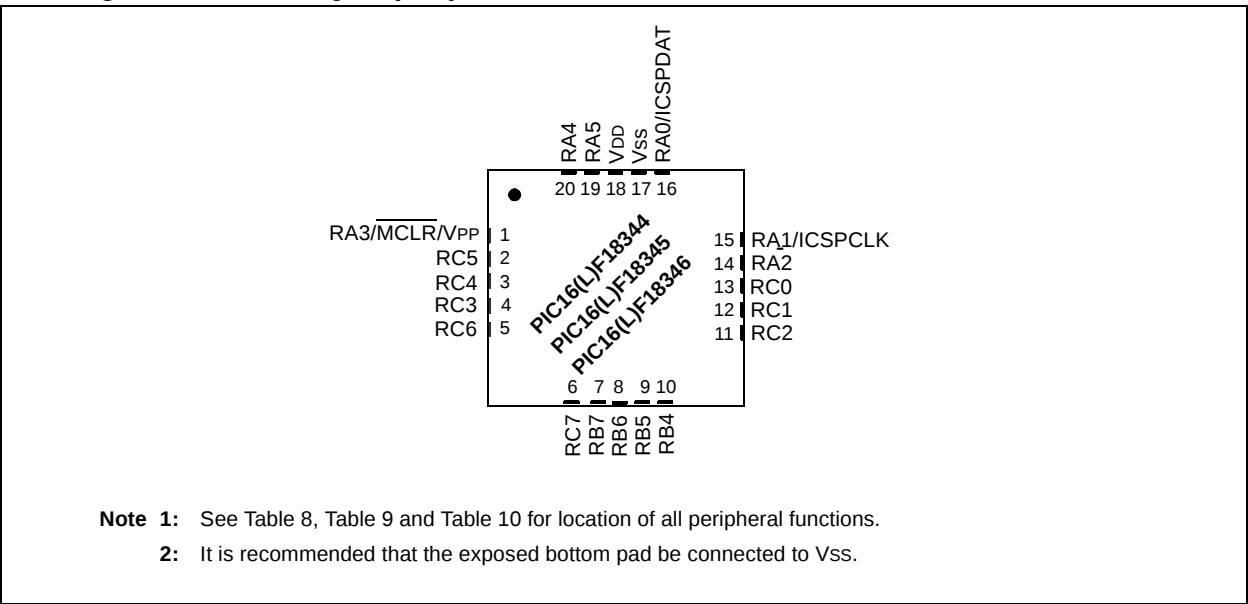
**Note 2:** It is recommended that the exposed bottom pad be connected to VSS.

# PIC16(L)F183XX

Pin Diagram – 20-Pin PDIP, SOIC, SSOP



Pin Diagram – 20-Pin UQFN (4x4)



## PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F18313)

| I/O <sup>(2)</sup> | 8-Pin PDIP/SOIC/UDFN | ADC  | Reference | Comparator | NCO | DAC      | DSM                   | Timers                                  | CCP                                        | PWM  | CWG                 | MSSP                                         | EUSART                                   | CLC                   | CLKR | Interrupt                   | Pull-up | Basic                   |
|--------------------|----------------------|------|-----------|------------|-----|----------|-----------------------|-----------------------------------------|--------------------------------------------|------|---------------------|----------------------------------------------|------------------------------------------|-----------------------|------|-----------------------------|---------|-------------------------|
| RA0                | 7                    | ANA0 | —         | C1IN0+     | —   | DAC1OUT  | MDCIN1 <sup>(1)</sup> | —                                       | —                                          | —    | —                   | —                                            | TX <sup>(1)</sup><br>CK <sup>(1)</sup>   | CLCIN3 <sup>(1)</sup> | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT      |
| RA1                | 6                    | ANA1 | VREF+     | C1IN0-     | —   | DAC1REF+ | MDMIN <sup>(1)</sup>  | —                                       | —                                          | —    | —                   | SCK <sup>(1)</sup><br>SCL <sup>(1,3,4)</sup> | RX <sup>(1)</sup><br>DT <sup>(1,3)</sup> | CLCIN2 <sup>(1)</sup> | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK      |
| RA2                | 5                    | ANA2 | VREF-     | —          | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                    | —                                          | —    | CWG1 <sup>(1)</sup> | SDA <sup>(1,3,4)</sup><br>SDO <sup>(1)</sup> | —                                        | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                       |
| RA3                | 4                    | —    | —         | —          | —   | —        | —                     | —                                       | —                                          | —    | —                   | SS <sup>(4)</sup>                            | —                                        | CLCIN0 <sup>(1)</sup> | —    | IOCA3                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4                | 3                    | ANA4 | —         | C1IN1-     | —   | —        | —                     | T1G <sup>(1)</sup><br>SOSCO             | —                                          | —    | —                   | —                                            | —                                        | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2          |
| RA5                | 2                    | ANA5 | —         | —          | —   | —        | MDCIN2 <sup>(1)</sup> | T1CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | CCP1 <sup>(1)</sup><br>CCP2 <sup>(1)</sup> | —    | —                   | —                                            | —                                        | CLCIN1 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1           |
| V <sub>DD</sub>    | 1                    | —    | —         | —          | —   | —        | —                     | —                                       | —                                          | —    | —                   | —                                            | —                                        | —                     | —    | —                           | —       | V <sub>DD</sub>         |
| V <sub>SS</sub>    | 8                    | —    | —         | —          | —   | —        | —                     | —                                       | —                                          | —    | —                   | —                                            | —                                        | —                     | —    | —                           | —       | V <sub>SS</sub>         |
| OUT <sup>(2)</sup> | —                    | —    | —         | C1OUT      | NCO | —        | DSM                   | TMR0                                    | CCP1                                       | PWM5 | CWG1A               | SDA <sup>(3)</sup>                           | CK                                       | CLC1OUT               | CLKR | —                           | —       | —                       |
|                    | —                    | —    | —         | —          | —   | —        | —                     | —                                       | CCP2                                       | PWM6 | CWG1B               | SCL <sup>(3)</sup>                           | DT <sup>(3)</sup>                        | CLC2OUT               | —    | —                           | —       | —                       |
|                    | —                    | —    | —         | —          | —   | —        | —                     | —                                       | —                                          | —    | CWG1C               | SDO                                          | TX                                       | —                     | —    | —                           | —       | —                       |
|                    | —                    | —    | —         | —          | —   | —        | —                     | —                                       | —                                          | —    | CWG1D               | SCK                                          | —                                        | —                     | —    | —                           | —       | —                       |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                  | CCP                 | PWM | CWG                 | MSSP                                         | EUSART                                   | CLC                   | CLKR | Interrupt                   | Pull-up | Basic              |
|--------------------|---------------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------|---------------------|-----|---------------------|----------------------------------------------|------------------------------------------|-----------------------|------|-----------------------------|---------|--------------------|
| RA0                | 13                        | 12          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT |
| RA1                | 12                        | 11          | ANA1 | VREF+     | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK |
| RA2                | 11                        | 10          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                    | —                   | —   | CWG1 <sup>(1)</sup> | —                                            | —                                        | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                  |
| RA3                | 4                         | 3           | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | IOCA3                       | Y       | MCLR<br>VPP        |
| RA4                | 3                         | 2           | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>SOSCO             | —                   | —   | —                   | —                                            | —                                        | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2     |
| RA5                | 2                         | 1           | ANA5 | —         | —                | —   | —        | —                     | T1CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                   | —                                            | —                                        | CLCIN3 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1      |
| RC0                | 10                        | 9           | ANC0 | —         | C2IN0+           | —   | —        | —                     | —                                       | —                   | —   | —                   | SCK <sup>(1)</sup><br>SCL <sup>(1,3,4)</sup> | —                                        | —                     | —    | IOCC0                       | Y       | —                  |
| RC1                | 9                         | 8           | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                       | —                   | —   | —                   | SDI <sup>(1)</sup><br>SDA <sup>(1,3,4)</sup> | —                                        | CLCIN2 <sup>(1)</sup> | —    | IOCC1                       | Y       | —                  |
| RC2                | 8                         | 7           | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | IOCC2                       | Y       | —                  |
| RC3                | 7                         | 6           | ANC3 | —         | C1IN3-<br>C2IN3- | —   | —        | MDMIN <sup>(1)</sup>  | —                                       | CCP2 <sup>(1)</sup> | —   | —                   | SS <sup>(1)</sup>                            | —                                        | CLCIN0 <sup>(1)</sup> | —    | IOCC3                       | Y       | —                  |
| RC4                | 6                         | 5           | ANC4 | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                   | —                                            | TX <sup>(1)</sup><br>CK <sup>(1)</sup>   | CLCIN1 <sup>(1)</sup> | —    | IOCC4                       | Y       | —                  |
| RC5                | 5                         | 4           | ANC5 | —         | —                | —   | —        | MDCIN2 <sup>(1)</sup> | —                                       | CCP1 <sup>(1)</sup> | —   | —                   | —                                            | RX <sup>(1)</sup><br>DT <sup>(1,3)</sup> | —                     | —    | IOCC5                       | Y       | —                  |
| VDD                | 1                         | 16          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | —                           | —       | VDD                |
| VSS                | 14                        | 13          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                   | —                                            | —                                        | —                     | —    | —                           | —       | VSS                |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323) (CONTINUED)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | DSM | Timers | CCP  | PWM  | CWG   | MSSP               | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|---------------------------|-------------|-----|-----------|------------|-----|-----|-----|--------|------|------|-------|--------------------|-------------------|---------|------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —                         | —           | —   | —         | C1OUT      | NCO | —   | DSM | TMR0   | CCP1 | PWM5 | CWG1A | SDA <sup>(3)</sup> | CK                | CLC1OUT | CLKR | —         | —       | —     |
|                    | —                         | —           | —   | —         | C2OUT      | —   | —   | —   | —      | CCP2 | PWM6 | CWG1B | SCL <sup>(3)</sup> | DT <sup>(3)</sup> | CLC2OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | —    | —    | CWG1C | SDO                | TX                | —       | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | —    | —    | CWG1D | SCK                | —                 | —       | —    | —         | —       | —     |

- Note**
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  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                  | CCP                 | PWM | CWG                                        | MSSP                                         | EUSART                                   | CLC                   | CLKR | Interrupt                   | Pull-up | Basic                   |
|--------------------|---------------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------|---------------------|-----|--------------------------------------------|----------------------------------------------|------------------------------------------|-----------------------|------|-----------------------------|---------|-------------------------|
| RA0                | 13                        | 12          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT      |
| RA1                | 12                        | 11          | ANA1 | VREF+     | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK      |
| RA2                | 11                        | 10          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                            | —                                        | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                       |
| RA3                | 4                         | 3           | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | IOCA3                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4                | 3                         | 2           | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(4)</sup><br>SOSCO             | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2          |
| RA5                | 2                         | 1           | ANA5 | —         | —                | —   | —        | —                     | T1CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                            | —                                        | CLCIN3 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1           |
| RC0                | 10                        | 9           | ANC0 | —         | C2IN0+           | —   | —        | —                     | T5CKI <sup>(1)</sup>                    | —                   | —   | —                                          | SCK <sup>(1)</sup><br>SCL <sup>(1,3,4)</sup> | —                                        | —                     | —    | IOCC0                       | Y       | —                       |
| RC1                | 9                         | 8           | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | CCP4 <sup>(1)</sup>                     | —                   | —   | —                                          | SDI <sup>(1)</sup><br>SDA <sup>(1,3,4)</sup> | —                                        | CLCIN2 <sup>(1)</sup> | —    | IOCC1                       | Y       | —                       |
| RC2                | 8                         | 7           | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | IOCC2                       | Y       | —                       |
| RC3                | 7                         | 6           | ANC3 | —         | C1IN3-<br>C2IN3- | —   | —        | MDMIN <sup>(1)</sup>  | T5G <sup>(1)</sup>                      | CCP2 <sup>(1)</sup> | —   | —                                          | SS <sup>(1)</sup>                            | —                                        | CLCIN0 <sup>(1)</sup> | —    | IOCC3                       | Y       | —                       |
| RC4                | 6                         | 5           | ANC4 | —         | —                | —   | —        | —                     | T3G <sup>(1)</sup>                      | —                   | —   | —                                          | —                                            | TX <sup>(1)</sup><br>CK <sup>(1)</sup>   | CLCIN1 <sup>(1)</sup> | —    | IOCC4                       | Y       | —                       |
| RC5                | 5                         | 4           | ANC5 | —         | —                | —   | —        | MDCIN2 <sup>(1)</sup> | T3CKI <sup>(1)</sup>                    | CCP1 <sup>(1)</sup> | —   | —                                          | —                                            | RX <sup>(1)</sup><br>DT <sup>(1,3)</sup> | —                     | —    | IOCC5                       | Y       | —                       |
| V <sub>DD</sub>    | 1                         | 16          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | —                           | —       | V <sub>DD</sub>         |
| V <sub>SS</sub>    | 14                        | 13          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                            | —                                        | —                     | —    | —                           | —       | V <sub>SS</sub>         |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | DSM | Timers | CCP  | PWM  | CWG            | MSSP               | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|---------------------------|-------------|-----|-----------|------------|-----|-----|-----|--------|------|------|----------------|--------------------|-------------------|---------|------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —                         | —           | —   | —         | C1OUT      | NCO | —   | DSM | TMR0   | CCP1 | PWM5 | CWG1A<br>CWG2A | SDA <sup>(3)</sup> | CK                | CLC1OUT | CLKR | —         | —       | —     |
|                    | —                         | —           | —   | —         | C2OUT      | —   | —   | —   | —      | CCP2 | PWM6 | CWG1B<br>CWG2B | SCL <sup>(3)</sup> | DT <sup>(3)</sup> | CLC2OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP3 | —    | CWG1C<br>CWG2C | SDO                | TX                | CLC3OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP4 | —    | CWG1D<br>CWG2D | SCK                | —                 | CLC4OUT | —    | —         | —       | —     |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325)

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                  | CCP                 | PWM | CWG                                        | MSSP                                           | EUSART                                   | CLC                   | CLKR | Interrupt                   | Pull-up | Basic                   |
|--------------------|---------------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------|---------------------|-----|--------------------------------------------|------------------------------------------------|------------------------------------------|-----------------------|------|-----------------------------|---------|-------------------------|
| RA0                | 13                        | 12          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                       | —                   | —   | —                                          | SS2 <sup>(1)</sup>                             | —                                        | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT      |
| RA1                | 12                        | 11          | ANA1 | VREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK      |
| RA2                | 11                        | 10          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                              | —                                        | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                       |
| RA3                | 4                         | 3           | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA3                       | Y       | MCLR<br>V <sub>PP</sub> |
| RA4                | 3                         | 2           | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>SOSCO             | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2          |
| RA5                | 2                         | 1           | ANA5 | —         | —                | —   | —        | —                     | T1CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                              | —                                        | CLCIN3 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1           |
| RC0                | 10                        | 9           | ANC0 | —         | C2IN0+           | —   | —        | —                     | T5CKI <sup>(1)</sup>                    | —                   | —   | —                                          | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup> | —                                        | —                     | —    | IOCC0                       | Y       | —                       |
| RC1                | 9                         | 8           | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                       | CCP4 <sup>(1)</sup> | —   | —                                          | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup> | —                                        | CLCIN2 <sup>(1)</sup> | —    | IOCC1                       | Y       | —                       |
| RC2                | 8                         | 7           | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCC2                       | Y       | —                       |
| RC3                | 7                         | 6           | ANC3 | —         | C1IN3-<br>C2IN3- | —   | —        | MDMIN <sup>(1)</sup>  | T5G <sup>(1)</sup>                      | CCP2 <sup>(1)</sup> | —   | —                                          | SS1 <sup>(1)</sup>                             | —                                        | CLCIN0 <sup>(1)</sup> | —    | IOCC3                       | Y       | —                       |
| RC4                | 6                         | 5           | ANC4 | —         | —                | —   | —        | —                     | T3G <sup>(1)</sup>                      | —                   | —   | —                                          | SCK2 <sup>(1)</sup><br>SCL2 <sup>(1,3,4)</sup> | TX <sup>(1)</sup><br>CK <sup>(1)</sup>   | CLCIN1 <sup>(1)</sup> | —    | IOCC4                       | Y       | —                       |
| RC5                | 5                         | 4           | ANC5 | —         | —                | —   | —        | MDCIN2 <sup>(1)</sup> | T3CKI <sup>(1)</sup>                    | CCP1 <sup>(1)</sup> | —   | —                                          | SDI2 <sup>(1)</sup><br>SDA2 <sup>(1,3,4)</sup> | RX <sup>(1)</sup><br>DT <sup>(1,3)</sup> | —                     | —    | IOCC5                       | Y       | —                       |
| VDD                | 1                         | 16          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | —                           | —       | VDD                     |
| VSS                | 14                        | 13          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | —                           | —       | VSS                     |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325) (CONTINUED)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | DSM | Timers | CCP  | PWM  | CWG            | MSSP                                       | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|---------------------------|-------------|-----|-----------|------------|-----|-----|-----|--------|------|------|----------------|--------------------------------------------|-------------------|---------|------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —                         | —           | —   | —         | C1OUT      | DDS | —   | DSM | TMR0   | CCP1 | PWM5 | CWG1A<br>CWG2A | SDA1 <sup>(3)</sup><br>SDA2 <sup>(3)</sup> | CK                | CLC1OUT | CLKR | —         | —       | —     |
|                    | —                         | —           | —   | —         | C2OUT      | —   | —   | —   | —      | CCP2 | PWM6 | CWG1B<br>CWG2B | SCL1 <sup>(3)</sup><br>SCL2 <sup>(3)</sup> | DT <sup>(3)</sup> | CLC2OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP3 | —    | CWG1C<br>CWG2C | SDO1<br>SDO2                               | TX                | CLC3OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP4 | —    | CWG1D<br>CWG2D | SCK1<br>SCK2                               | —                 | CLC4OUT | —    | —         | —       | —     |

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- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326)

| (2) I/O | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                  | CCP                 | PWM | CWG                                        | MSSP                                           | EUSART                                   | CLC                   | CLKR | Interrupt                   | Pull-up | Basic              |
|---------|---------------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------|---------------------|-----|--------------------------------------------|------------------------------------------------|------------------------------------------|-----------------------|------|-----------------------------|---------|--------------------|
| RA0     | 13                        | 12          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                       | —                   | —   | —                                          | SS2 <sup>(1)</sup>                             | —                                        | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT |
| RA1     | 12                        | 11          | ANA1 | VREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK |
| RA2     | 11                        | 10          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CK1 <sup>(1)</sup>                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                              | —                                        | —                     | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                  |
| RA3     | 4                         | 3           | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA3                       | Y       | MCLR<br>VPP        |
| RA4     | 3                         | 2           | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>SOSCO             | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2     |
| RA5     | 2                         | 1           | ANA5 | —         | —                | —   | —        | —                     | T1CK1 <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                              | —                                        | CLCIN3 <sup>(1)</sup> | —    | IOCA5                       | Y       | CLKIN<br>OSC1      |
| RC0     | 10                        | 9           | ANC0 | —         | C2IN0+           | —   | —        | —                     | T5CK1 <sup>(1)</sup>                    | —                   | —   | —                                          | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup> | —                                        | —                     | —    | IOCC0                       | Y       | —                  |
| RC1     | 9                         | 8           | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                       | CCP4 <sup>(1)</sup> | —   | —                                          | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup> | —                                        | CLCIN2 <sup>(1)</sup> | —    | IOCC1                       | Y       | —                  |
| RC2     | 8                         | 7           | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | IOCC2                       | Y       | —                  |
| RC3     | 7                         | 6           | ANC3 | —         | C1IN3-<br>C2IN3- | —   | —        | MDMIN <sup>(1)</sup>  | T5G <sup>(1)</sup>                      | CCP2 <sup>(1)</sup> | —   | —                                          | SS1 <sup>(1)</sup>                             | —                                        | CLCIN0 <sup>(1)</sup> | —    | IOCC3                       | Y       | —                  |
| RC4     | 6                         | 5           | ANC4 | —         | —                | —   | —        | —                     | T3G <sup>(1)</sup>                      | —                   | —   | —                                          | SCK2 <sup>(1)</sup><br>SCL2 <sup>(1,3,4)</sup> | TX <sup>(1)</sup><br>CK <sup>(1)</sup>   | CLCIN1 <sup>(1)</sup> | —    | IOCC4                       | Y       | —                  |
| RC5     | 5                         | 4           | ANC5 | —         | —                | —   | —        | MDCIN2 <sup>(1)</sup> | T3CK1 <sup>(1)</sup>                    | CCP1 <sup>(1)</sup> | —   | —                                          | SDI2 <sup>(1)</sup><br>SDA2 <sup>(1,3,4)</sup> | RX <sup>(1)</sup><br>DT <sup>(1,3)</sup> | —                     | —    | IOCC5                       | Y       | —                  |
| VDD     | 1                         | 16          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | —                           | —       | VDD                |
| VSS     | 14                        | 13          | —    | —         | —                | —   | —        | —                     | —                                       | —                   | —   | —                                          | —                                              | —                                        | —                     | —    | —                           | —       | VSS                |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
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**TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326) (CONTINUED)**

| I/O <sup>(2)</sup> | 14/16-Pin PDIP/SOIC/TSSOP | 16-Pin UQFN | ADC | Reference | Comparator | NCO | DAC | DSM | Timers | CCP  | PWM  | CWG            | MSSP                                       | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|---------------------------|-------------|-----|-----------|------------|-----|-----|-----|--------|------|------|----------------|--------------------------------------------|-------------------|---------|------|-----------|---------|-------|
| OUT <sup>(2)</sup> | —                         | —           | —   | —         | C1OUT      | DDS | —   | DSM | TMR0   | CCP1 | PWM5 | CWG1A<br>CWG2A | SDA1 <sup>(3)</sup><br>SDA2 <sup>(3)</sup> | CK                | CLC1OUT | CLKR | —         | —       | —     |
|                    | —                         | —           | —   | —         | C2OUT      | —   | —   | —   | —      | CCP2 | PWM6 | CWG1B<br>CWG2B | SCL1 <sup>(3)</sup><br>SCL2 <sup>(3)</sup> | DT <sup>(3)</sup> | CLC2OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP3 | —    | CWG1C<br>CWG2C | SDO1<br>SDO2                               | TX                | CLC3OUT | —    | —         | —       | —     |
|                    | —                         | —           | —   | —         | —          | —   | —   | —   | —      | CCP4 | —    | CWG1D<br>CWG2D | SCK1<br>SCK2                               | —                 | CLC4OUT | —    | —         | —       | —     |

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**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)**

| I/O <sup>(2)</sup> | 20-Pin PDIP/SOIC/SSOP | 20-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                                                                  | CCP                 | PWM | CWG                                        | MSSP                                         | EUSART                                 | CLC                   | CLKR | Interrupt                   | Pull-up | Basic              |
|--------------------|-----------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------------------------------------------------------|---------------------|-----|--------------------------------------------|----------------------------------------------|----------------------------------------|-----------------------|------|-----------------------------|---------|--------------------|
| RA0                | 19                    | 16          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT |
| RA1                | 18                    | 15          | ANA1 | VREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK |
| RA2                | 17                    | 14          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                                                                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                            | —                                      | CLCIN0 <sup>(1)</sup> | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                  |
| RA3                | 4                     | 1           | —    | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCA3                       | Y       | MCLR<br>VPP        |
| RA4                | 3                     | 20          | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>T3G <sup>(1)</sup><br>T5G <sup>(1)</sup><br>SOSCO                 | CCP4 <sup>(1)</sup> | —   | —                                          | —                                            | —                                      | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2     |
| RA5                | 2                     | 19          | ANA5 | —         | —                | —   | —        | —                     | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T5CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCA5                       | Y       | CLKIN<br>OSC1      |
| RB4                | 13                    | 10          | ANB4 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SDI <sup>(1)</sup><br>SDA <sup>(1,3,4)</sup> | —                                      | CLCIN2 <sup>(1)</sup> | —    | IOCB4                       | Y       | —                  |
| RB5                | 12                    | 9           | ANB5 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | RX <sup>(1)</sup><br>DT <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB5                       | Y       | —                  |
| RB6                | 11                    | 8           | ANB6 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SCK <sup>(1)</sup><br>SCL <sup>(1,3,4)</sup> | —                                      | —                     | —    | IOCB6                       | Y       | —                  |
| RB7                | 10                    | 7           | ANB7 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | TX <sup>(1)</sup><br>CK <sup>(1)</sup> | —                     | —    | IOCB7                       | Y       | —                  |
| RC0                | 16                    | 13          | ANC0 | —         | C2IN0+           | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCC0                       | Y       | —                  |
| RC1                | 15                    | 12          | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCC1                       | Y       | —                  |
| RC2                | 14                    | 11          | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                                                                       | —                   | —   | —                                          | —                                            | —                                      | —                     | —    | IOCC2                       | Y       | —                  |

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  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (CONTINUED)**

| I/O <sup>(2)</sup> | 20-Pin PDI/SS/CI/IO/SDI/SDO | 20-Pin UQFN | ADC  | Reference | Comparator   | NCO | DAC | DSM                   | Timers | CCP                 | PWM  | CWG            | MSSP               | EUSART            | CLC                   | CLKR | Interrupt | Pull-up | Basic |
|--------------------|-----------------------------|-------------|------|-----------|--------------|-----|-----|-----------------------|--------|---------------------|------|----------------|--------------------|-------------------|-----------------------|------|-----------|---------|-------|
| RC3                | 7                           | 4           | ANC3 | —         | C1IN3-C2IN3- | —   | —   | MDMIN <sup>(1)</sup>  | —      | CCP2 <sup>(1)</sup> | —    | —              | —                  | —                 | CLCIN1 <sup>(1)</sup> | —    | IOCC3     | Y       | —     |
| RC4                | 6                           | 3           | ANC4 | —         | —            | —   | —   | —                     | —      | —                   | —    | —              | —                  | —                 | —                     | —    | IOCC4     | Y       | —     |
| RC5                | 5                           | 2           | ANC5 | —         | —            | —   | —   | MDCIN2 <sup>(1)</sup> | —      | CCP1 <sup>(1)</sup> | —    | —              | —                  | —                 | —                     | —    | IOCC5     | Y       | —     |
| RC6                | 8                           | 5           | ANC6 | —         | —            | —   | —   | —                     | —      | —                   | —    | —              | SS <sup>(1)</sup>  | —                 | —                     | —    | IOCC6     | Y       | —     |
| RC7                | 9                           | 6           | ANC7 | —         | —            | —   | —   | —                     | —      | —                   | —    | —              | —                  | —                 | —                     | —    | IOCC7     | Y       | —     |
| VDD                | 1                           | 18          | —    | —         | —            | —   | —   | —                     | —      | —                   | —    | —              | —                  | —                 | —                     | —    | —         | —       | VDD   |
| VSS                | 20                          | 17          | —    | —         | —            | —   | —   | —                     | —      | —                   | —    | —              | —                  | —                 | —                     | —    | —         | —       | VSS   |
| OUT <sup>(2)</sup> | —                           | —           | —    | —         | C1OUT        | NCO | —   | DSM                   | TMR0   | CCP1                | PWM5 | CWG1A<br>CWG2A | SDO                | DT <sup>(3)</sup> | CLC1OUT               | CLKR | —         | —       | —     |
|                    | —                           | —           | —    | —         | C2OUT        | —   | —   | —                     | —      | CCP2                | PWM6 | CWG1B<br>CWG2B | SCK                | CK                | CLC2OUT               | —    | —         | —       | —     |
|                    | —                           | —           | —    | —         | —            | —   | —   | —                     | —      | CCP3                | —    | CWG1C<br>CWG2C | SCL <sup>(3)</sup> | TX                | CLC3OUT               | —    | —         | —       | —     |
|                    | —                           | —           | —    | —         | —            | —   | —   | —                     | —      | CCP4                | —    | CWG1D<br>CWG2D | SDA <sup>(3)</sup> | —                 | CLC4OUT               | —    | —         | —       | —     |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

**TABLE 9: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)**

| I/O <sup>(2)</sup> | 20-Pin PDIP/28-Pin UQFN | 20-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                                                                  | CCP                 | PWM | CWG                                        | MSSP                                           | EUSART                                 | CLC                   | CLKR | Interrupt                   | Pull-up | Basic              |
|--------------------|-------------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------------------------------------------------------|---------------------|-----|--------------------------------------------|------------------------------------------------|----------------------------------------|-----------------------|------|-----------------------------|---------|--------------------|
| RA0                | 19                      | 16          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT |
| RA1                | 18                      | 15          | ANA1 | VREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                                                                       | —                   | —   | —                                          | SS2 <sup>(1)</sup>                             | —                                      | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK |
| RA2                | 17                      | 14          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CKI <sup>(1)</sup>                                                                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                              | —                                      | CLCIN0 <sup>(1)</sup> | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                  |
| RA3                | 4                       | 1           | —    | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA3                       | Y       | MCLR<br>VPP        |
| RA4                | 3                       | 20          | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>T3G <sup>(1)</sup><br>T5G <sup>(1)</sup><br>SOSCO                 | CCP4 <sup>(1)</sup> | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2     |
| RA5                | 2                       | 19          | ANA5 | —         | —                | —   | —        | —                     | T1CKI <sup>(1)</sup><br>T3CKI <sup>(1)</sup><br>T5CKI <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA5                       | Y       | CLKIN<br>OSC1      |
| RB4                | 13                      | 10          | ANB4 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup> | —                                      | CLCIN2 <sup>(1)</sup> | —    | IOCB4                       | Y       | —                  |
| RB5                | 12                      | 9           | ANB5 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SDI2 <sup>(1)</sup><br>SDA2 <sup>(1,3,4)</sup> | RX <sup>(1)</sup><br>DT <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB5                       | Y       | —                  |
| RB6                | 11                      | 8           | ANB6 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup> | —                                      | —                     | —    | IOCB6                       | Y       | —                  |
| RB7                | 10                      | 7           | ANB7 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SCK2 <sup>(1)</sup><br>SCL2 <sup>(1,3,4)</sup> | TX <sup>(1)</sup><br>CK <sup>(1)</sup> | —                     | —    | IOCB7                       | Y       | —                  |
| RC0                | 16                      | 13          | ANC0 | —         | C2IN0+           | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC0                       | Y       | —                  |
| RC1                | 15                      | 12          | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC1                       | Y       | —                  |
| RC2                | 14                      | 11          | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC2                       | Y       | —                  |
| RC3                | 7                       | 4           | ANC3 | —         | C1IN3-<br>C2IN3- | —   | —        | MDMIN <sup>(1)</sup>  | —                                                                                       | CCP2 <sup>(1)</sup> | —   | —                                          | —                                              | —                                      | CLCIN1 <sup>(1)</sup> | —    | IOCC3                       | Y       | —                  |

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
  - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
  - 4: These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register.

| I/O <sup>(2)</sup> | 20-Pin PDIP/SOIC/SSOP | 20-Pin UQFN | ADC  | Reference | Comparator | NCO | DAC | DSM                   | Timers | CCP                 | PWM  | CWG            | MSSP                                       | EUSART            | CLC     | CLKR | Interrupt | Pull-up | Basic |
|--------------------|-----------------------|-------------|------|-----------|------------|-----|-----|-----------------------|--------|---------------------|------|----------------|--------------------------------------------|-------------------|---------|------|-----------|---------|-------|
| RC4                | 6                     | 3           | ANC4 | —         | —          | —   | —   | —                     | —      | —                   | —    | —              | —                                          | —                 | —       | —    | IOCC4     | Y       | —     |
| RC5                | 5                     | 2           | ANC5 | —         | —          | —   | —   | MDCIN2 <sup>(1)</sup> | —      | CCP1 <sup>(1)</sup> | —    | —              | —                                          | —                 | —       | —    | IOCC5     | Y       | —     |
| RC6                | 8                     | 5           | ANC6 | —         | —          | —   | —   | —                     | —      | —                   | —    | —              | SS <sup>(1)</sup>                          | —                 | —       | —    | IOCC6     | Y       | —     |
| RC7                | 9                     | 6           | ANC7 | —         | —          | —   | —   | —                     | —      | —                   | —    | —              | —                                          | —                 | —       | —    | IOCC7     | Y       | —     |
| VDD                | 1                     | 18          | —    | —         | —          | —   | —   | —                     | —      | —                   | —    | —              | —                                          | —                 | —       | —    | —         | —       | VDD   |
| VSS                | 20                    | 17          | —    | —         | —          | —   | —   | —                     | —      | —                   | —    | —              | —                                          | —                 | —       | —    | —         | —       | VSS   |
| OUT <sup>(2)</sup> | —                     | —           | —    | —         | C1OUT      | NCO | —   | DSM                   | TMR0   | CCP1                | PWM5 | CWG1A<br>CWG2A | SDO1<br>SDO2                               | DT <sup>(3)</sup> | CLC1OUT | CLKR | —         | —       | —     |
|                    | —                     | —           | —    | —         | C2OUT      | —   | —   | —                     | —      | CCP2                | PWM6 | CWG1B<br>CWG2B | SCK1<br>SCK2                               | CK                | CLC2OUT | —    | —         | —       | —     |
|                    | —                     | —           | —    | —         | —          | —   | —   | —                     | —      | CCP3                | —    | CWG1C<br>CWG2C | SCL1 <sup>(3)</sup><br>SCL2 <sup>(3)</sup> | TX                | CLC3OUT | —    | —         | —       | —     |
|                    | —                     | —           | —    | —         | —          | —   | —   | —                     | —      | CCP4                | —    | CWG1D<br>CWG2D | SDA1 <sup>(3)</sup><br>SDA2 <sup>(3)</sup> | —                 | CLC4OUT | —    | —         | —       | —     |

- |             |           |                                                                                                                                                                                                                                                           |
|-------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Note</b> | <b>1:</b> | Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.                                                                                                                                                     |
|             | <b>2:</b> | All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.                                                                                                               |
|             | <b>3:</b> | These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.                                                                                                                                     |
|             | <b>4:</b> | These pins are configured for I <sup>2</sup> C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but logic levels will be standard TTL/ST as selected by the INLVL register. |

**TABLE 10: 20-PIN ALLOCATION TABLE (PIC16(L)F18346)**

| I/O <sup>(2)</sup> | 20-Pin PDIP/SOIC/SSOP | 20-Pin UQFN | ADC  | Reference | Comparator       | NCO | DAC      | DSM                   | Timers                                                                                  | CCP                 | PWM | CWG                                        | MSSP                                           | EUSART                                 | CLC                   | CLKR | Interrupt                   | Pull-up | Basic              |
|--------------------|-----------------------|-------------|------|-----------|------------------|-----|----------|-----------------------|-----------------------------------------------------------------------------------------|---------------------|-----|--------------------------------------------|------------------------------------------------|----------------------------------------|-----------------------|------|-----------------------------|---------|--------------------|
| RA0                | 19                    | 16          | ANA0 | —         | C1IN0+           | —   | DAC1OUT  | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA0                       | Y       | ICDDAT/<br>ICSPDAT |
| RA1                | 18                    | 15          | ANA1 | VREF<br>+ | C1IN0-<br>C2IN0- | —   | DAC1REF+ | —                     | —                                                                                       | —                   | —   | —                                          | SS2 <sup>(1)</sup>                             | —                                      | —                     | —    | IOCA1                       | Y       | ICDCLK/<br>ICSPCLK |
| RA2                | 17                    | 14          | ANA2 | VREF-     | —                | —   | DAC1REF- | —                     | T0CK1 <sup>(1)</sup>                                                                    | CCP3 <sup>(1)</sup> | —   | CWG1 <sup>(1)</sup><br>CWG2 <sup>(1)</sup> | —                                              | —                                      | CLCIN0 <sup>(1)</sup> | —    | INT <sup>(1)</sup><br>IOCA2 | Y       | —                  |
| RA3                | 4                     | 1           | —    | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA3                       | Y       | MCLR<br>VPP        |
| RA4                | 3                     | 20          | ANA4 | —         | —                | —   | —        | —                     | T1G <sup>(1)</sup><br>T3G <sup>(1)</sup><br>T5G <sup>(1)</sup><br>SOSCO                 | CCP4 <sup>(1)</sup> | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA4                       | Y       | CLKOUT<br>OSC2     |
| RA5                | 2                     | 19          | ANA5 | —         | —                | —   | —        | —                     | T1CK1 <sup>(1)</sup><br>T3CK1 <sup>(1)</sup><br>T5CK1 <sup>(1)</sup><br>SOSCIN<br>SOSCI | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCA5                       | Y       | CLKIN<br>OSC1      |
| RB4                | 13                    | 10          | ANB4 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SDI1 <sup>(1)</sup><br>SDA1 <sup>(1,3,4)</sup> | —                                      | CLCIN2 <sup>(1)</sup> | —    | IOCB4                       | Y       | —                  |
| RB5                | 12                    | 9           | ANB5 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SDI2 <sup>(1)</sup><br>SDA2 <sup>(1,3,4)</sup> | RX <sup>(1)</sup><br>DT <sup>(1)</sup> | CLCIN3 <sup>(1)</sup> | —    | IOCB5                       | Y       | —                  |
| RB6                | 11                    | 8           | ANB6 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SCK1 <sup>(1)</sup><br>SCL1 <sup>(1,3,4)</sup> | —                                      | —                     | —    | IOCB6                       | Y       | —                  |
| RB7                | 10                    | 7           | ANB7 | —         | —                | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | SCK2 <sup>(1)</sup><br>SCL2 <sup>(1,3,4)</sup> | TX <sup>(1)</sup><br>CK <sup>(1)</sup> | —                     | —    | IOCB7                       | Y       | —                  |
| RC0                | 16                    | 13          | ANC0 | —         | C2IN0+           | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC0                       | Y       | —                  |
| RC1                | 15                    | 12          | ANC1 | —         | C1IN1-<br>C2IN1- | —   | —        | —                     | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC1                       | Y       | —                  |
| RC2                | 14                    | 11          | ANC2 | —         | C1IN2-<br>C2IN2- | —   | —        | MDCIN1 <sup>(1)</sup> | —                                                                                       | —                   | —   | —                                          | —                                              | —                                      | —                     | —    | IOCC2                       | Y       | —                  |

- Note**
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  - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
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Fax: 31-416-690340

#### Poland - Warsaw

Tel: 48-22-3325737

#### Spain - Madrid

Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

#### Sweden - Stockholm

Tel: 46-8-5090-4654

#### UK - Wokingham

Tel: 44-118-921-5800  
Fax: 44-118-921-5820

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