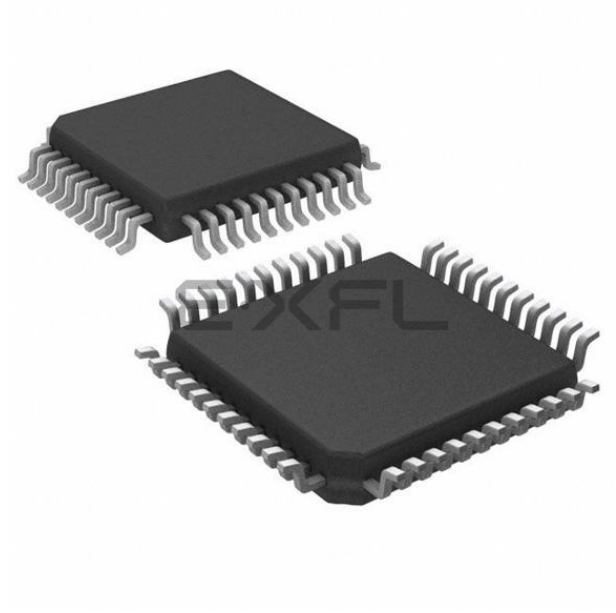
Infineon Technologies - C505CA4EMCABXQMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505ca4emcabxqma1

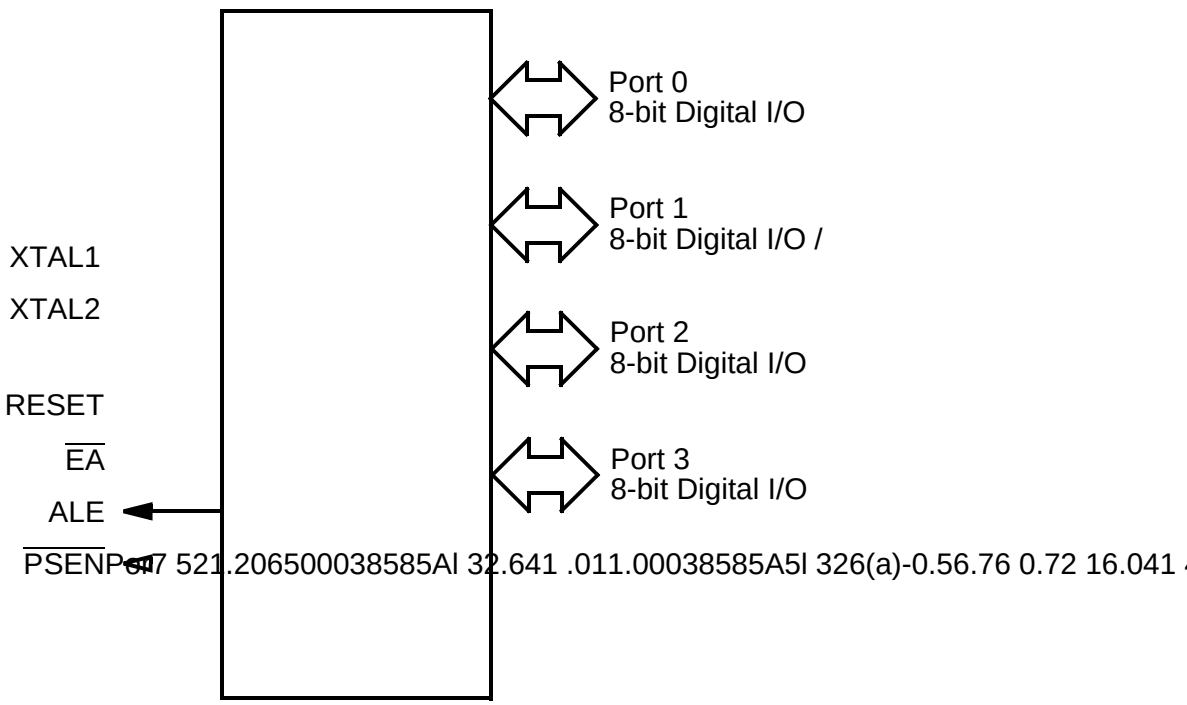


Figure 2
Logic Symbol

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
$\overline{EA}$	29	I	**$\overline{External\ Access\ Enable}$** When held at high level, instructions are fetched from the internal program memory when the PC is less than 4000_H (C505(C)(A)-2R) or 8000_H (C505A-4R/C505CA-4R/C505A-4E/C505CA-4E). When held at low level, the C505 fetches all instructions from external program memory. For the C505 romless versions (i.e. C505-L, C505C-L, C505A-L and C505CA-L) this pin must be tied low. For the ROM protection version $\overline{EA}$ pin is latched during reset.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C505 ROM versions. External pullup resistors are required during program verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{DD}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the RESET pin to V_{DD} via a capacitor. **Figure 6** shows the possible reset circuitries.

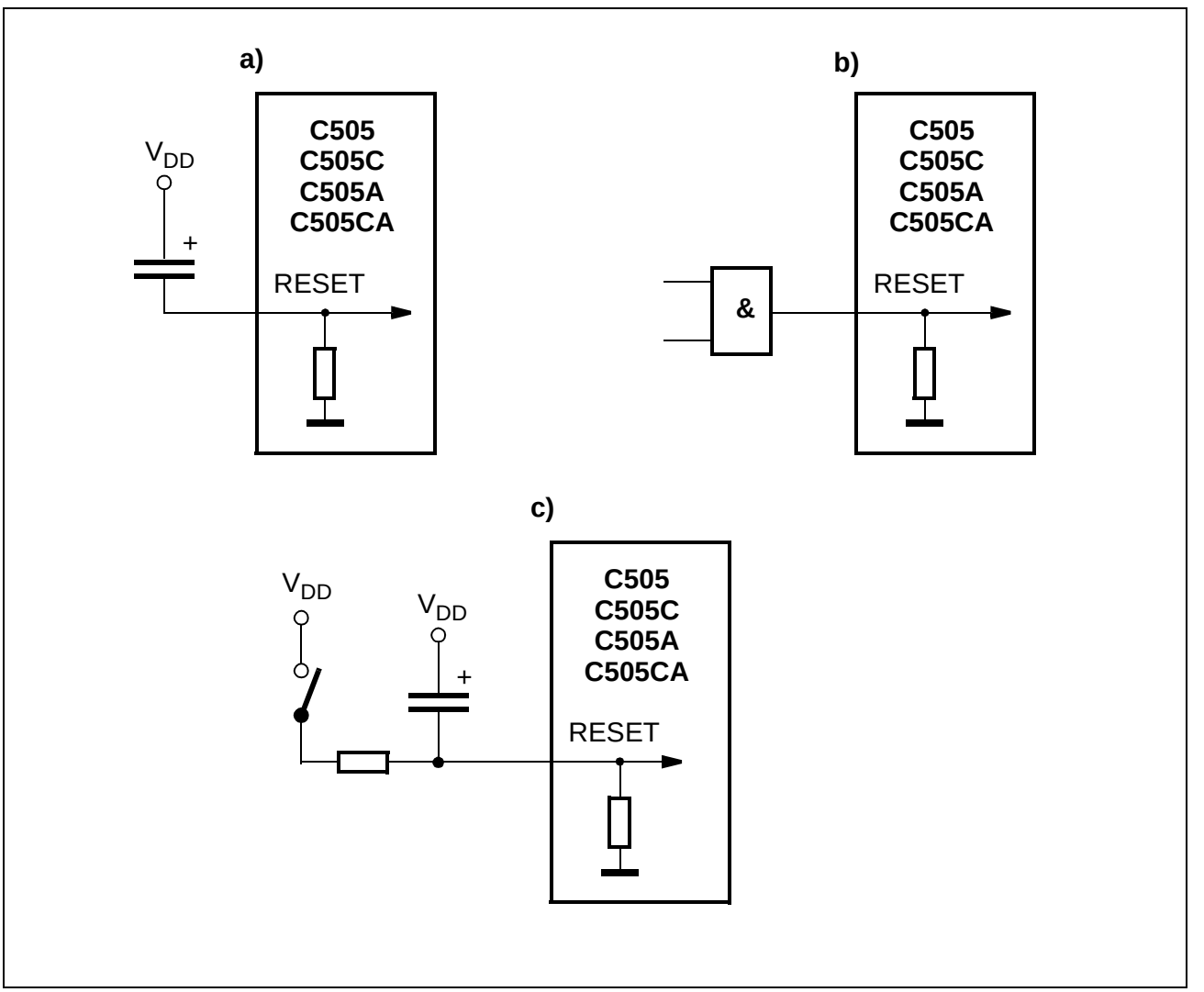


Figure 6
Reset Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

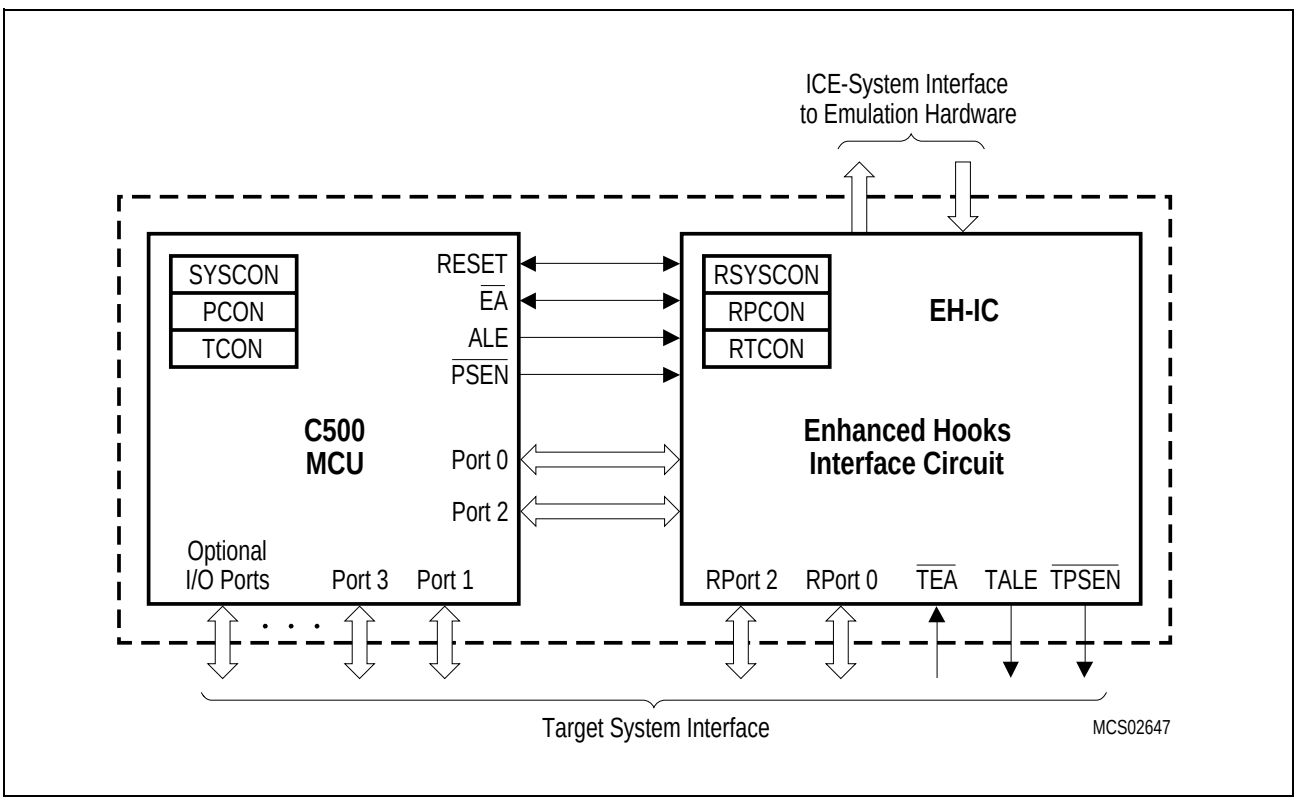


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Table 5
Contents of the CAN Registers in numeric order of their addresses (C505C/C505CA only)

Addr. n=1-F$_H$ 1)	Register	Content after Reset 2)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
F700$_H$	CR	01$_H$	TEST	CCE	0	0	EIE	SIE	IE	INIT
F701$_H$	SR	XX$_H$	BOFF	EWRN	–	RXOK	TXOK	LEC2	LEC1	LEC0
F702$_H$	IR	XX$_H$	INTID							
F704$_H$	BTR0	UU$_H$	SJW		BRP					
F705$_H$	BTR1	0UUU. UUUU$_B$	0	TSEG2			TSEG1			
F706$_H$	GMS0	UU$_H$	ID28-21							
F707$_H$	GMS1	UUU1. 1111$_B$	ID20-18			1	1	1	1	1
F708$_H$	UGML0	UU$_H$	ID28-21							
F709$_H$	UGML1	UU$_H$	ID20-13							
F70A$_H$	LGML0	UU$_H$	ID12-5							
F70B$_H$	LGML1	UUUU. U000$_B$	ID4-0					0	0	0
F70C$_H$	UMLM0	UU$_H$	ID28-21							
F70D$_H$	UMLM1	UU$_H$	ID20-18			ID17-13				
F70E$_H$	LMLM0	UU$_H$	ID12-5							
F70F$_H$	LMLM1	UUUU. U000$_B$	ID4-0					0	0	0
F7n0$_H$	MCR0	UU$_H$	MSGVAL		TXIE		RXIE		INTPND	
F7n1$_H$	MCR1	UU$_H$	RMTPND		TXRQ		MSGLST CPUUPD		NEWDAT	
F7n2$_H$	UAR0	UU$_H$	ID28-21							
F7n3$_H$	UAR1	UU$_H$	ID20-18			ID17-13				
F7n4$_H$	LAR0	UU$_H$	ID12-5							
F7n5$_H$	LAR1	UUUU. U000$_B$	ID4-0					0	0	0

1) The notation “n“ (n= 1 to F) in the address definition defines the number of the related message object.
2) “X“ means that the value is undefined and the location is reserved. “U“ means that the value is unchanged by a reset operation. “U“ values are undefined (as “X“) after a power-on reset operation

I/O Ports

The C505 has four 8-bit I/O ports and one 2-bit I/O port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 4 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 4 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET .

Port 4 is 2-bit I/O port with CAN controller specific alternate functions. The eight analog input lines are realized as mixed digital/analog inputs. The 8 analog inputs, AN0-AN7, are located at the port 1 pins P1.0 to P1.7. After reset, all analog inputs are disabled and the related pins of port 1 are configured as digital inputs. The analog function of a specific port 1 pin is enabled by bits in the SFR P1ANA. Writing a 0 to a bit position of P1ANA assigns the corresponding pin to operate as analog input.

Note : P1ANA is a mapped SFR and can be only accessed if bit RMAP in SFR SYSCON is set.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{osc}/6x32	f_{osc}/12x32
1	16-bit timer/counter	0	1	f_{osc}/6	f_{osc}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{osc}/6.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{osc}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

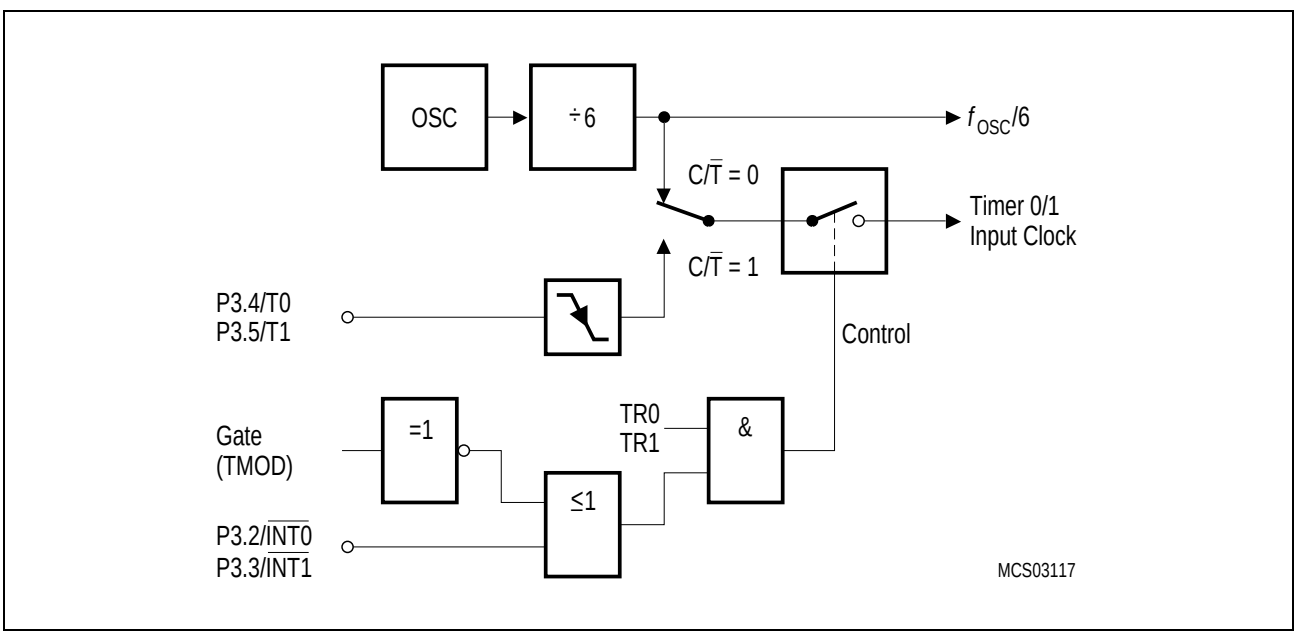


Figure 10
Timer/Counter 0 and 1 Input Clock Logic

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 12** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

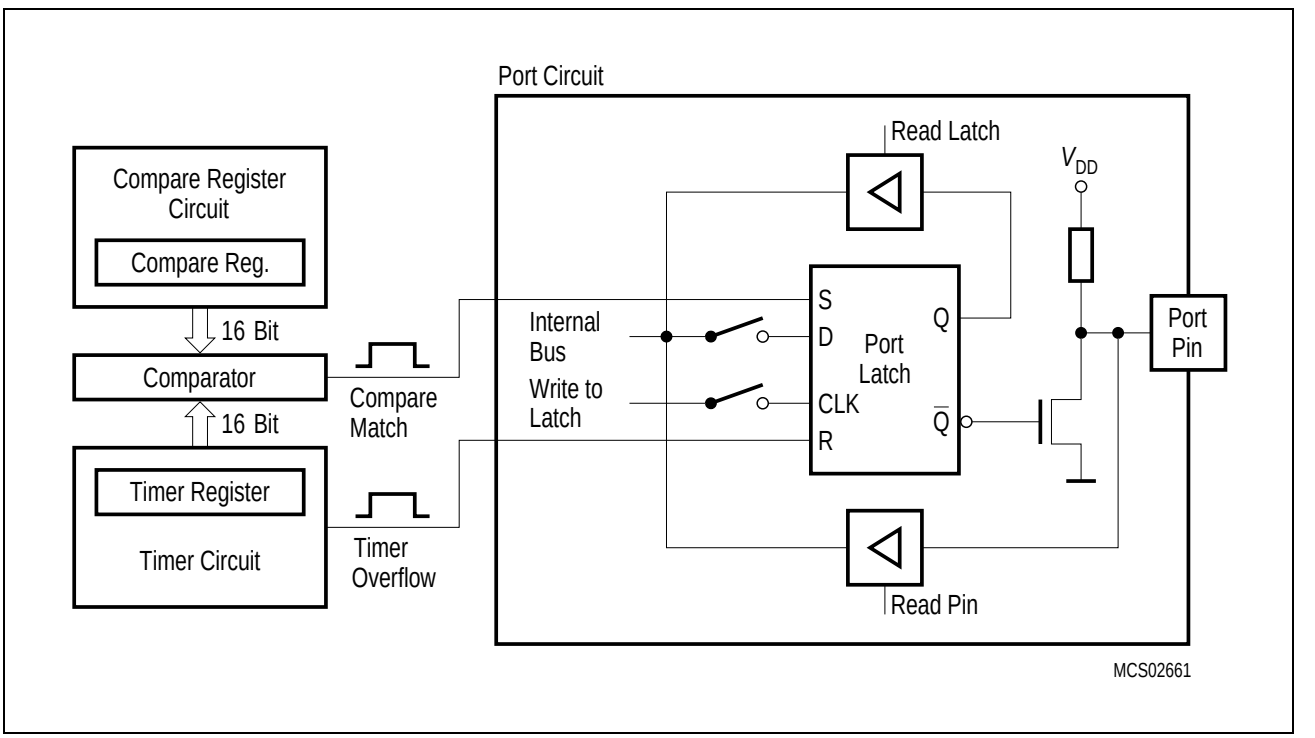


Figure 12
Port Latch in Compare Mode 0

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 7**.

Table 7
USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode, fixed baud rate Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	9-bit UART, variable baud rate Like mode 2

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **Figure 14** to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abbrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a decdicated baud rate generator (see **Figure 14**).

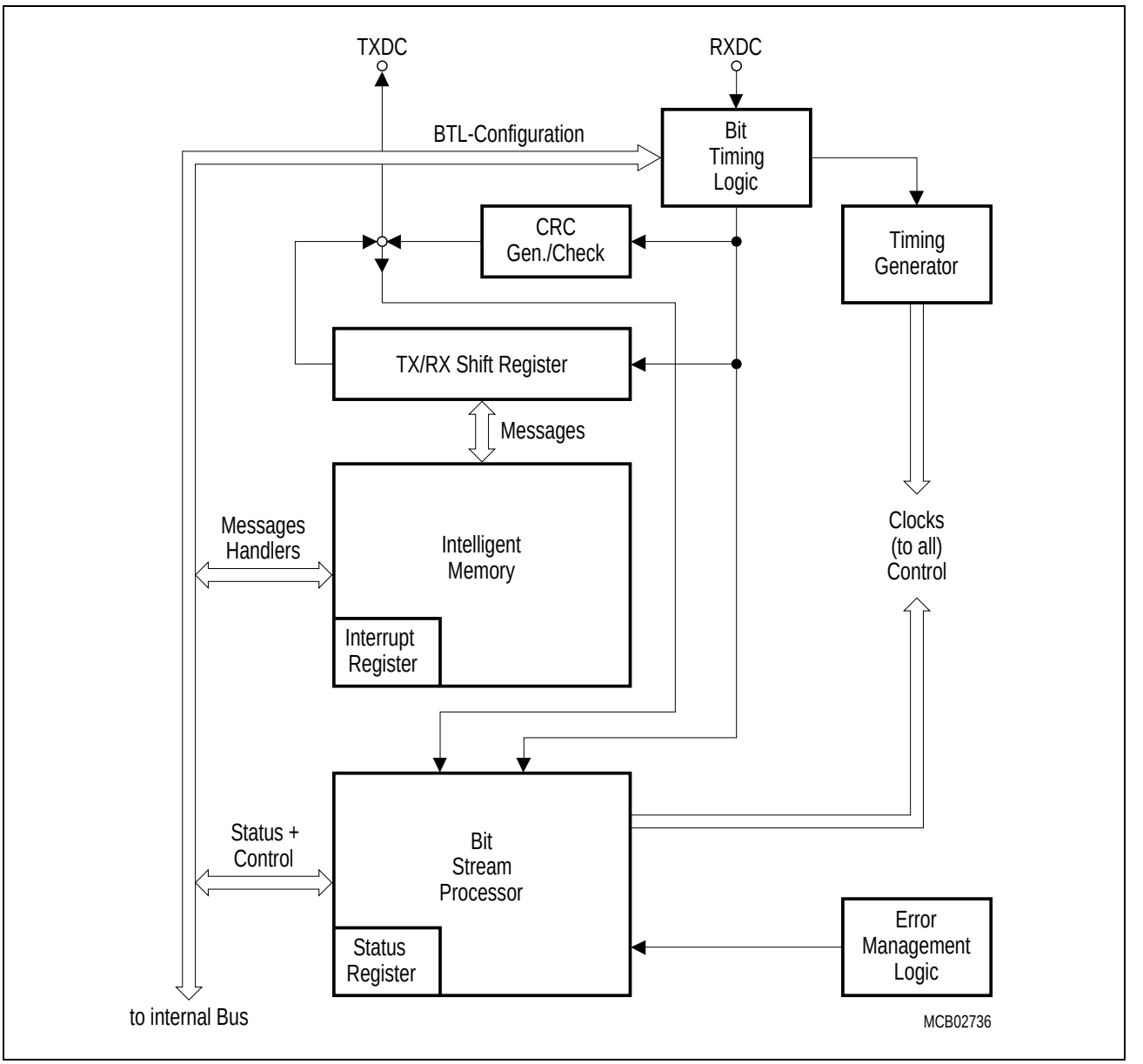


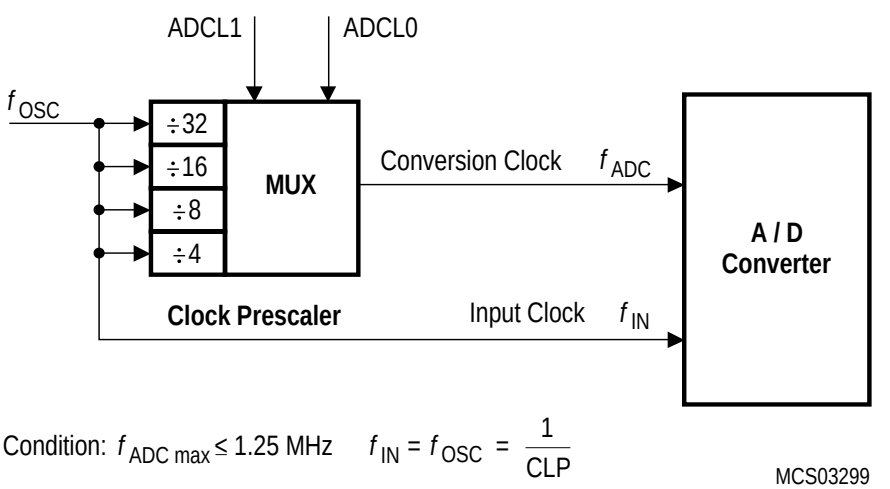
Figure 15
CAN Controller Block Diagram

8-Bit A/D Converter (C505 and C505C only)

The C505/C505C includes a high performance / high speed 8-bit A/D converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital outputs/inputs
- 8-bit resolution
- Internal start-of-conversion trigger
- Interrupt request generation after each conversion
- Single or continuous conversion mode

The 8-bit ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (1/t_{IN}). f_{ADC} is derived from the C505 system clock f_{OSC} which is applied at the XTAL pins via the ADC clock prescaler as shown in **Figure 17**. The input clock is equal to f_{OSC}. The conversion clock f_{ADC} is limited to a maximum frequency of 1.25 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 1.25 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
5 MHz	5	÷ 4	1.25	0	0
6 MHz	6	÷ 8	0.75	0	1
10 MHz	10	÷ 8	1.25	0	1
12 MHz	12	÷ 16	0.75	1	0
16 MHz	16	÷ 16	1	1	0
20 MHz	20	÷ 16	1.25	1	0

Figure 17
8-Bit A/D Converter Clock Selection

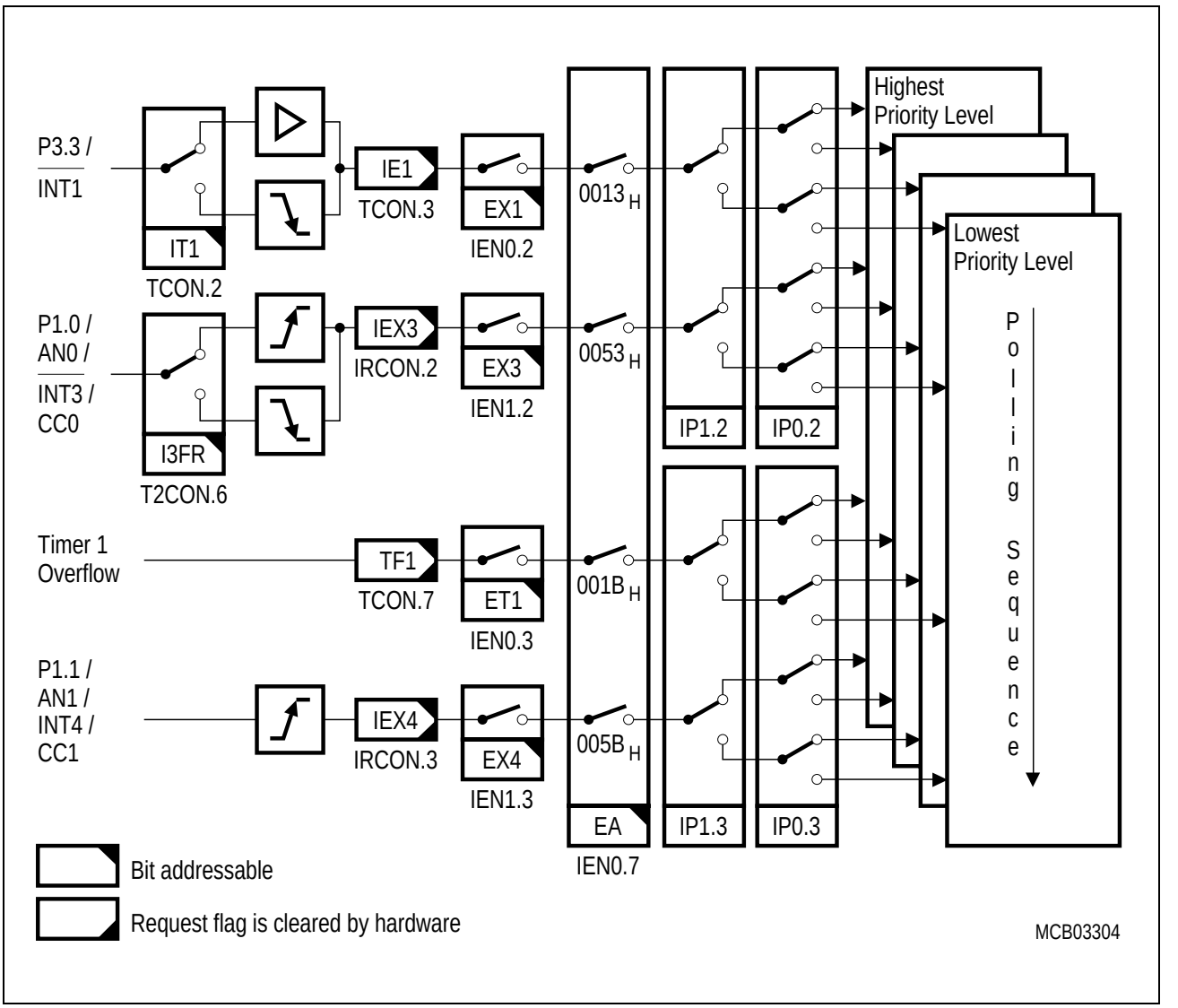


Figure 22
Interrupt Structure, Overview Part 2

Fail Save Mechanisms

The C505 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

- a programmable watchdog timer (WDT), with variable time-out period from 192 µs up to approx. 393.2 ms at 16 MHz (314.5 ms at 20 MHz).
- an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C505 is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ upto $f_{OSC}/192$. The system clock of the C505 is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bits of the watchdog timer can be written. **Figure 24** shows the block diagram of the watchdog timer unit.

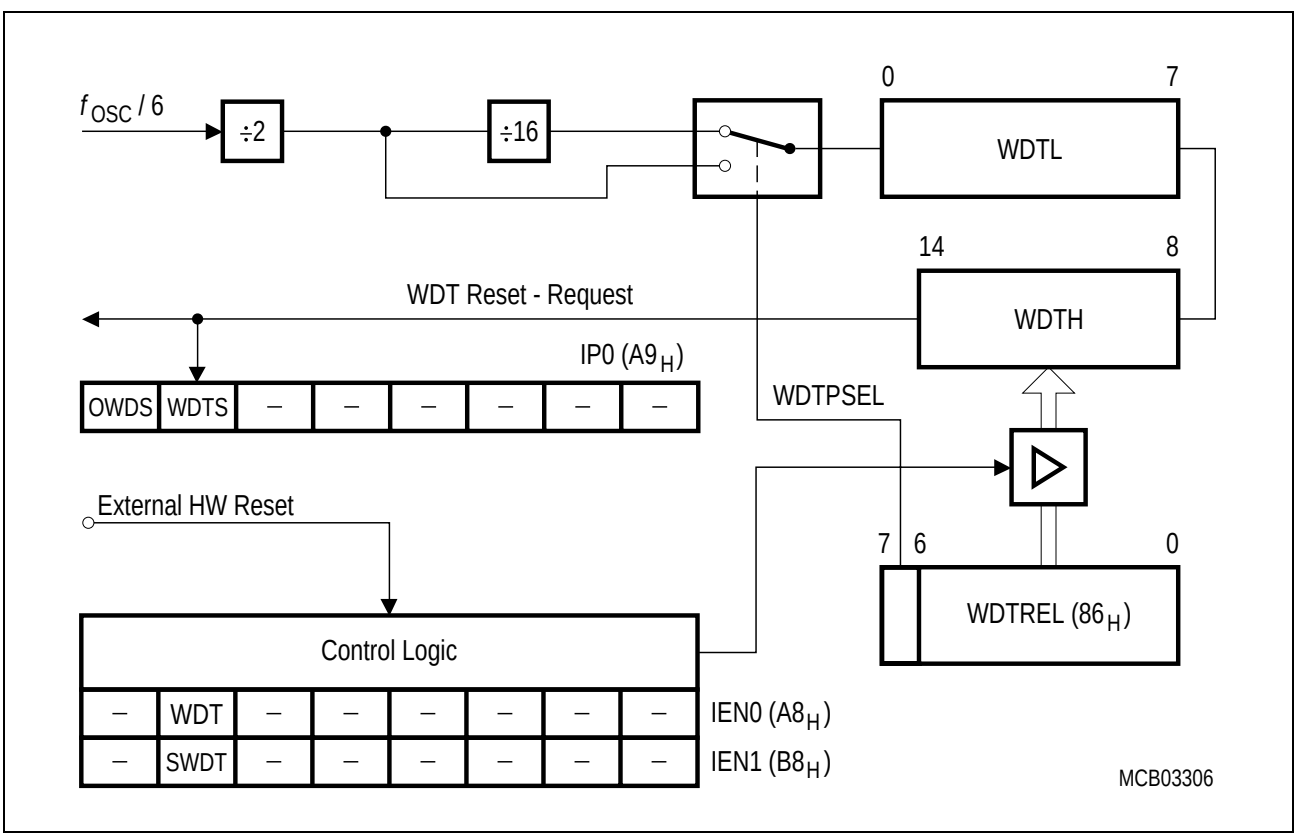


Figure 24
Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT in SFR IEN1) but it cannot be stopped during active mode of the device. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transfered to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consequtive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 28**.

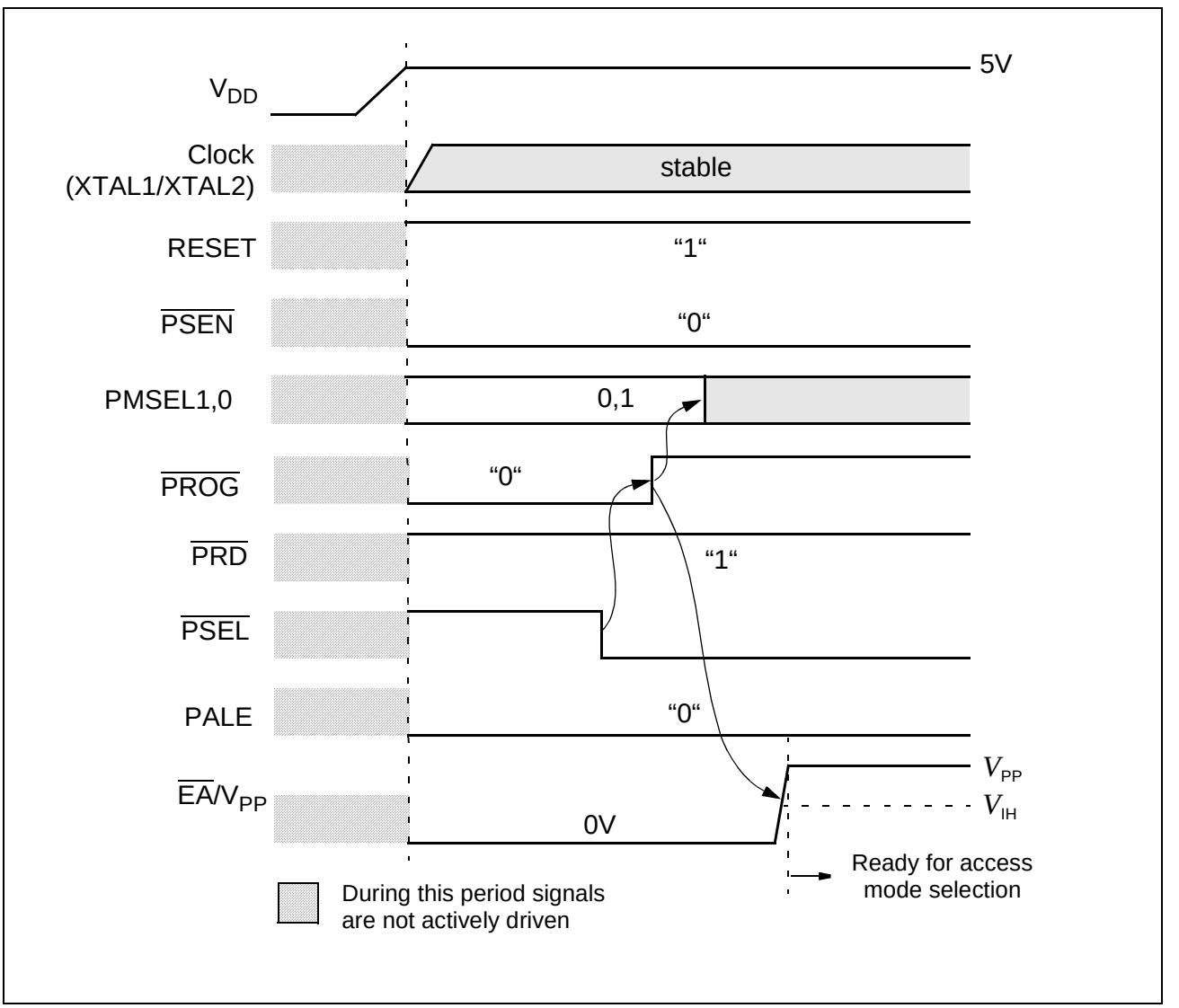


Figure 28
Basic Programming Mode Selection

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode, $f_{osc\ max}$ = 20 MHz
		2	5.5	V	PowerDown mode
Ground voltage	V_{SS}	0		V	Reference voltage
Ambient temperature				°C	–
SAB-C505	T_A	0	70		
SAF-C505	T_A	-40	85		
SAH-C505	T_A	-40	110		
SAK-C505	T_A	-40	125		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND} -0.2	V_{AREF} +0.2	V	–
XTAL clock	f_{osc}	2	20 (with 50% duty cycle)	MHz	1)

1) For the extended temperature range -40 °C to 110 °C (SAH) and -40 °C to 125 °C (SAK), the devices C505-2R, C505-L, C505C-2R and C505C-L have the max. operating frequency of 16MHz with 50% clock duty cycle.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C505 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the C505 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective characteristics to the C505.

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} -15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} -15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP - 50	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	TCL_{Lmin} -15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} -15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}- 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} -55	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (20 MHz, 0.5 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

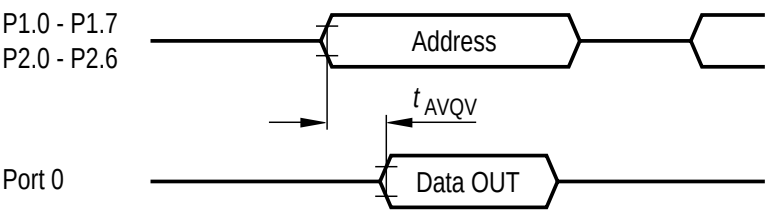
Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	CLP/2 - 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	CLP/2 - 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	55	–	2 CLP - 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	CLP/2 - 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	3/2 CLP - 15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	25	–	3/2 CLP - 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	CLP/2 - 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	CLP/2 - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	65	–	5/2 CLP - 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	- 5	–	- 5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

ROM/OTP Verification Characteristics for C505

ROM Verification Mode 1 (C505(C)(A)-2R and C505(C)A-4R only)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	5 CLP	ns



Address: P1.0 - P1.7 = A0 - A7
P2.0 - P2.6 = A8 - A14
Data: P0.0 - P0.7 = D0 - D7

Inputs: P2.7, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IH2}

Note: P2.6 should be connected to V_{SS} for C505(C)(A)-2R

Figure 40
ROM Verification Mode 1

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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