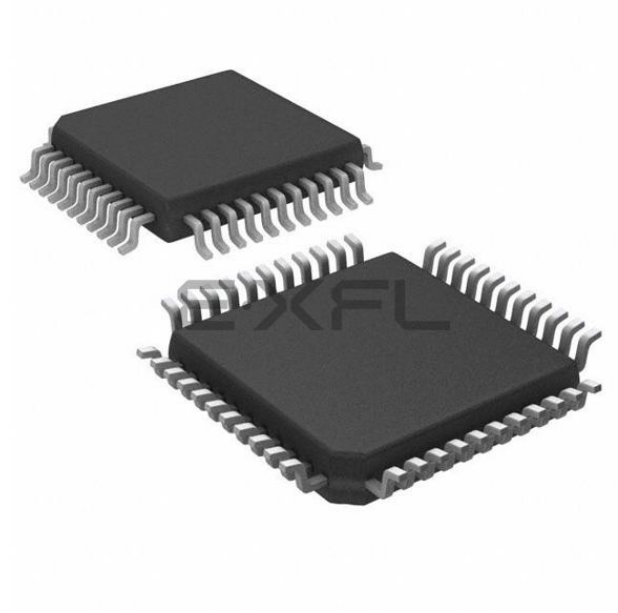
Infineon Technologies - C505CA4EMCABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505ca4emcabxuma1

Edition 2000-12

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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Table 2
Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function
P1.0-P1.7	40-44,1-3	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs of the A/D converter. Port 1 pins that have 1's written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 — Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O
	41		P1.1 / AN1 / INT4 / CC1 — Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O
	42		P1.2 / AN2 / INT5 / CC2 — Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
	43		P1.3 / AN3 / INT6 / CC3 — Analog input channel 3 interrupt 6 input / capture/compare channel 3 I/O
	44		P1.4 / AN4 — Analog input channel 4
	1		P1.5 / AN5 / T2EX — Analog input channel 5 / Timer 2 external reload / trigger input
	2		P1.6 / AN6 / CLKOUT — Analog input channel 6 / system clock output
	3		P1.7 / AN7 / T2 — Analog input channel 7 / counter 2 input
			Port 1 is used for the low-order address byte during program verification of the C505 ROM versions (i.e. C505(C)(A)-2R/ C505A-4R/C505CA-4R).

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal ROM or OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
$\overline{EA}$	29	I	**$\overline{External\ Access\ Enable}$** When held at high level, instructions are fetched from the internal program memory when the PC is less than 4000_H (C505(C)(A)-2R) or 8000_H (C505A-4R/C505CA-4R/C505A-4E/C505CA-4E). When held at low level, the C505 fetches all instructions from external program memory. For the C505 romless versions (i.e. C505-L, C505C-L, C505A-L and C505CA-L) this pin must be tied low. For the ROM protection version $\overline{EA}$ pin is latched during reset.
P0.0-P0.7	37-30	I/O	**Port 0** is an 8-bit open-drain bidirectional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impendance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program or data memory. In this application it uses strong internal pullup transistors when issuing 1's. Port 0 also outputs the code bytes during program verification in the C505 ROM versions. External pullup resistors are required during program verification.
V_{AREF}	38	–	**Reference voltage** for the A/D converter.
V_{AGND}	39	–	**Reference ground** for the A/D converter.
V_{SS}	16	–	**Ground** (0V)
V_{DD}	17	–	**Power Supply** (+5V)

*) I = Input
O = Output

Reset and System Clock

The reset input is an active high input at pin RESET. Since the reset is synchronized internally, the RESET pin must be held high for at least two machine cycles (12 oscillator periods) while the oscillator is running. A pulldown resistor is internally connected to V_{SS} to allow a power-up reset with an external capacitor only. An automatic reset can be obtained when V_{DD} is applied by connecting the RESET pin to V_{DD} via a capacitor. **Figure 6** shows the possible reset circuitries.

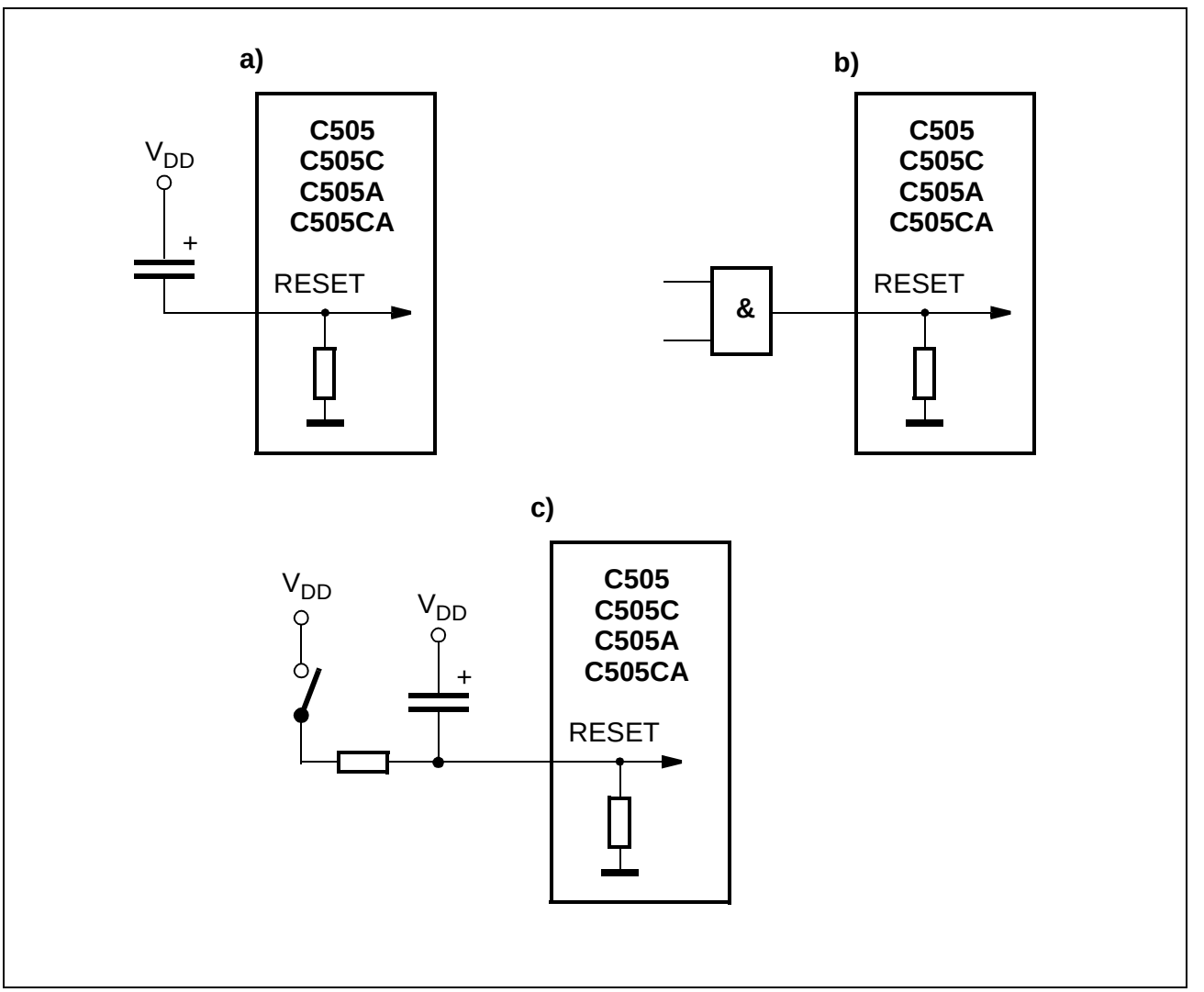


Figure 6
Reset Circuitries

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C505 contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function regsiter DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

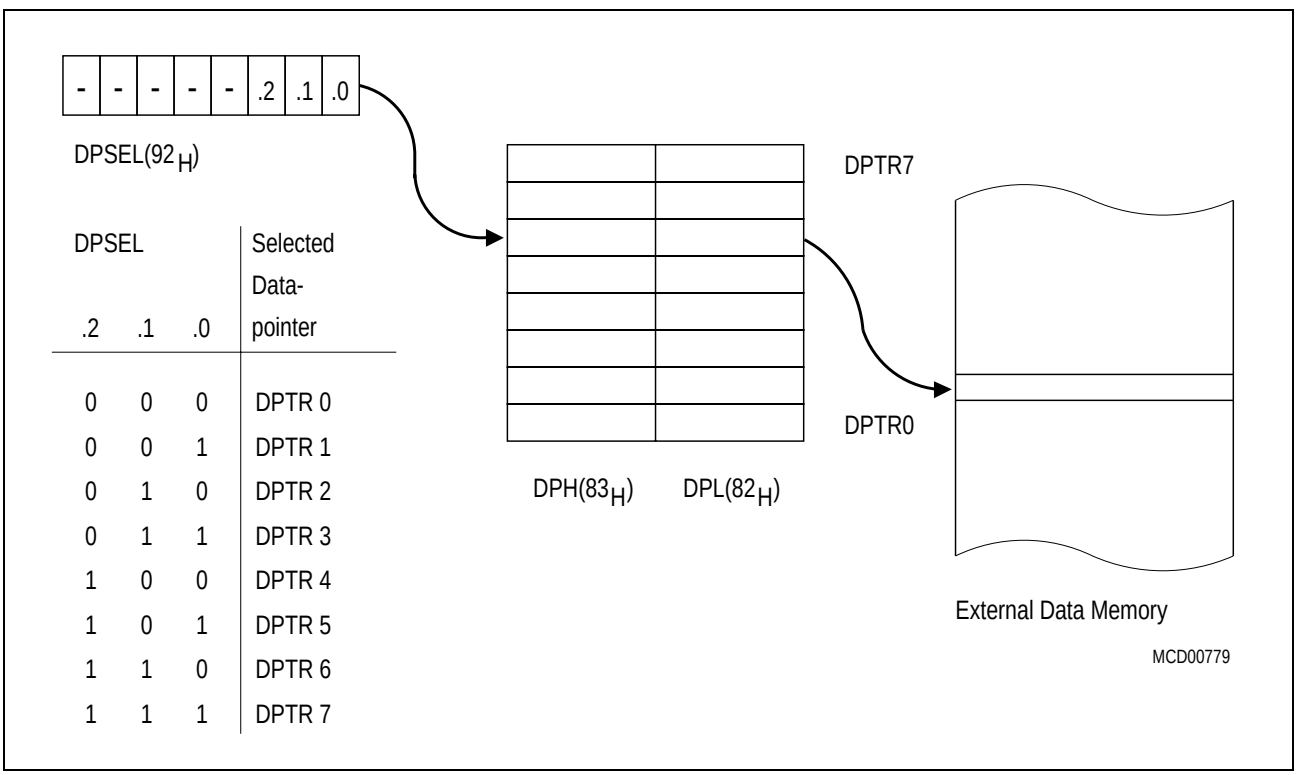


Figure 8
External Data Memory Addressing using Multiple Datapointers

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

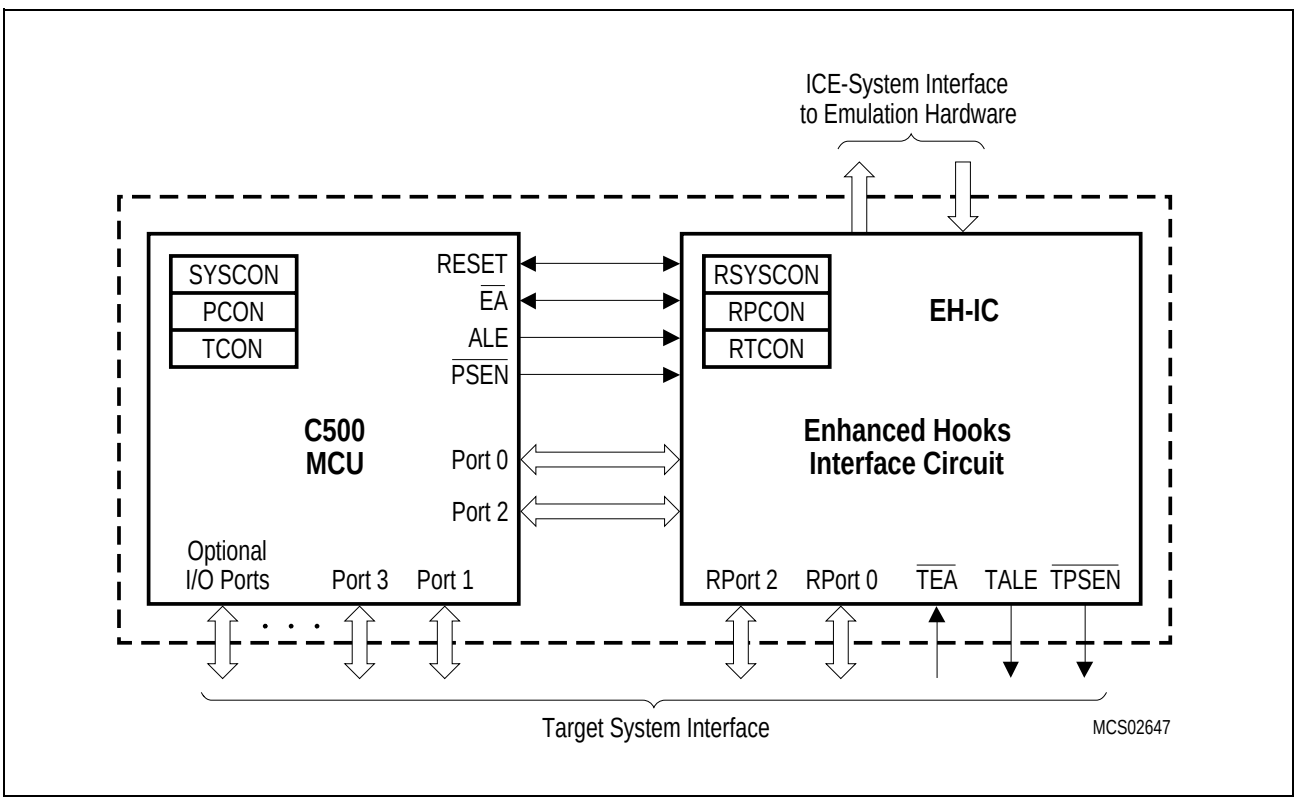


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions : the standard special function register area and the mapped special function register area. Five special function register of the C505 (PCON1,P1ANA, VR0, VR1, VR2) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

The registers and data locations of the CAN controller (CAN-SFRs) are located in the external data memory area at addresses $F700_H$ to $F7FF_H$..

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100X01_B$**
(C505CA only) **Reset Value : $XX100001_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	CMOD	CSWO 1)	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described here.
1) This bit is only available in the C505CA.

Bit	Function
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
CSWO	CAN Controller switch-off bit CSWO = 0 : CAN Controller is enabled (default after reset). CSWO = 1 : CAN Controller is switched off.

As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 52 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505 are listed in **Table 3** and **Table 4**. In **Table 3** they are organized in groups which refer to the functional blocks of the C505. The CAN-SFRs (applicable for the C505C and C505CA only) are also included in **Table 3**. **Table 4** illustrates the contents of the SFRs in numeric order of their addresses. **Table 5** list the CAN-SFRs in numeric order of their addresses.

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2) 4)	Port 1 Analog Input Selection Register	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**E8H** 1)	$XXXXXX11_B$
Serial Channel	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H 3)
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$ 3)
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
Pow. Save Modes	PCON 2)	Power Control Register	87_H	00_H
	PCON1 4)	Power Control Register 1	**88_H** 1)	$0XX0XXXX_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 12** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

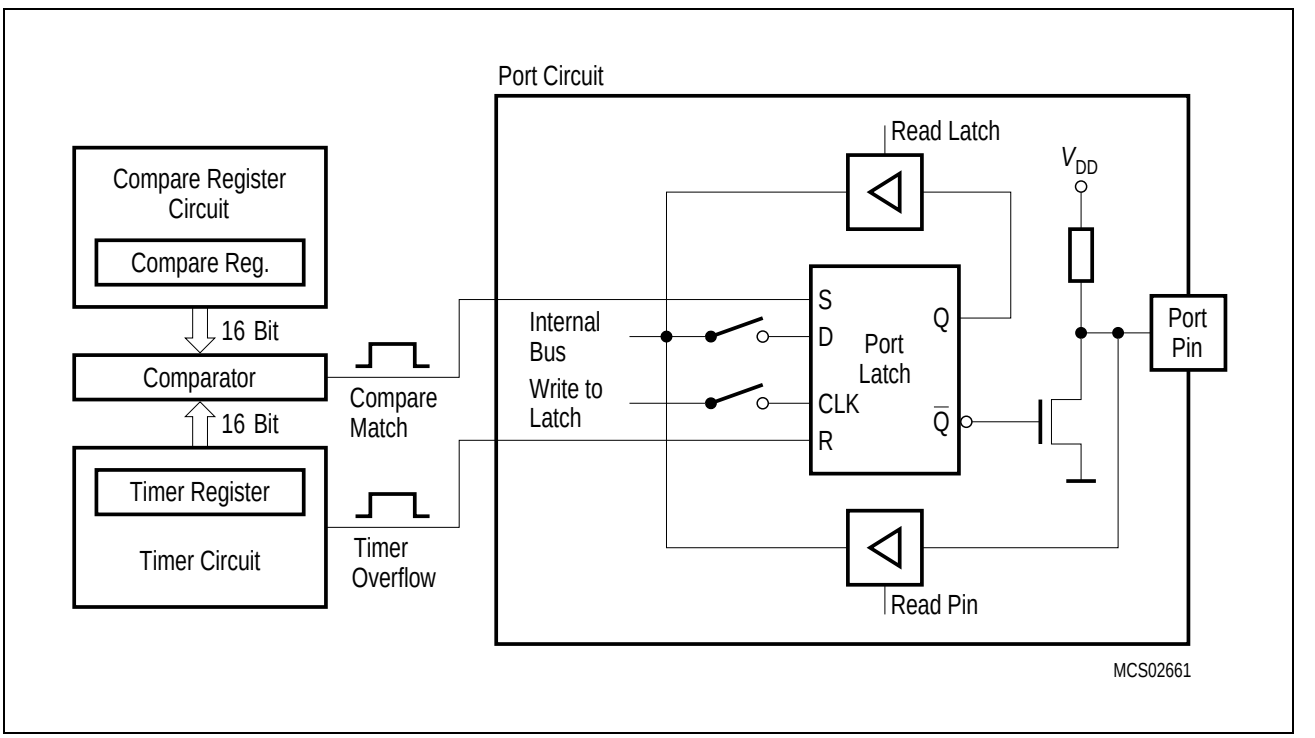


Figure 12
Port Latch in Compare Mode 0

CAN Controller (C505C and C505CA only)

The on-chip CAN controller, compliant to version 2.0B, is the functional heart which provides all resources that are required to run the standard CAN protocol (11-bit identifiers) as well as the extended CAN protocol (29-bit identifiers). It provides a sophisticated object layer to relieve the CPU of as much overhead as possible when controlling many different message objects (up to 15). This includes bus arbitration, resending of garbled messages, error handling, interrupt generation, etc. In order to implement the physical layer, external components have to be connected to the C505C/C505CA.

The internal bus interface connects the on-chip CAN controller to the internal bus of the microcontroller. The registers and data locations of the CAN interface are mapped to a specific 256 byte wide address range of the external data memory area ($F700_H$ to $F7FF_H$) and can be accessed using MOVX instructions. **Figure 15** shows a block diagram of the on-chip CAN controller.

The **TX/RX Shift Register** holds the destuffed bit stream from the bus line to allow the parallel access to the whole data or remote frame for the acceptance match test and the parallel transfer of the frame to and from the Intelligent Memory.

The **Bit Stream Processor (BSP)** is a sequencer controlling the sequential data stream between the TX/RX Shift Register, the CRC Register, and the bus line. The BSP also controls the EML and the parallel data stream between the TX/RX Shift Register and the Intelligent Memory such that the processes of reception, arbitration, transmission, and error signalling are performed according to the CAN protocol. Note that the automatic retransmission of messages which have been corrupted by noise or other external error conditions on the bus line is handled by the BSP.

The **Cyclic Redundancy Check Register (CRC)** generates the Cyclic Redundancy Check code to be transmitted after the data bytes and checks the CRC code of incoming messages. This is done by dividing the data stream by the code generator polynomial.

The **Error Management Logic (EML)** is responsible for the fault confinement of the CAN device. Its counters, the Receive Error Counter and the Transmit Error Counter, are incremented and decremented by commands from the Bit Stream Processor. According to the values of the error counters, the CAN controller is set into the states error *active*, error *passive* and busoff.

The **Bit Timing Logic (BTL)** monitors the busline input RXDC and handles the busline related bit timing according to the CAN protocol. The BTL synchronizes on a *recessive* to *dominant* busline transition at *Start of Frame* (hard synchronization) and on any further *recessive* to *dominant* busline transition, if the CAN controller itself does not transmit a *dominant* bit (resynchronization). The BTL also provides programmable time segments to compensate for the propagation delay time and for phase shifts and to define the position of the Sample Point in the bit time. The programming of the BTL depends on the baudrate and on external physical delay times.

The **Intelligent Memory** (CAM/RAM array) provides storage for up to 15 message objects of maximum 8 data bytes length. Each of these objects has a unique identifier and its own set of control and status bits. After the initial configuration, the Intelligent Memory can handle the reception and transmission of data without further microcontroller actions.

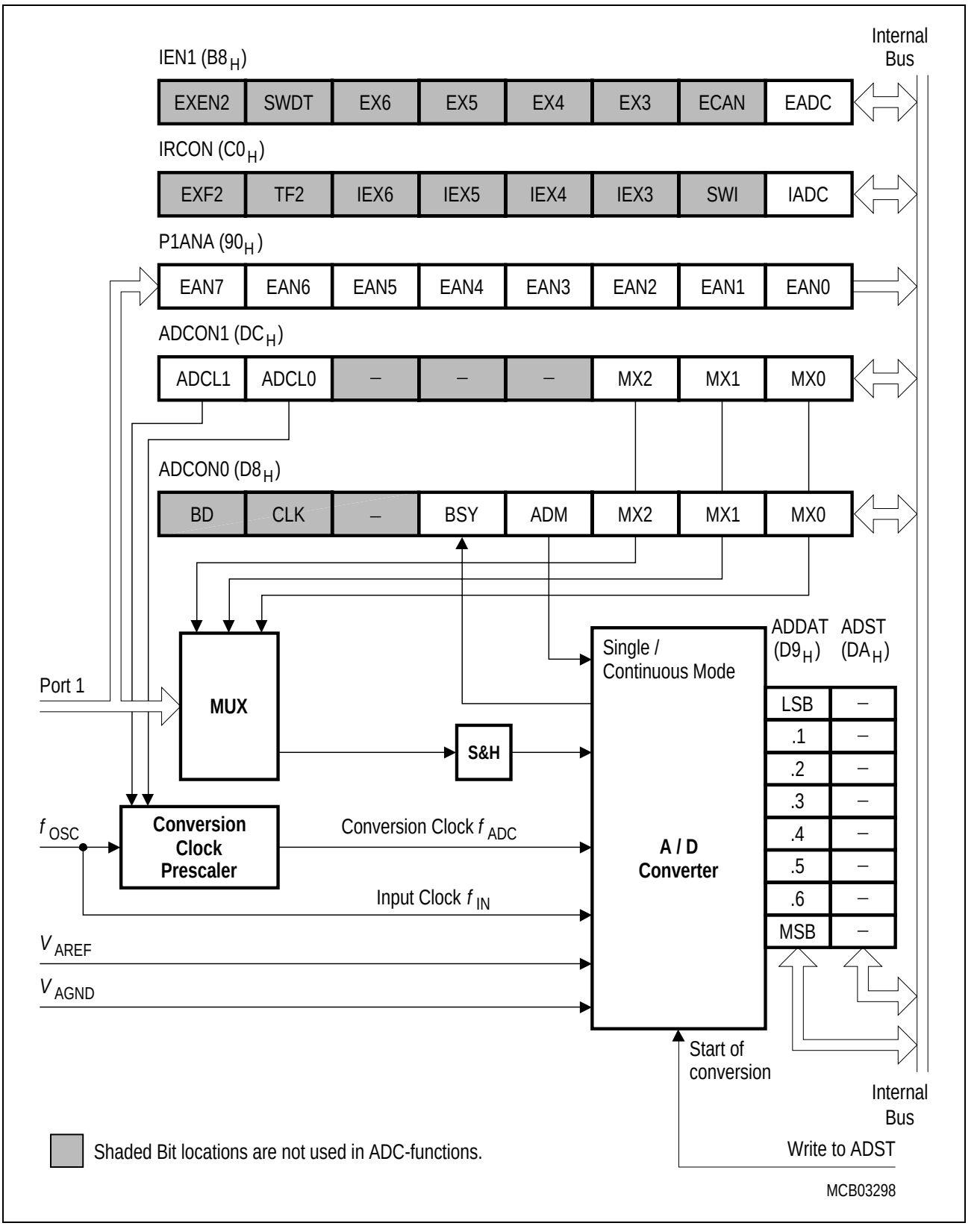


Figure 18
Block Diagram of the 8-Bit A/D Converter

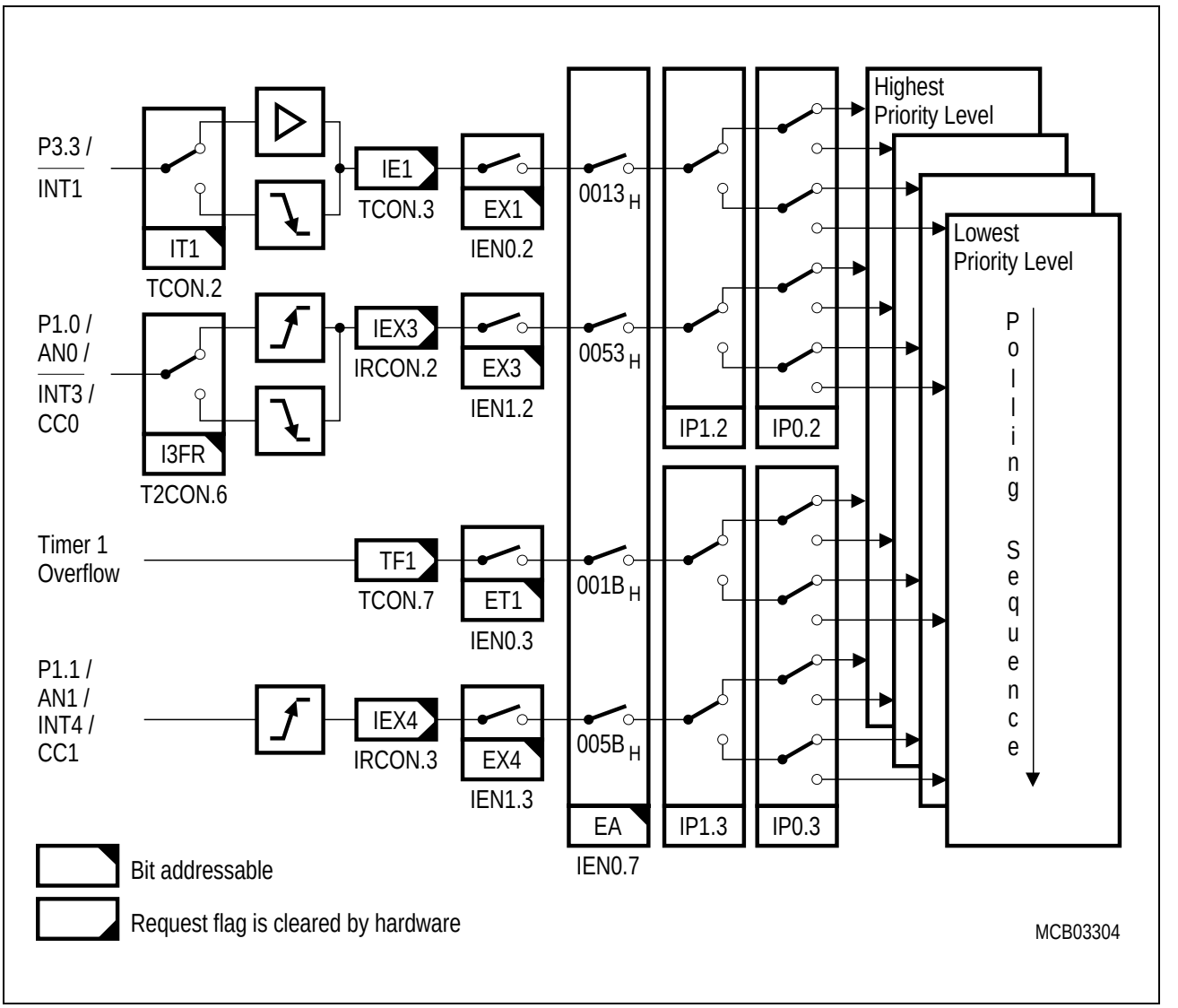


Figure 22
Interrupt Structure, Overview Part 2

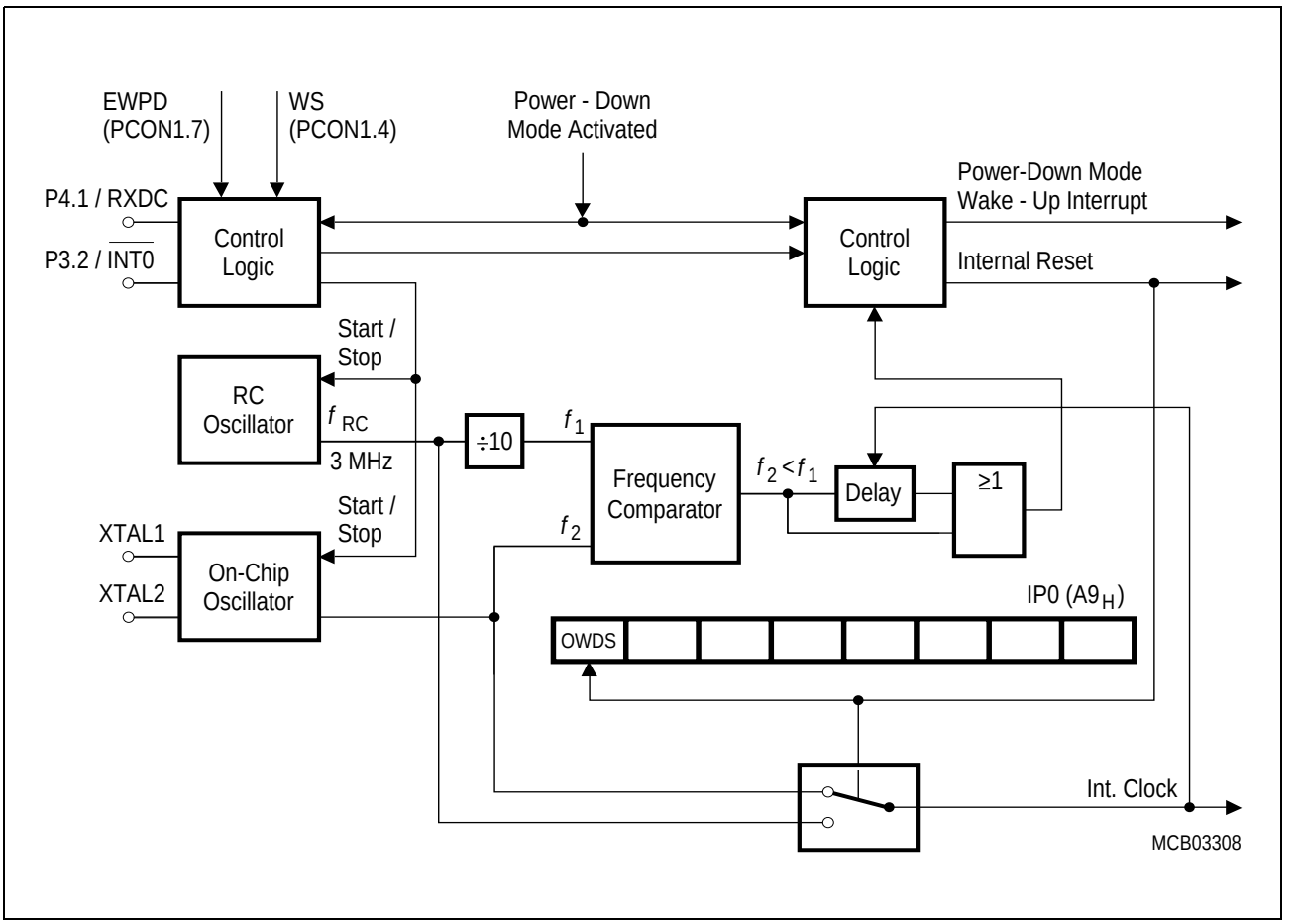


Figure 25
Functional Block Diagram of the Oscillator Watchdog

Power Saving Modes

The C505 provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  In the idle mode the main oscillator of the C505 continues to run, but the CPU is gated off from the clock signal. All peripheral units are further provided with the clock. The CPU status is preserved in its entirety. The idle mode can be terminated by any enabled interrupt of a peripheral unit or by a hardware reset.
- **Power down mode**
  The operation of the C505 is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. Power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/$\overline{\text{INT0}}$.or P4.1/RXDC.
- **Slow down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32-th of their normal operating frequency. Slowing down the frequency significantly reduces power consumption.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated. **Table 10** gives a general overview of the entry and exit procedures of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering (Instruction Example)	Leaving by	Remarks
Idle Mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC	
Slow Down Mode	ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Oscillator frequency is reduced to 1/32 of its nominal frequency

Table 11
Pin Definitions and Functions in Programming Mode (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-7	18-25	I	**Address lines** P2.0-7 are used as multiplexed address input lines A0-A7 and A8-A14. A8-A14 must be latched with PALE.
$\overline{\text{PSEN}}$	26	I	**Program store enable** This input must be at static "0" level during the whole programming mode.
$\overline{\text{PROG}}$	27	I	**Programming mode write strobe** This input is used in programming mode as a write strobe for OTP memory program, and lock bit write operations During basic programming mode selection a low level must be applied to $\overline{\text{PROG}}$.
$\overline{\text{EA}}/V_{PP}$	29	–	**$\overline{\text{External Access}}$ / Programming voltage** This pin must be at 11.5V (V_{PP}) voltage level during programming of an OTP memory byte or lock bit. During an OTP memory read operation this pin must be at V_{IH} high level. This pin is also used for basic programming mode selection. At basic programming mode selection a low level must be applied to $\overline{\text{EA}}/V_{PP}$.
D7-0	30-37	I/O	**Data lines 0-7** During programming mode, data bytes are transferred via the bidirectional port 0 data lines.
N.C.	1-3, 6, 11-13, 28, 38-44	–	**Not Connected** These pins should not be connected in programming mode.

*) I = Input
O = Output

Table 12
Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL		Address (Port 2)	Data (Port 0)
				1	0		
Program OTP memory byte	V_{PP}	⊓	H	H	H	A0-7 A8-14	D0-7
Read OTP memory byte	V_{IH}	H	⊓				
Program OTP lock bits	V_{PP}	⊓	H	H	L	–	D1,D0 see Table 13
Read OTP lock bits	V_{IH}	H	⊓				
Read OTP version byte	V_{IH}	H	⊓	L	H	Byte addr. of sign. byte	D0-7

Lock Bits Programming / Read

The C505A-4E/C505CA-4E has two programmable lock bits which, when programmed according to **Table 13**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 13
Lock Bit Protection Types

Lock Bits at D1,D0		Protection Level	Protection Type
D1	D0		
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C505A-4E/C505CA-4E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C505A-4E/C505CA-4E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible using the ROM/OTP verification mode 2 for protection level 1. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C505A-4E/ C505CA-4E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

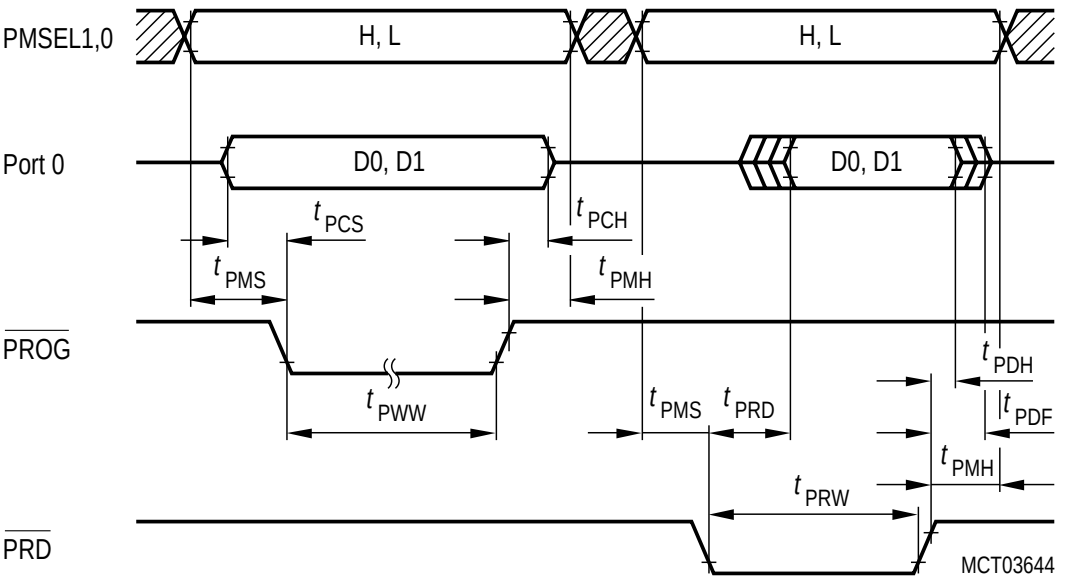
5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

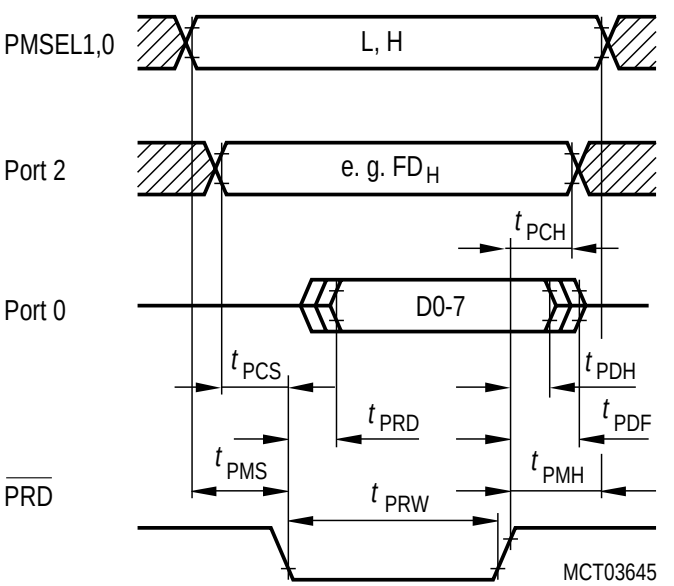
External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	158	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	158	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	100	–	2 CLP+ TCL_{Hmin} - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP + TCL_{Hmin} -75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	73	103	CLP + TCL_{Lmin} - 15	CLP+ TCL_{Lmin}+ 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	95	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	TCL_{Hmin} - 15	TCL_{Hmin} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	TCL_{Hmin} - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns



Note: PALE should be low during a lock bit read / write cycle.

Figure 38
Lock Bit Access Timing



Note: $\overline{\text{PROG}}$ must be high during a programming read cycle.

Figure 39
Version Byte Read Timing