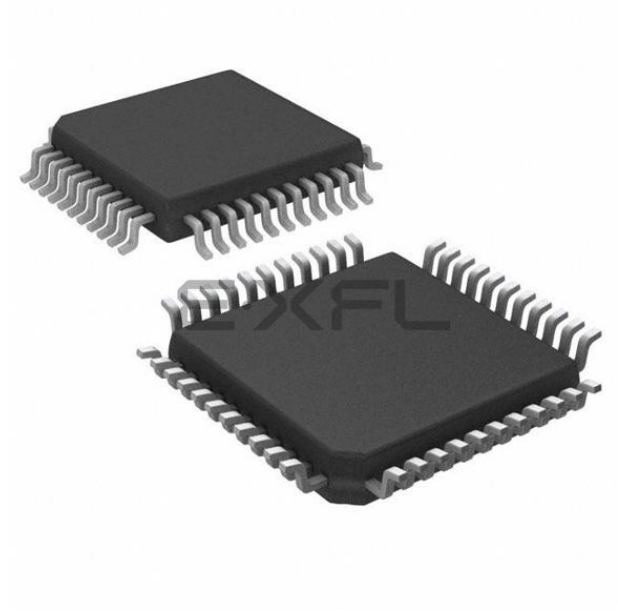
Infineon Technologies - C505CA4EMCAFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505ca4emcafxuma1

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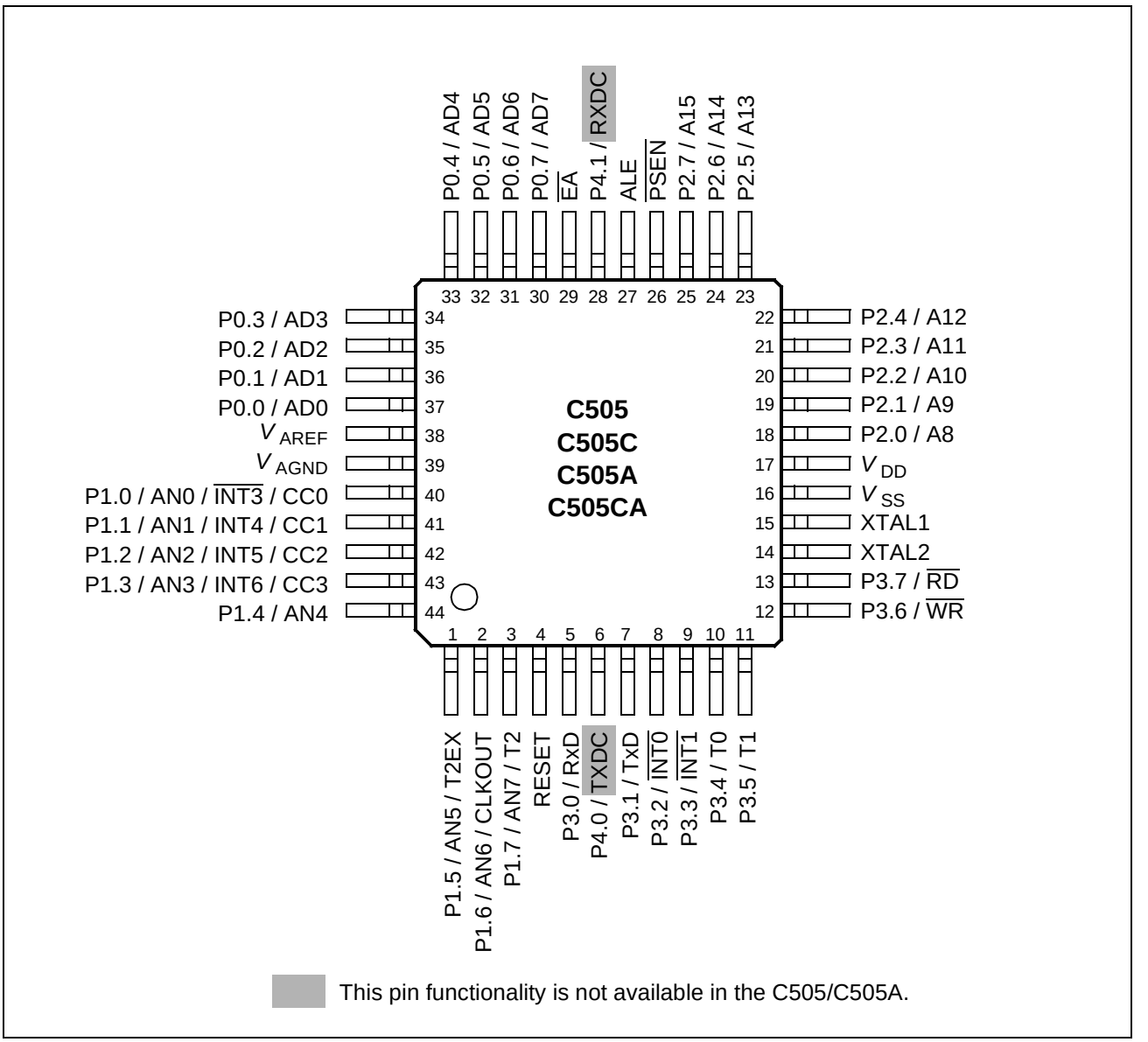


Figure 3
C505 Pin Configuration P-MQFP-44 Package (Top View)

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
RESET	4	I	**RESET** A high level on this pin for two machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	9		P3.3 / $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	10		P3.4 / T0 — Timer 0 counter input
	11		P3.5 / T1 — Timer 1 counter input
	12		P3.6 / $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal ROM or OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

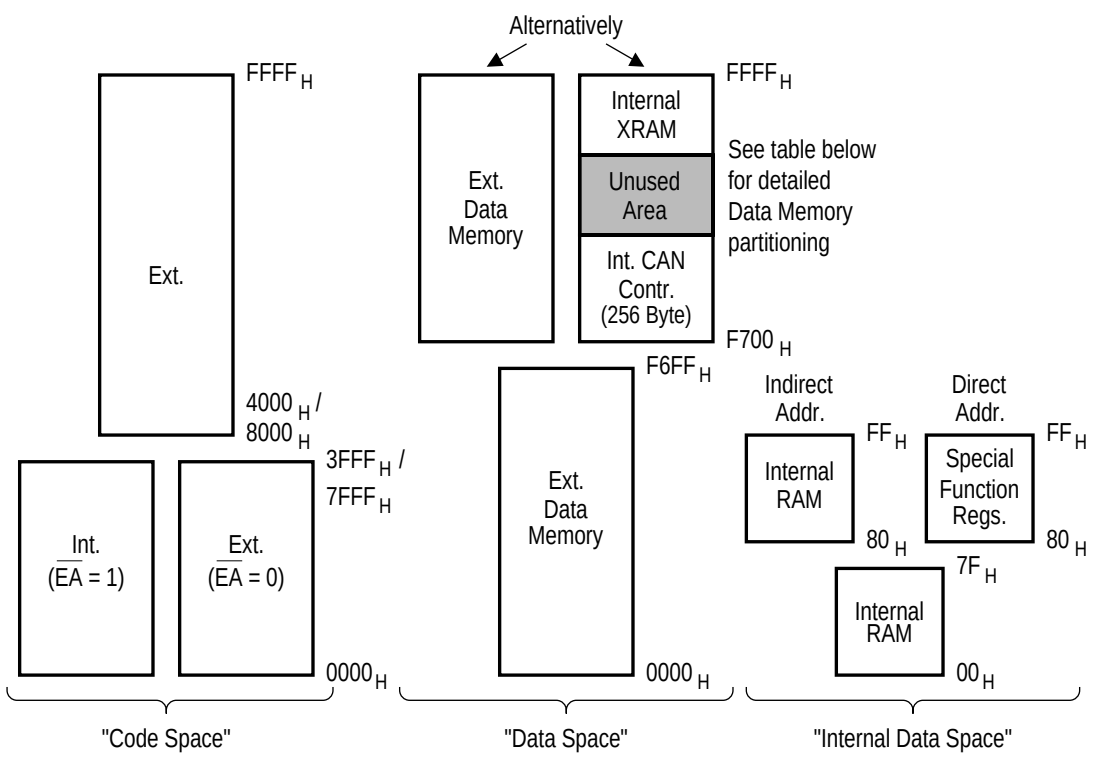
*) I = Input
O = Output

Memory Organization

The C505 CPU manipulates operands in the following four address spaces:

- On-chip program memory : 16K byte ROM (C505(C)(A)-2R) or
  32K byte ROM (C505A-4R/C505CA-4R) or
  32K byte OTP (C505A-4E/C505CA-4E)
- Totally up to 64K byte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- Internal XRAM data memory : 256 byte (C505/C505C)
  1K byte (C505A/C505CA)
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C505 versions.



"Data Space" $F700_H$ to $FFFF_H$:

Device	CAN Area	Unused Area	XRAM Area
C505	–	$F700_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505C	$F700_H$–$F7FF_H$	$F800_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505A	–	$F700_H$–$FBFF_H$	$FC00_H$–$FFFF_H$
C505CA	$F700_H$–$F7FF_H$	$F800_H$–$FBFF_H$	$FC00_H$–$FFFF_H$

Figure 5
C505 Memory Map Memory Map

Special Function Registers

The registers, except the program counter and the four general purpose register banks, reside in the special function register area. The special function register area consists of two portions : the standard special function register area and the mapped special function register area. Five special function register of the C505 (PCON1,P1ANA, VR0, VR1, VR2) are located in the mapped special function register area. For accessing the mapped special function register area, bit RMAP in special function register SYSCON must be set. All other special function registers are located in the standard special function register area which is accessed when RMAP is cleared (“0“).

The registers and data locations of the CAN controller (CAN-SFRs) are located in the external data memory area at addresses $F700_H$ to $F7FF_H$..

Special Function Register SYSCON (Address $B1_H$) **Reset Value : $XX100X01_B$**
(C505CA only) **Reset Value : $XX100001_B$**

Bit No.	MSB 7	6	5	4	3	2	1	LSB 0	
$B1_H$	–	–	EALE	RMAP	CMOD	CSWO 1)	XMAP1	XMAP0	SYSCON

The functions of the shaded bits are not described here.
1) This bit is only available in the C505CA.

Bit	Function
RMAP	Special function register map bit RMAP = 0 : The access to the non-mapped (standard) special function register area is enabled. RMAP = 1 : The access to the mapped special function register area is enabled.
CSWO	CAN Controller switch-off bit CSWO = 0 : CAN Controller is enabled (default after reset). CSWO = 1 : CAN Controller is switched off.

As long as bit RMAP is set, mapped special function register area can be accessed. This bit is not cleared by hardware automatically. Thus, when non-mapped/mapped registers are to be accessed, the bit RMAP must be cleared/set respectively by software.

All SFRs with addresses where address bits 0-2 are 0 (e.g. 80_H, 88_H, 90_H, 98_H, ..., $F8_H$, FF_H) are bitaddressable.

The 52 special function registers (SFRs) in the standard and mapped SFR area include pointers and registers that provide an interface between the CPU and the other on-chip peripherals. The SFRs of the C505 are listed in **Table 3** and **Table 4**. In **Table 3** they are organized in groups which refer to the functional blocks of the C505. The CAN-SFRs (applicable for the C505C and C505CA only) are also included in **Table 3**. **Table 4** illustrates the contents of the SFRs in numeric order of their addresses. **Table 5** list the CAN-SFRs in numeric order of their addresses.

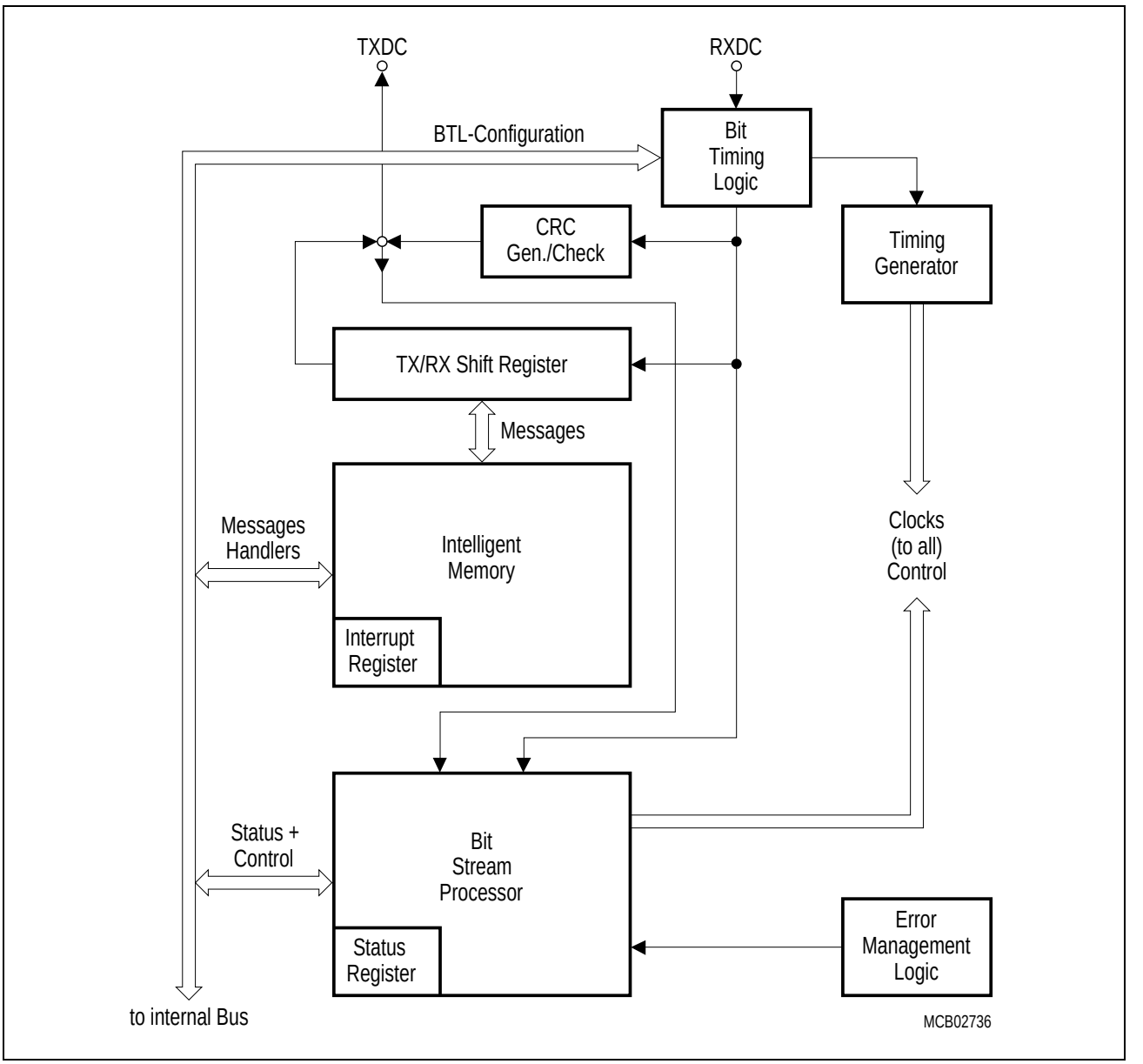


Figure 15
CAN Controller Block Diagram

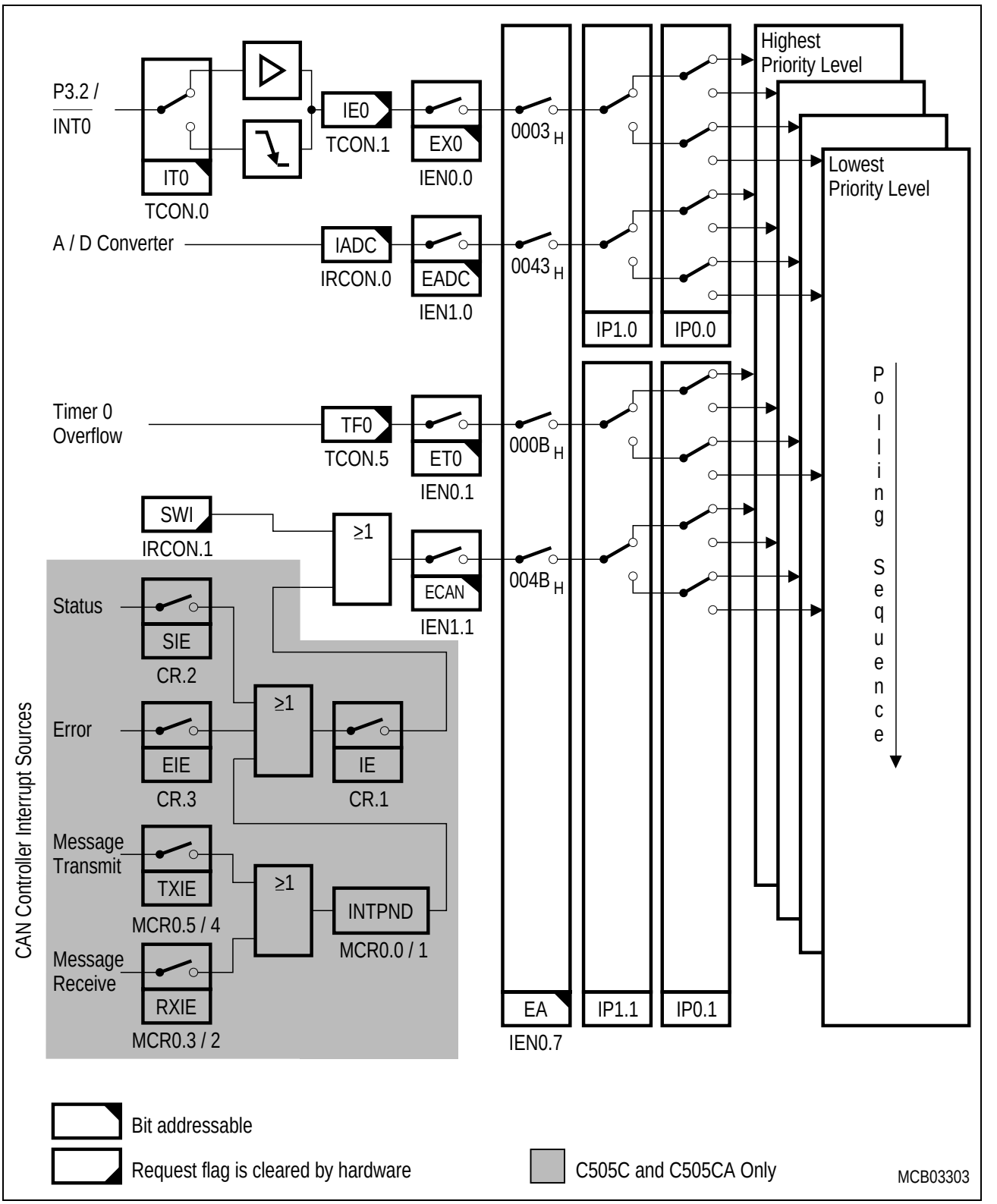


Figure 21
Interrupt Structure, Overview Part 1

*Note: Each of the 15 CAN controller message objects (C505C and C505CA only), shown in the shaded area of **Figure 21** provides the bits/flags.*

Pin Configuration in Programming Mode

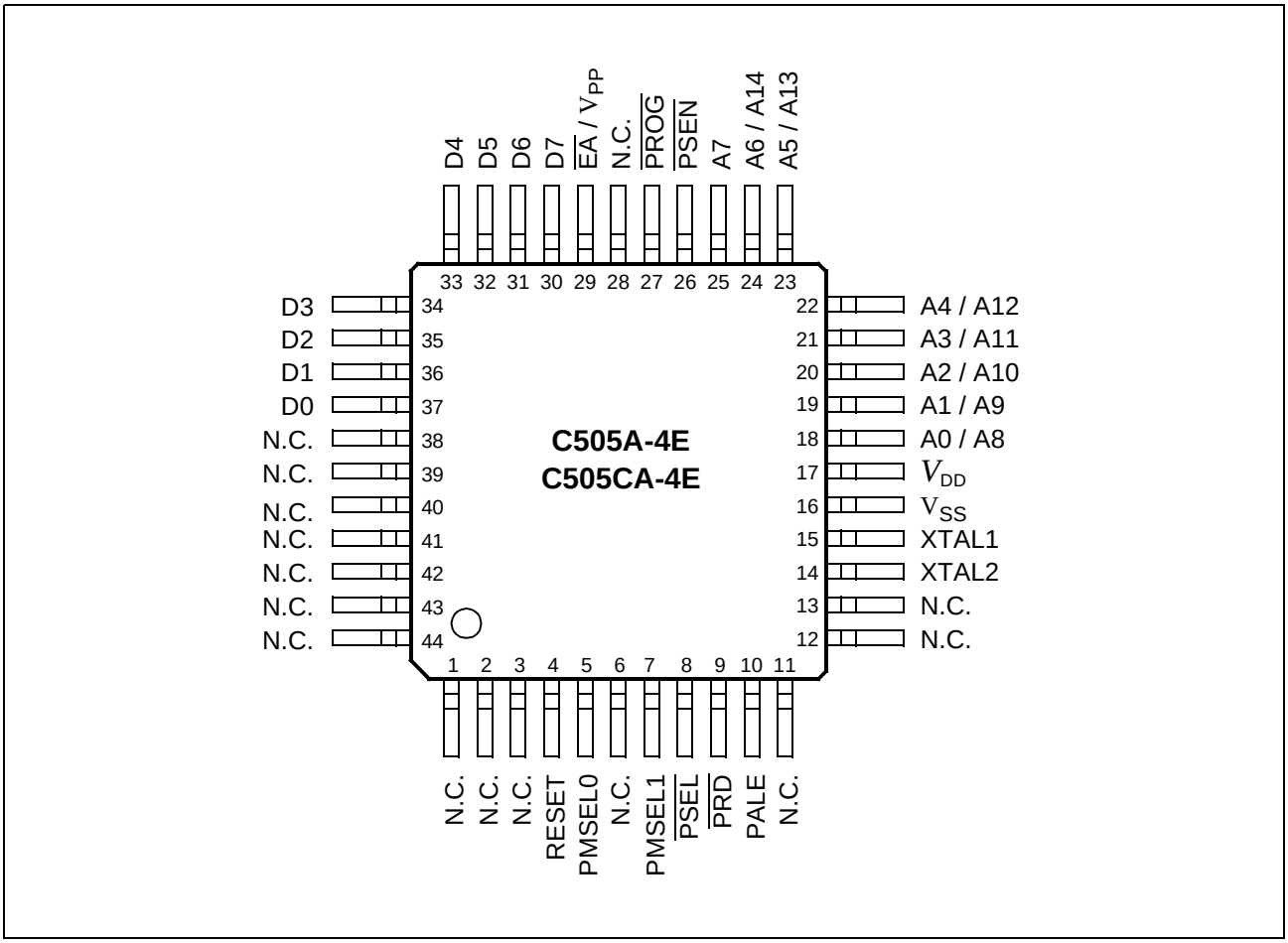


Figure 27
P-MQFP-44 Pin Configuration of the C505A-4E/C505CA-4E in Programming Mode (Top View)

The following **Table 11** contains the functional description of all C505A-4E/C505CA-4E pins which are required for OTP memory programming.

Table 11
Pin Definitions and Functions in Programming Mode

<table>
<tr><th>Symbol</th><th>Pin Number</th><th>I/O *)</th><th>Function</th></tr>
<tr><td>RESET</td><td>4</td><td>I</td><td>Reset
This input must be at static “1“ (active) level during the whole programming mode.</td></tr>
<tr><td>PMSEL0
PMSEL1</td><td>5
7</td><td>I
I</td><td>Programming mode selection pins
These pins are used to select the different access modes in programming mode. PMSEL1,0 must satisfy a setup time to the rising edge of PALE. When the logic level of PMSEL1,0 is changed, PALE must be at low level.
<table>
<tr><th>PMSEL1</th><th>PMSEL0</th><th>Access Mode</th></tr>
<tr><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>Read version bytes</td></tr>
<tr><td>1</td><td>0</td><td>Program/read lock bits</td></tr>
<tr><td>1</td><td>1</td><td>Program/read OTP memory byte</td></tr>
</table></td></tr>
<tr><td>$\overline{\text{PSEL}}$</td><td>8</td><td>I</td><td>Basic programming mode select
This input is used for the basic programming mode selection and must be switched according Figure 28.</td></tr>
<tr><td>$\overline{\text{PRD}}$</td><td>9</td><td>I</td><td>Programming mode read strobe
This input is used for read access control for OTP memory read, Version Register read, and lock bit read operations.</td></tr>
<tr><td>PALE</td><td>10</td><td>I</td><td>Programming address latch enable
PALE is used to latch the high address lines. The high address lines must satisfy a setup and hold time to/from the falling edge of PALE. PALE must be at low level when the logic level of PMSEL1,0 is changed.</td></tr>
<tr><td>XTAL2</td><td>14</td><td>O</td><td>XTAL2
Output of the inverting oscillator amplifier.</td></tr>
<tr><td>XTAL1</td><td>15</td><td>I</td><td>XTAL1
Input to the oscillator amplifier.</td></tr>
<tr><td>V_{SS}</td><td>16</td><td>–</td><td>Circuit ground potential
must be applied in programming mode.</td></tr>
<tr><td>V_{DD}</td><td>17</td><td>–</td><td>Power supply terminal
must be applied in programming mode.</td></tr>
</table>

*) I = Input
O = Output

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	– 65	150	°C	–
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	– 0.5	6.5	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	– 0.5	V_{DD} + 0.5	V	–
Input current on any pin during overload condition		– 10	10	mA	–
Absolute sum of all input currents during overload condition			| 100 mA |	mA	–
Power dissipation	P_{DISS}		1	W	–

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for longer periods may affect device reliability. During absolute maximum rating overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

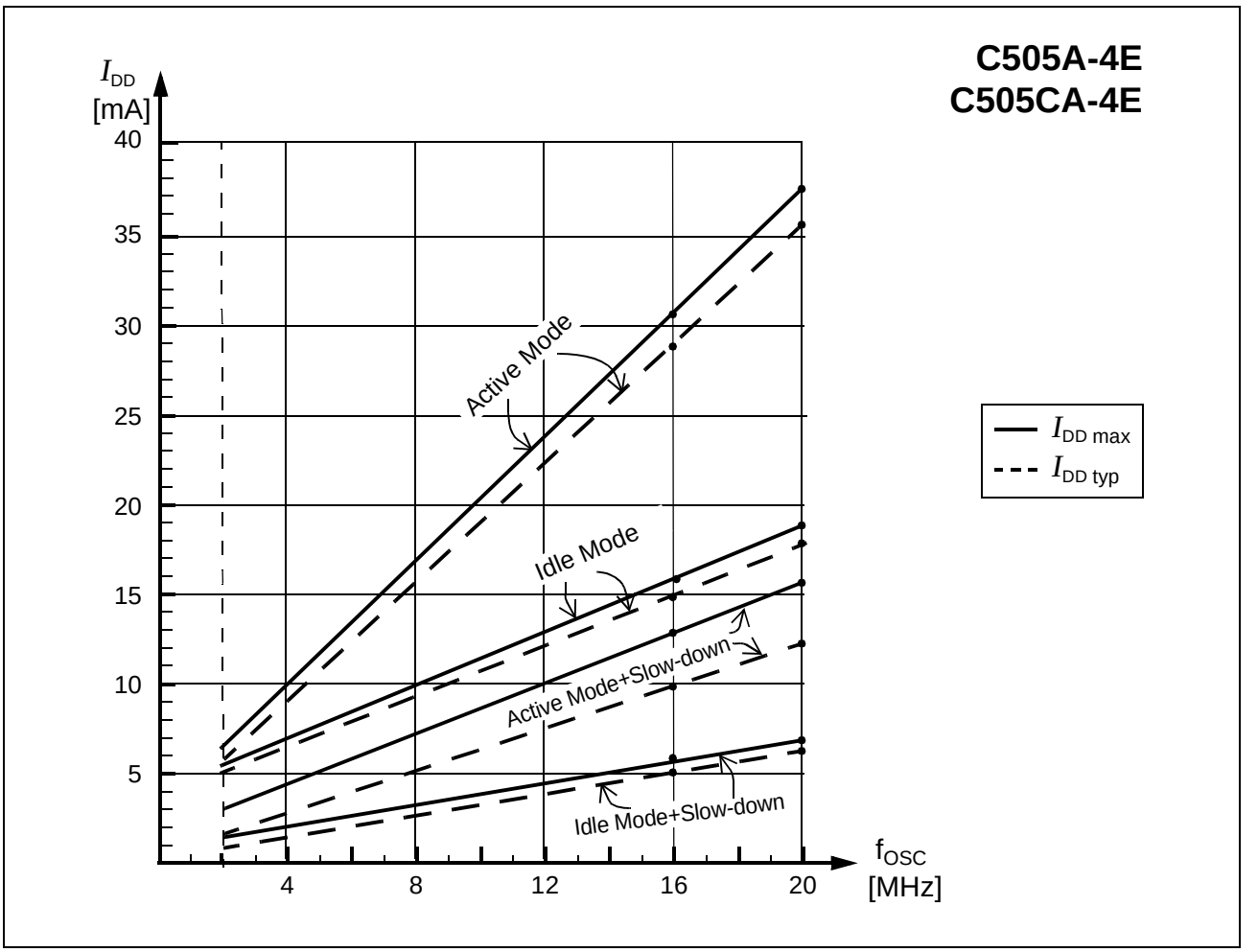


Figure 30
I_{DD} Diagram of C505A-4E and C505CA-4E

C505A-4E/C505CA-4E : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.63 * f_{OSC} + 2.6$ $1.74 * f_{OSC} + 2.8$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.69 * f_{OSC} + 3.9$ $0.74 * f_{OSC} + 4.1$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.6 * f_{OSC} + 0.3$ $0.7 * f_{OSC} + 1.6$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.3 * f_{OSC} + 0.3$ $0.3 * f_{OSC} + 0.8$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

A/D Converter Characteristics of C505A and C505CA

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND}	V_{AREF}	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	384 x t_{IN} 192 x t_{IN} 96 x t_{IN} 48 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{DD}-0.5V 4)
		–	± 4	LSB	V_{SS} < V_{AIN} < V_{DD}+0.5V V_{DD} - 0.5 V < V_{AIN} < V_{DD} 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 250 - 0.25	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 0.25	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	384 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	192 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	96 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	48 x t_{IN}

Further timing conditions : t_{ADC} min = 500 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 16 MHz Duty Cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 16 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	62.5	62.5	62.5	500	ns
High time	TCL_H	25	–	25	CLP - TCL_L	ns
Low time	TCL_L	25	–	25	CLP - TCL_H	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 - 25 / CLP	–
Clock cycle	TCL	25	37.5	CLP * DC_{min}	CLP * DC_{max}	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

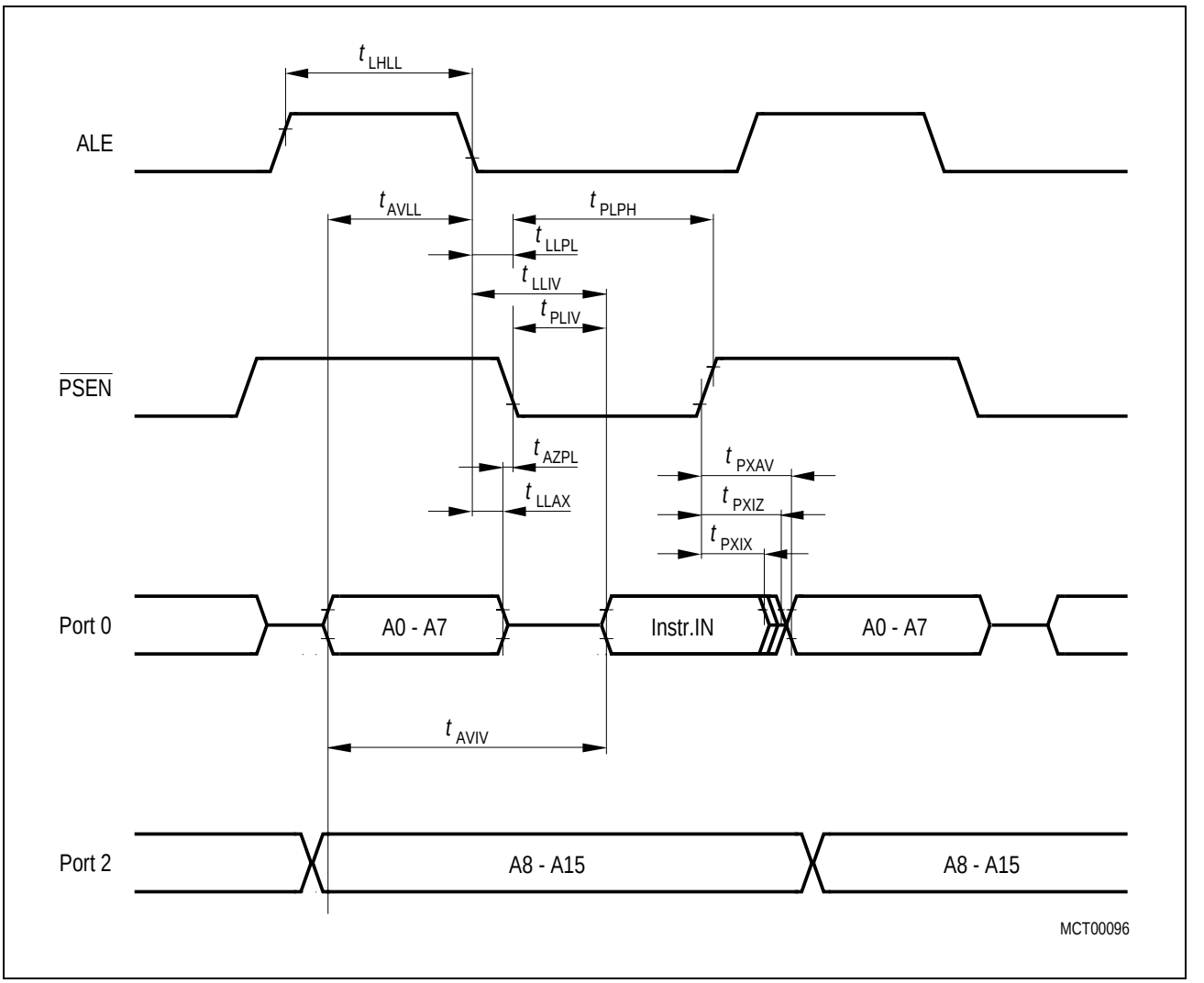


Figure 32
Program Memory Read Cycle

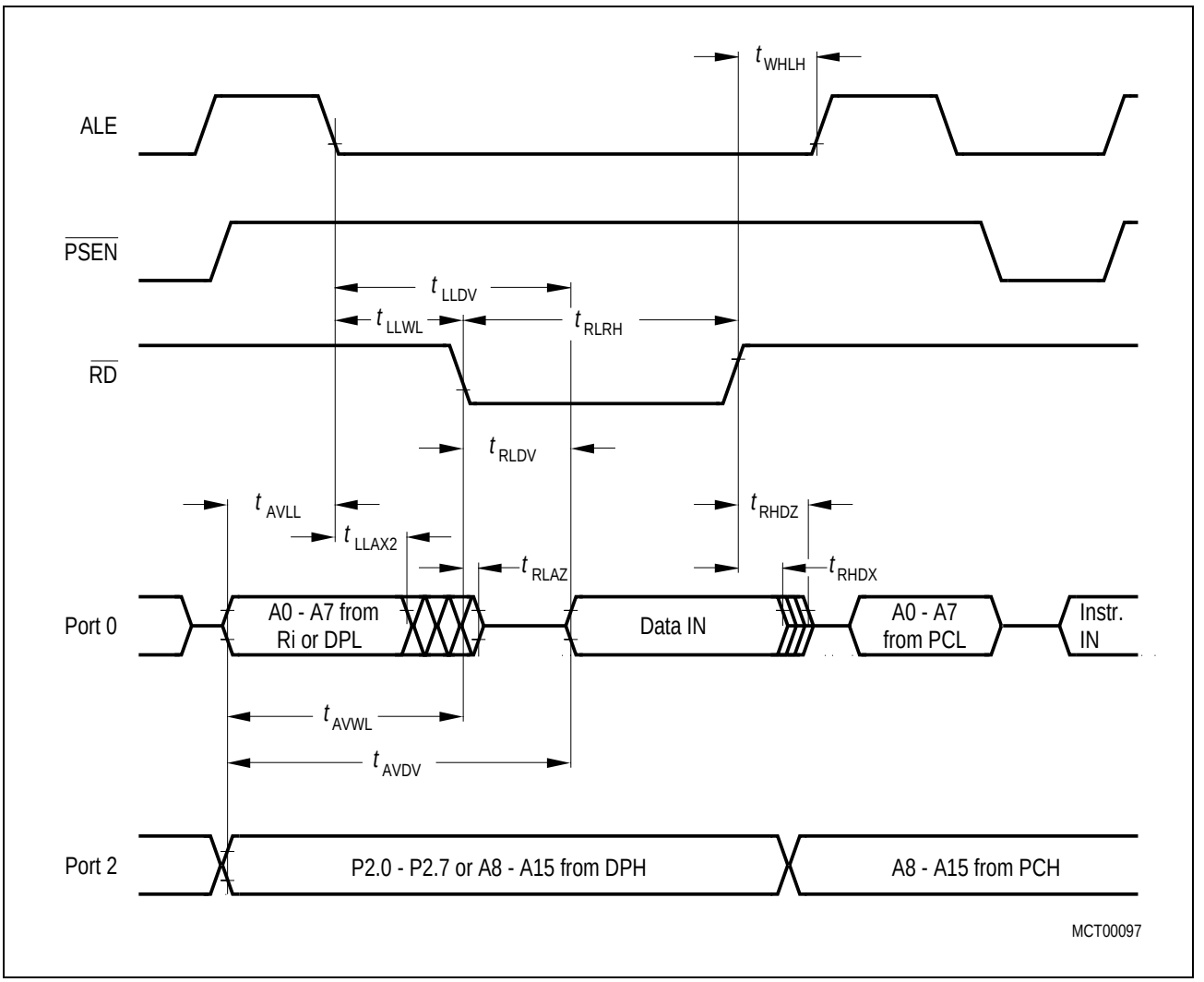


Figure 33
Data Memory Read Cycle

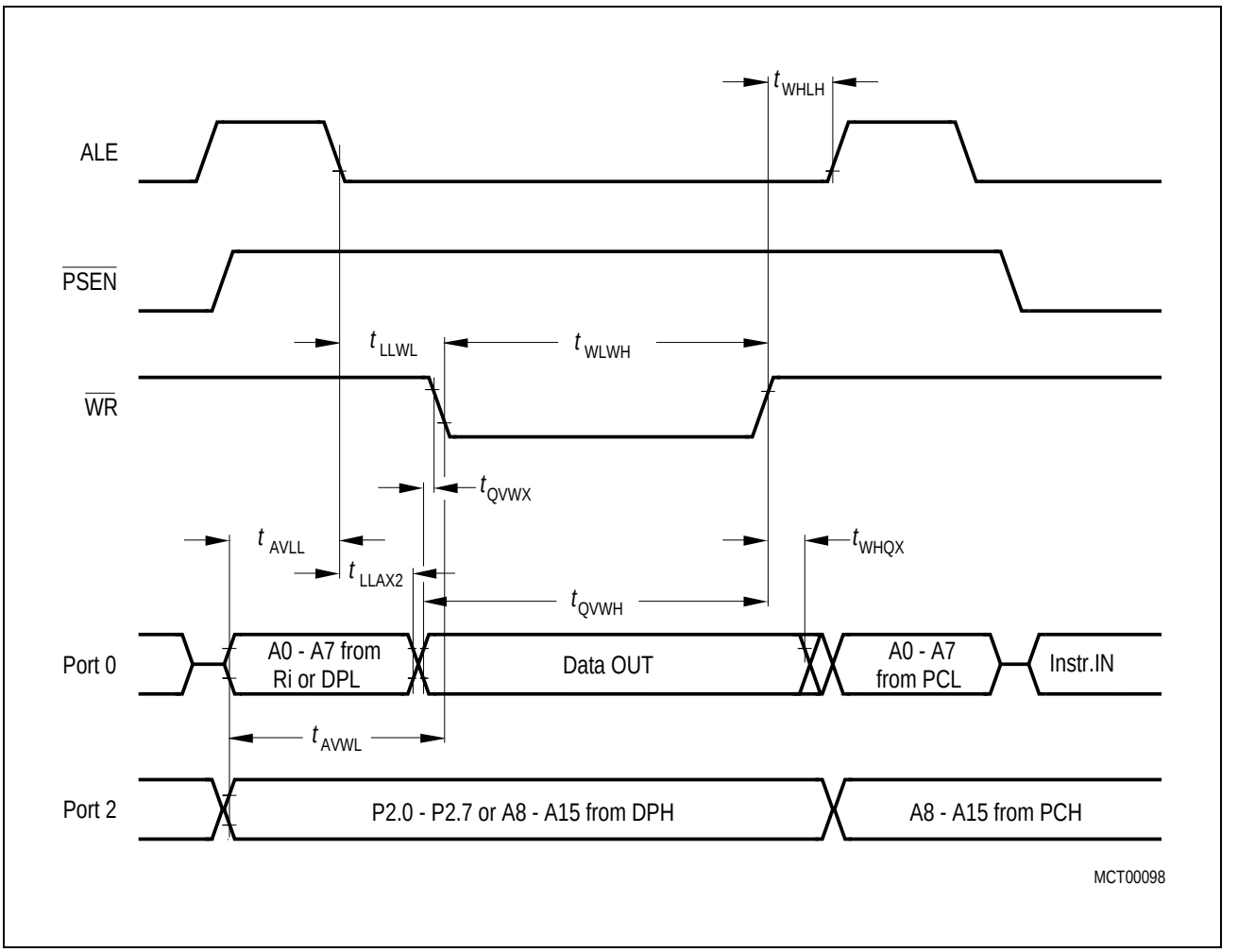


Figure 34
Data Memory Write Cycle

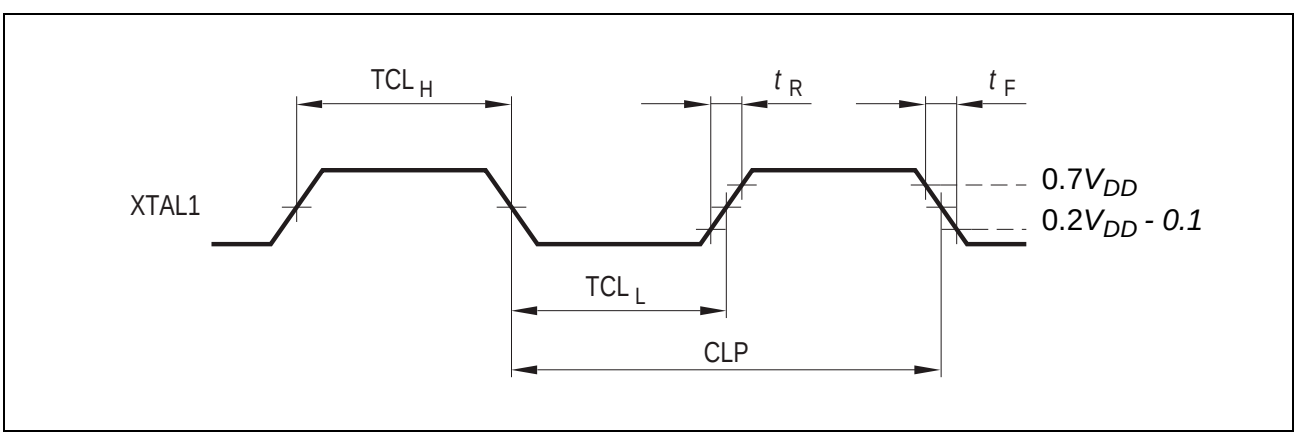
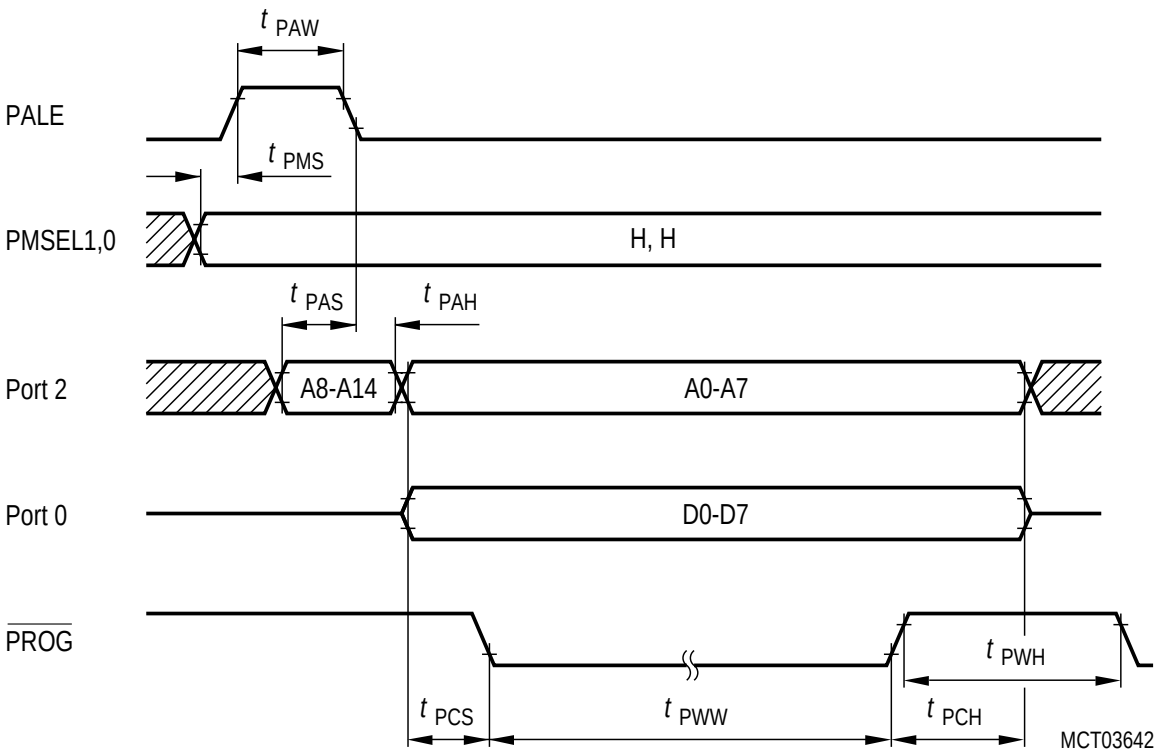


Figure 35
External Clock Drive on XTAL1



Notes: $\overline{PRD}$ must be high during a programming write cycle.

Figure 36
Programming Code Byte - Write Cycle Timing

ROM/OTP Verification Characteristics for C505 (cont'd)

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz

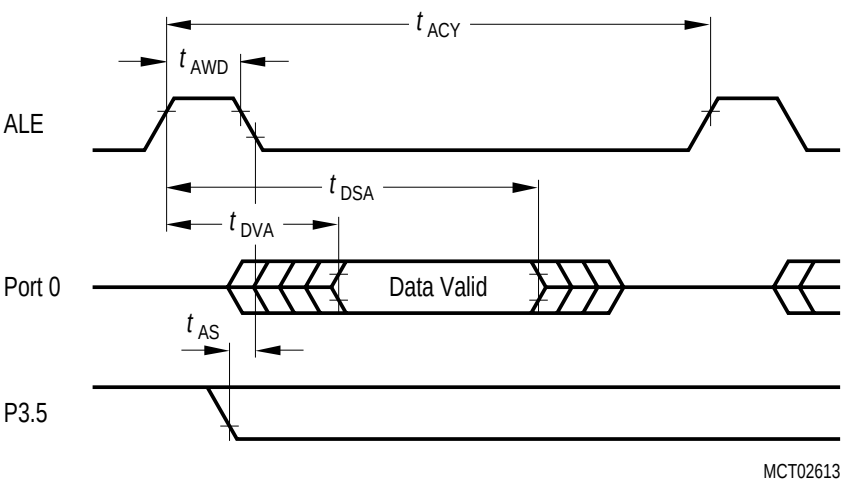


Figure 41
ROM/OTP Verification Mode 2