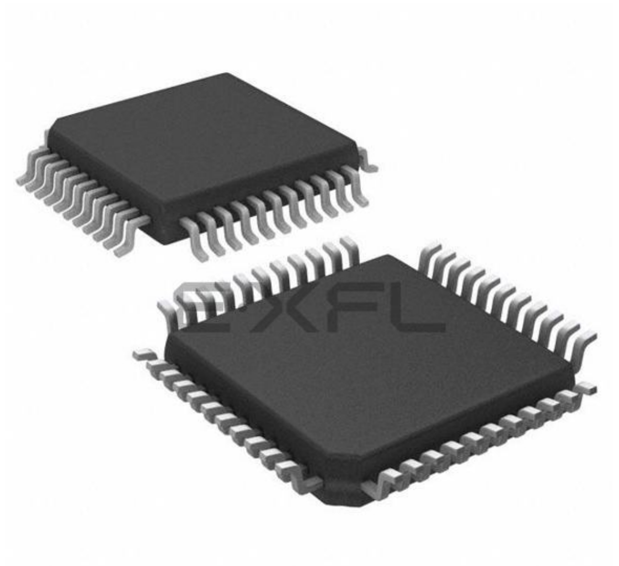

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505ca4emcakxqma1

C505/C505C/C505A/C505CA Data Sheet **Revision History :**		**Current Version : 2000-12**
Previous Releases :		08.00, 06.00, 07.99, 12.97
Page (in previous version	Page (in current version)	Subjects (major changes since last revision)
24	24	Version register VR2 for C505A-4R/C505CA-4R BB step is updated.

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8-Bit Single-Chip Microcontroller
C500 Family

C505/C505C/C505A/
C505CA

Advance Information

- Fully compatible to standard 8051 microcontroller
- Superset of the 8051 architecture with 8 datapointers
- Up to 20 MHz operating frequency
  - 375 ns instruction cycle time @16 MHz
  - 300 ns instruction cycle time @20 MHz (50 % duty cycle)
- On-chip program memory (with optional memory protection)
  - C505(C)(A)-2R : 16K byte on-chip ROM
  - C505A-4R/C505CA-4R: 32K byte on-chip ROM
  - C505A-4E/C505CA-4E: 32K byte on-chip OTP
  - alternatively up to 64k byte external program memory
- 256 byte on-chip RAM
- On-chip XRAM
  - C505/C505C : 256 byte
  - C505A/C505CA : 1K byte

(more features on next page)

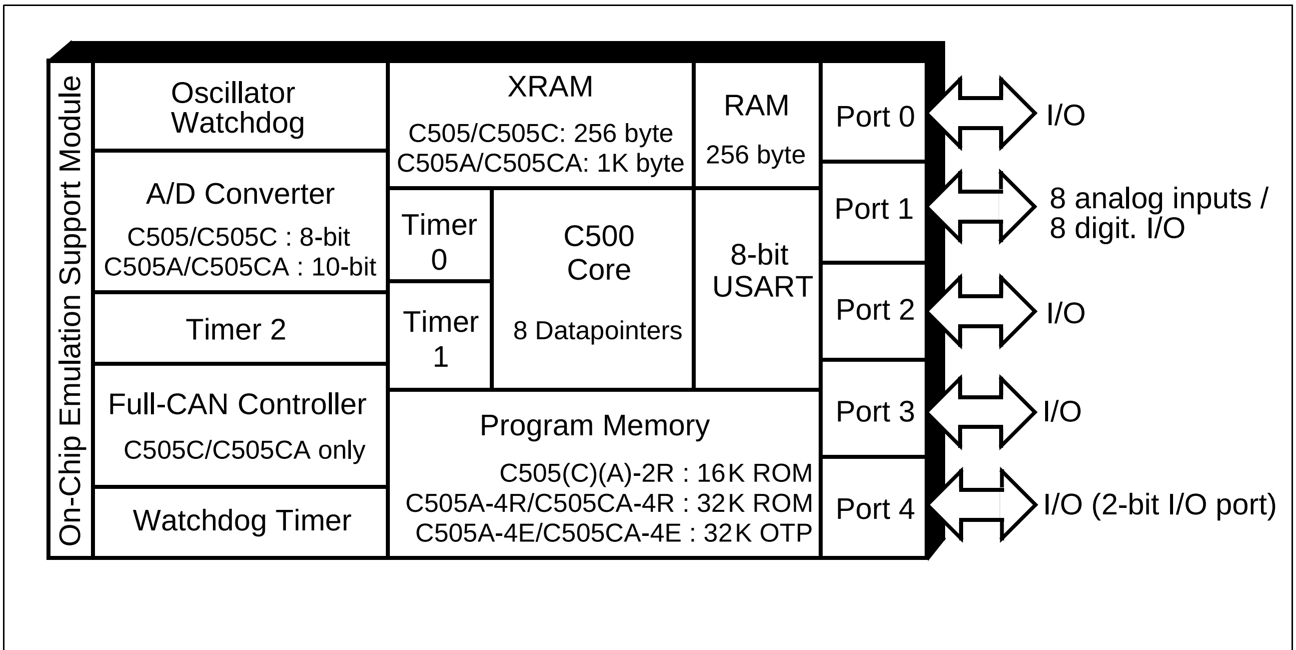


Figure 1
C505 Functional Units

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P4.0 P4.1	6 28	I/O I/O	**Port 4** is a 2-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to the secondary function RXDC must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows (C505C and C505CA only) : P4.0 / TXDC Transmitter output of CAN controller P4.1 / RXDC Receiver input of CAN controller
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of the etxernal clock signal of 50 % should be maintained. Minimum and maximum high and low times as well as rise/fall times specified in the AC characteristics must be observed.

*) I = Input
O = Output

Multiple Datapointers

As a functional enhancement to the standard 8051 architecture, the C505 contains eight 16-bit datapointers instead of only one datapointer. The instruction set uses just one of these datapointers at a time. The selection of the actual datapointer is done in the special function regsiter DPSEL. **Figure 8** illustrates the datapointer addressing mechanism.

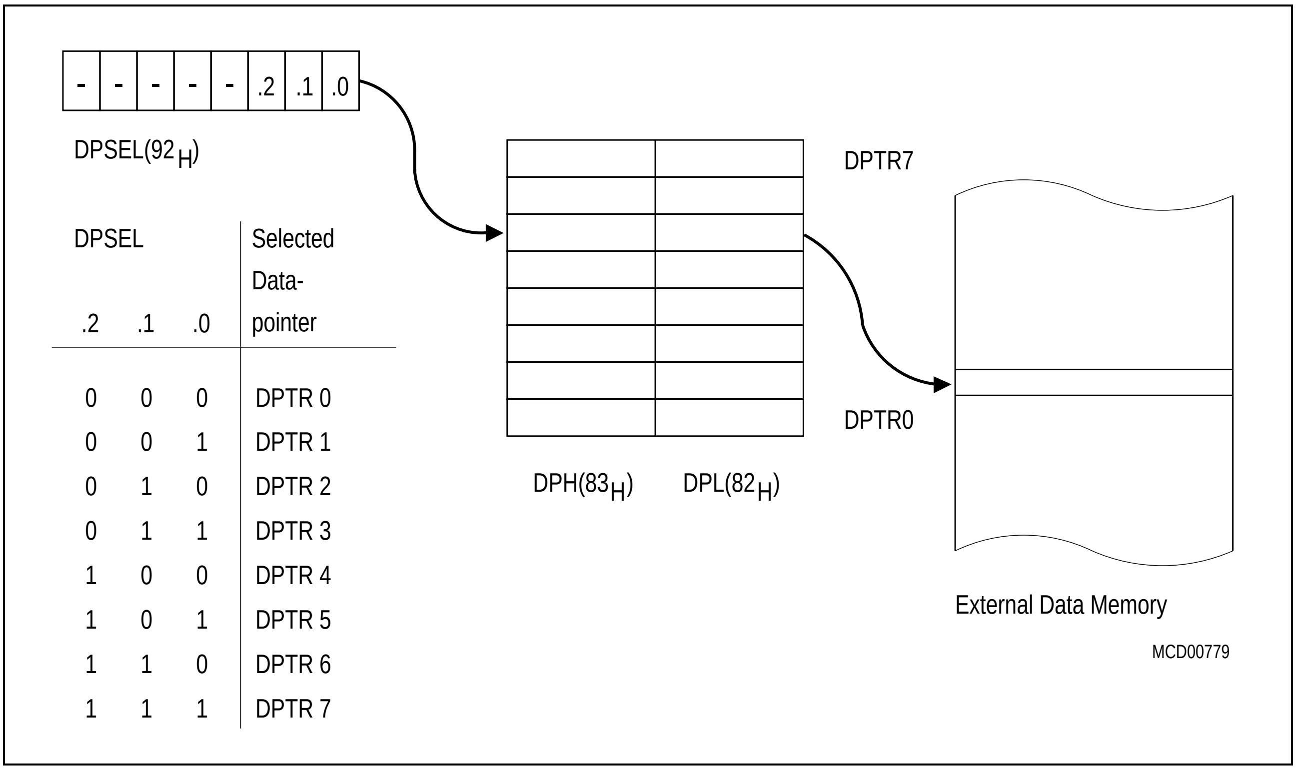


Figure 8
External Data Memory Addressing using Multiple Datapointers

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset 1)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$ 2)	P3	FF_H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD
$B1_H$	SYSCON 3)	$XX10\text{-}0X01_B$	–	–	EALE	RMAP	CMOD	–	XMAP1	XMAP0
$B1_H$	SYSCON 4)	$XX10\text{-}0001_B$	–	–	EALE	RMAP	CMOD	CSWO	XMAP1	XMAP0
$B8_H$ 2)	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	ECAN	EADC
$B9_H$	IP1	$XX00\text{-}0000_B$	–	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	.1	.0
$C0_H$ 2)	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC
$C1_H$	CCEN	00_H	COCA H3	COCAL 3	COCA H2	COCAL 2	COCA H1	COCAL 1	COCA H0	COCAL 0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$ 2)	T2CON	$00X0\text{-}0000_B$	T2PS	I3FR	–	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$ 2)	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$ 2)	ADCON0	$00X0\text{-}0000_B$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) C505 /C505C/C505A only
4) C505CA only

Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1's to all 0's sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode : In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode : In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode : In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2 : Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1's to all 0's, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

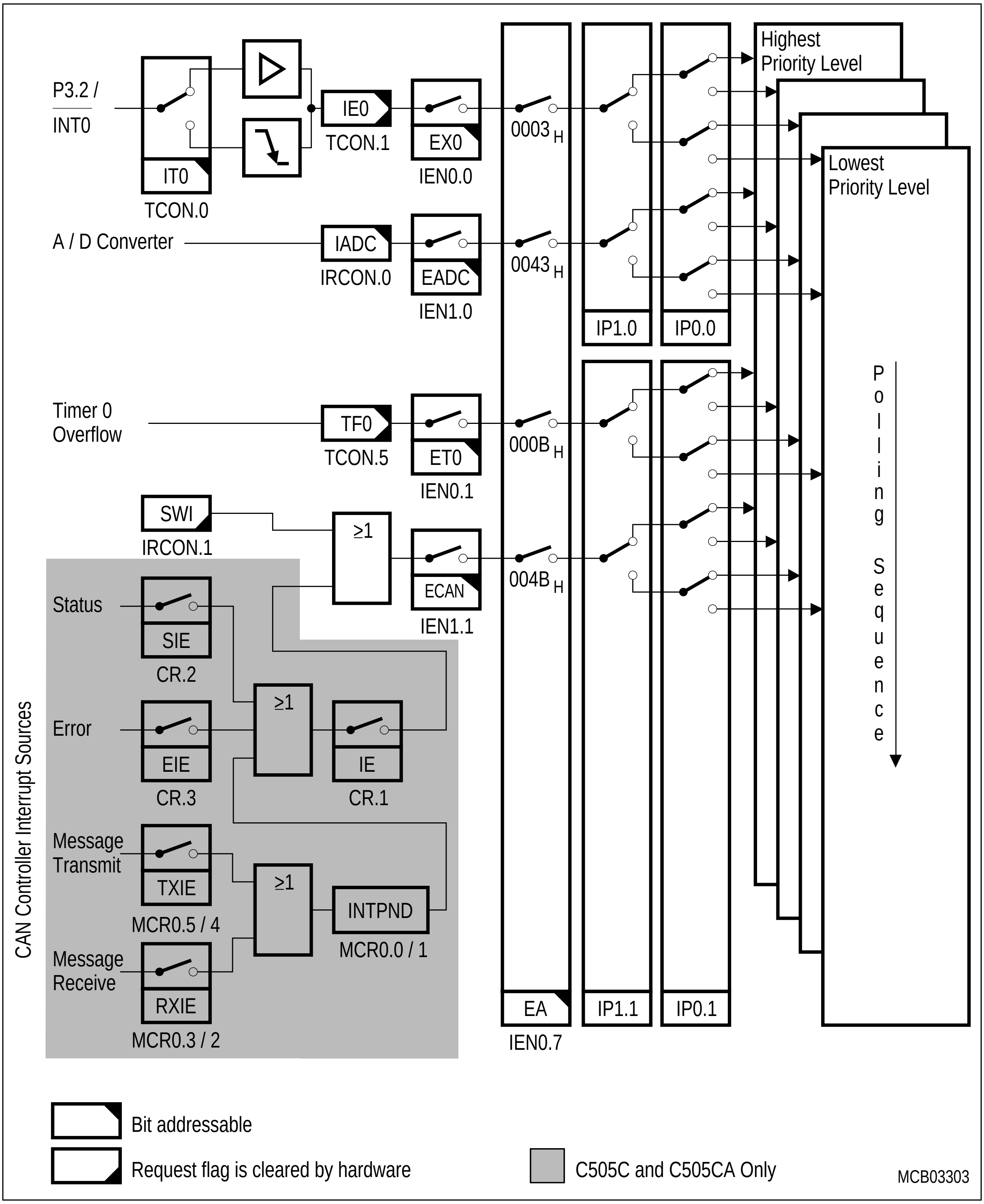


Figure 21
Interrupt Structure, Overview Part 1

Note: Each of the 15 CAN controller message objects (C505C and C505CA only), shown in the shaded area of ***Figure 21*** *provides the bits/flags.*

Fail Save Mechanisms

The C505 offers enhanced fail safe mechanisms, which allow an automatic recovery from software upset or hardware failure :

– a programmable watchdog timer (WDT), with variable time-out period from 192 µs up to approx. 393.2 ms at 16 MHz (314.5 ms at 20 MHz).
– an oscillator watchdog (OWD) which monitors the on-chip oscillator and forces the microcontroller into reset state in case the on-chip oscillator fails; it also provides the clock for a fast internal reset after power-on.

The watchdog timer in the C505 is a 15-bit timer, which is incremented by a count rate of $f_{OSC}/12$ upto $f_{OSC}/192$. The system clock of the C505 is divided by two prescalers, a divide-by-two and a divide-by-16 prescaler. For programming of the watchdog timer overflow rate, the upper 7 bits of the watchdog timer can be written. **Figure 24** shows the block diagram of the watchdog timer unit.

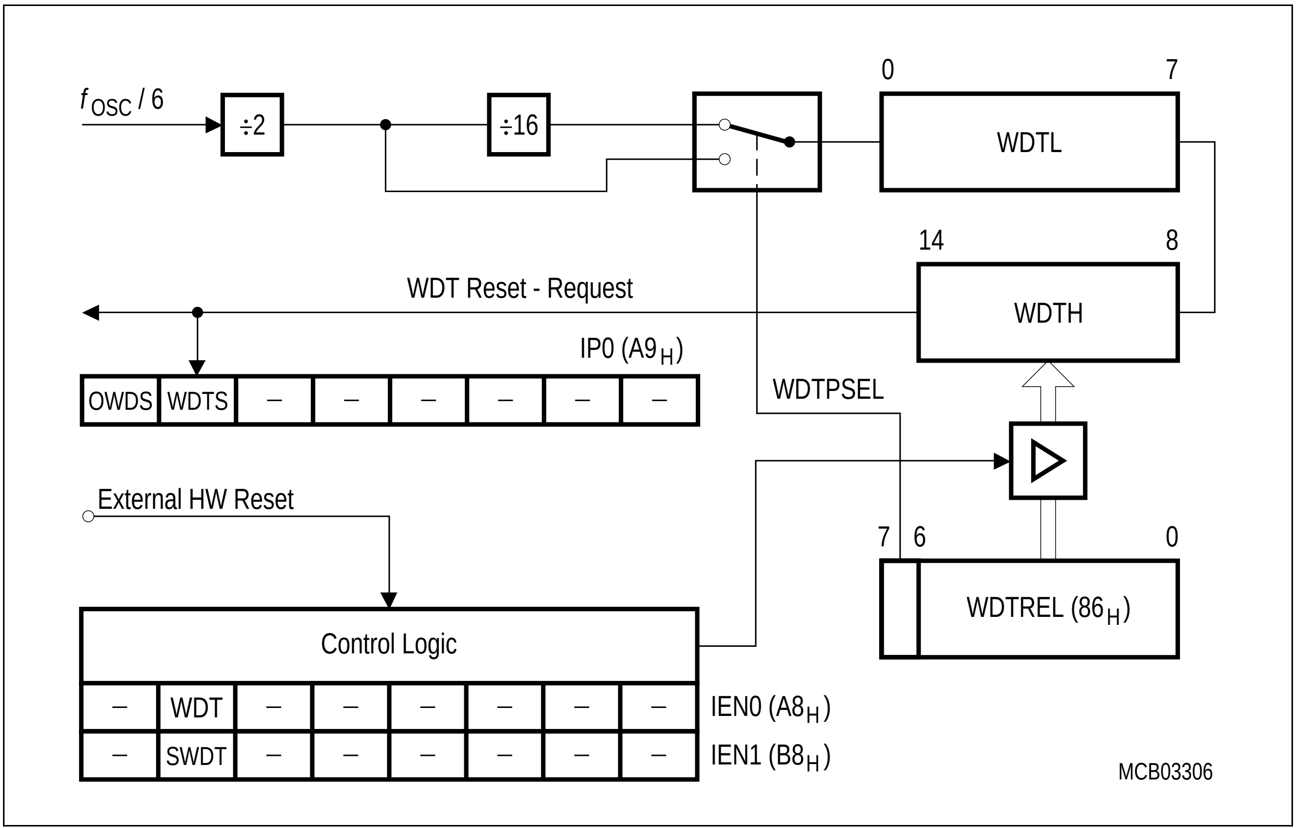


Figure 24
Block Diagram of the Programmable Watchdog Timer

The watchdog timer can be started by software (bit SWDT in SFR IEN1) but it cannot be stopped during active mode of the device. If the software fails to refresh the running watchdog timer an internal reset will be initiated on watchdog timer overflow. For refreshing of the watchdog timer the content of the SFR WDTREL is transfered to the upper 7-bit of the watchdog timer. The refresh sequence consists of two consequtive instructions which set the bits WDT and SWDT each. The reset cause (external reset or reset caused by the watchdog) can be examined by software (flag WDTS). It must be noted, however, that the watchdog timer is halted during the idle mode and power down mode of the processor.

Table 12
Access Modes Selection

Access Mode	$\overline{EA}$/ V_{PP}	$\overline{PROG}$	$\overline{PRD}$	PMSEL 1	PMSEL 0	Address (Port 2)	Data (Port 0)
Program OTP memory byte	V_{PP}		H	H	H	A0-7 A8-14	D0-7
Read OTP memory byte	V_{IH}	H					
Program OTP lock bits	V_{PP}		H	H	L	–	D1,D0 see Table 13
Read OTP lock bits	V_{IH}	H					
Read OTP version byte	V_{IH}	H		L	H	Byte addr. of sign. byte	D0-7

Lock Bits Programming / Read

The C505A-4E/C505CA-4E has two programmable lock bits which, when programmed according to **Table 13**, provide four levels of protection for the on-chip OTP code memory. The state of the lock bits can also be read.

Table 13
Lock Bit Protection Types

Lock Bits at D1,D0: D1	D0	Protection Level	Protection Type
1	1	Level 0	The OTP lock feature is disabled. During normal operation of the C505A-4E/C505CA-4E, the state of the $\overline{EA}$ pin is not latched on reset.
1	0	Level 1	During normal operation of the C505A-4E/C505CA-4E, MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory. $\overline{EA}$ is sampled and latched on reset. An OTP memory read operation is only possible using the ROM/OTP verification mode 2 for protection level 1. Further programming of the OTP memory is disabled (reprogramming security).
0	1	Level 2	Same as level 1, but also OTP memory read operation using OTP verification mode is disabled.
0	0	Level 3	Same as level 2; but additionally external code execution by setting $\overline{EA}$=low during normal operation of the C505A-4E/ C505CA-4E is no more possible. External code execution, which is initiated by an internal program (e.g. by an internal jump instruction above the ROM boundary), is still possible.

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode, $f_{osc\ max}$ = 20 MHz
		2	5.5	V	PowerDown mode
Ground voltage	V_{SS}	0		V	Reference voltage
Ambient temperature				°C	–
SAB-C505	T_A	0	70		
SAF-C505	T_A	-40	85		
SAH-C505	T_A	-40	110		
SAK-C505	T_A	-40	125		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND} -0.2	V_{AREF} +0.2	V	–
XTAL clock	f_{OSC}	2	20 (with 50% duty cycle)	MHz	1)

1) For the extended temperature range -40 °C to 110 °C (SAH) and -40 °C to 125 °C (SAK), the devices C505-2R, C505-L, C505C-2R and C505C-L have the max. operating frequency of 16MHz with 50% clock duty cycle.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C505 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the C505 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective characteristics to the C505.

Power Supply Currents

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[12]	max.[13]		
C505 / C505C	Active Mode	12 MHz 20 MHz	I_{DD} I_{DD}	19.3 31.3	27.0 39	mA	[7]
	Idle Mode	12 MHz 20 MHz	I_{DD} I_{DD}	10.3 16.2	13.0 21.0	mA	[8]
	Active Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.9 4.8	5.5 7.5	mA	[9]
	Idle Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.2 4.0	5.0 7.0	mA	[10]
	Power down mode		I_{PD}	10	50	µA	V_{DD} = 2..5.5 V [11]
C505A-4E /C505CA-4E	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	28.7 35.2	30.7 37.6	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	14.9 17.7	15.9 18.9	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	9.9 12.3	12.8 15.6	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.1 6.3	5.6 6.8	mA	[10]
	Power down mode		I_{PD}	5.6	20	µA	V_{DD} = 2..5.5 V [11]
C505A-4R / C505CA-4R /C505A-2R / C505CA-2R /C505A-L / C505CA-L	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	22.8 27.6	29.2 35.3	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	12.7 15.0	16.3 19.3	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	6.6 7.3	8.2 9.3	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.0 5.3	5.9 6.5	mA	[10]
	Power down mode		I_{PD}	5.3	30	µA	V_{DD} = 2..5.5 V [11]

Notes see **Page 60**

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} (max.) is tested at $-40 \le T_A \le 125$ °C ; $V_{DD} \le$ 5.5 V; $V_{AREF} \le V_{DD}$ + 0.1 V and $V_{SS} \le V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be $X000_H$ or $X3FF_H$, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result and the time for the calibration. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} is tested at V_{AREF} = 5.0 V, V_{AGND} = 0 V, V_{DD} = 4.9 V. It is guaranteed by design characterization for all other voltages within the defined voltage range.
   If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} -15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} -15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP - 50	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	TCL_{Lmin} -15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} -15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}- 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} -55	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	158	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	158	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	48	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	100	–	2 CLP+ TCL_{Hmin} - 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	51	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	200	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	200	–	4 CLP + TCL_{Hmin} -75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	73	103	CLP + TCL_{Lmin} - 15	CLP+ TCL_{Lmin}+ 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	95	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	TCL_{Hmin} - 15	TCL_{Hmin} + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	TCL_{Lmin} - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	163	–	3 CLP + TCL_{Lmin} - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	TCL_{Hmin} - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

AC Characteristics of Programming Mode (C505A-4E and C505CA-4E only)

V_{DD} = 5 V ± 10 %; V_{PP} = 11.5 V ± 5 %; T_A = 25 °C ± 10 °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PALE pulse width	t_{PAW}	35	–	ns
PMSEL setup to PALE rising edge	t_{PMS}	10	–	
Address setup to PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAS}	10	–	ns
Address hold after PALE, $\overline{PROG}$, or $\overline{PRD}$ falling edge	t_{PAH}	10	–	ns
Address, data setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PCS}	100	–	ns
Address, data hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PCH}	0	–	ns
PMSEL setup to $\overline{PROG}$ or $\overline{PRD}$	t_{PMS}	10	–	ns
PMSEL hold after $\overline{PROG}$ or $\overline{PRD}$	t_{PMH}	10	–	ns
$\overline{PROG}$ pulse width	t_{PWW}	100	–	µs
$\overline{PRD}$ pulse width	t_{PRW}	100	–	ns
Address to valid data out	t_{PAD}	–	75	ns
$\overline{PRD}$ to valid data out	t_{PRD}	–	20	ns
Data hold after $\overline{PRD}$	t_{PDH}	0	–	ns
Data float after $\overline{PRD}$	t_{PDF}	–	20	ns
$\overline{PROG}$ high between two consecutive $\overline{PROG}$ low pulses	t_{PWH1}	1	–	µs
$\overline{PRD}$ high between two consecutive $\overline{PRD}$ low pulses	t_{PWH2}	100		ns
XTAL clock period	t_{CLKP}	83.3	500	ns

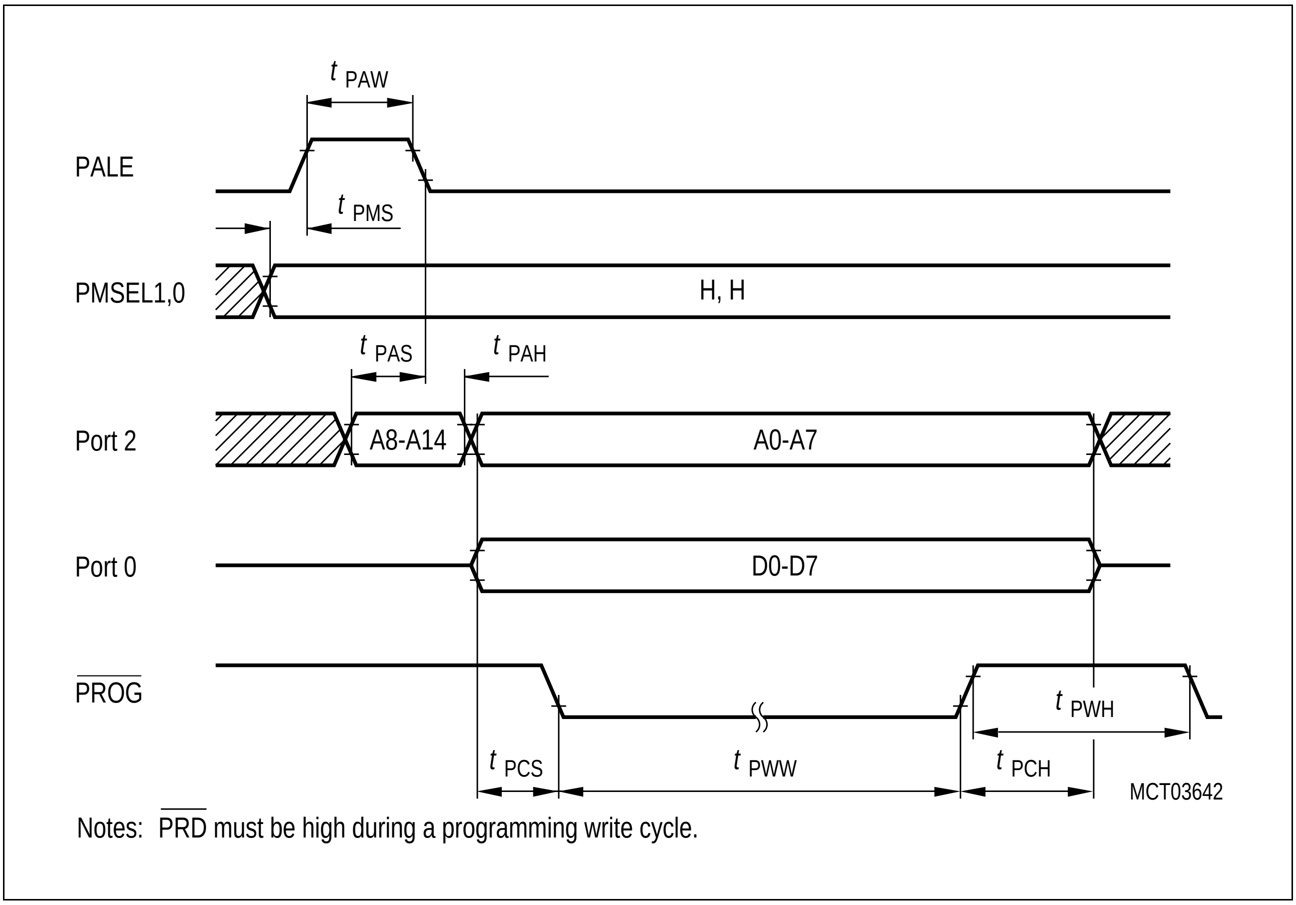


Figure 36
Programming Code Byte - Write Cycle Timing

ROM/OTP Verification Characteristics for C505 (cont'd)

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz

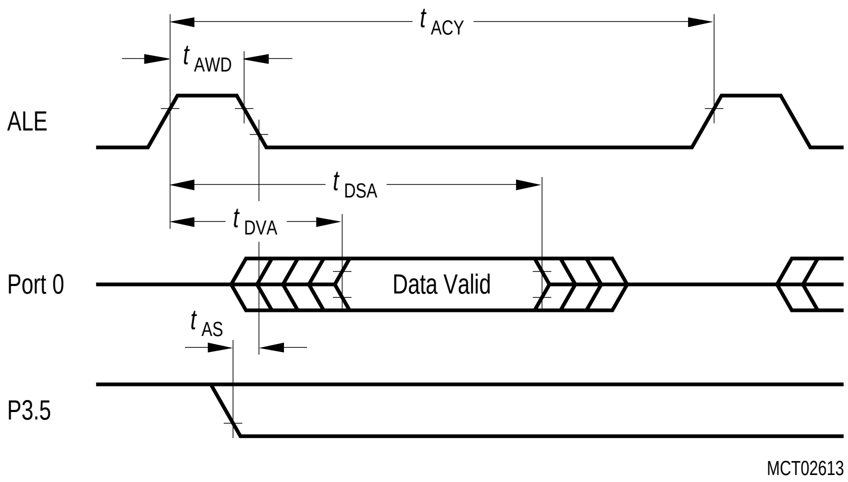
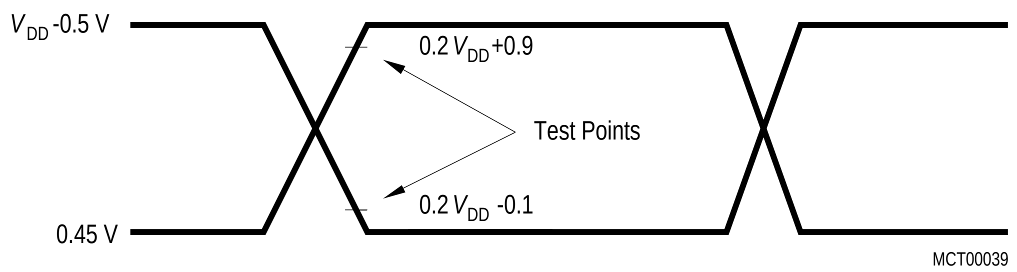
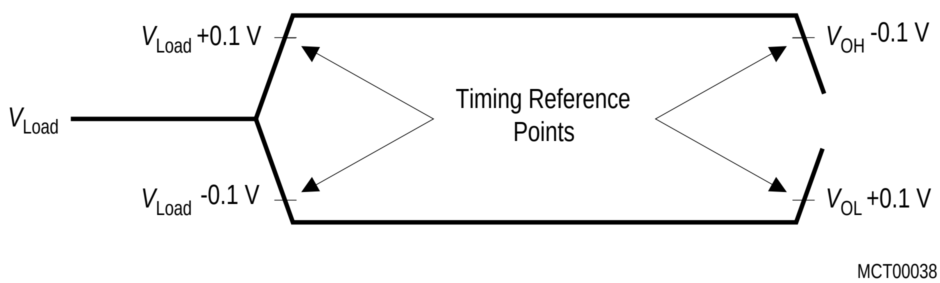


Figure 41
ROM/OTP Verification Mode 2



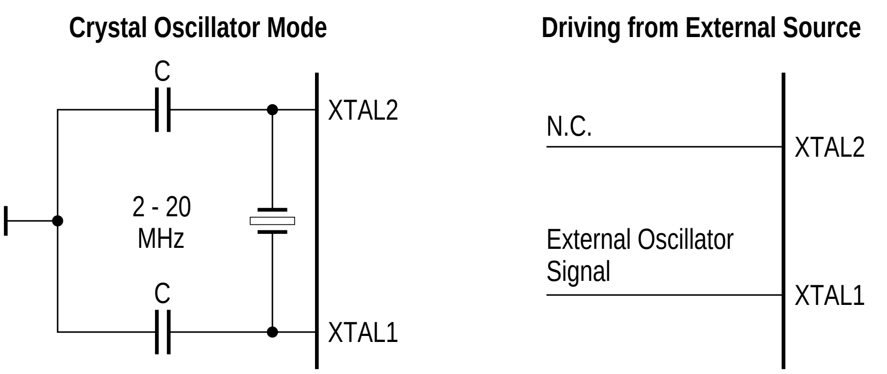
AC Inputs during testing are driven at V_{DD} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 42
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs.
$I_{OL}/I_{OH} \geq \pm 20$ mA

Figure 43
AC Testing : Float Waveforms



Crystal Mode: C = 20 pF ± 10 pF (incl. stray capacitance)

Figure 44
Recommended Oscillator Circuits for Crystal Oscillator

P-MQFP-44-2 (SMD)
(Plastic Metric Quad Flat Package)

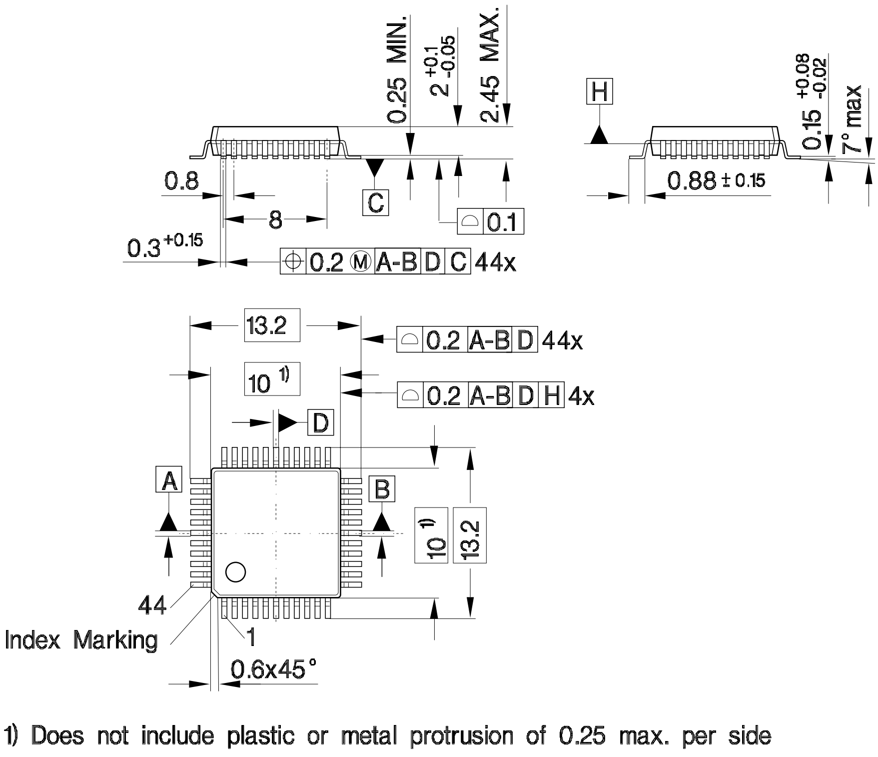


Figure 45
P-MQFP-44 Package Outline

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”

SMD = Surface Mounted Device

Dimensions in mm