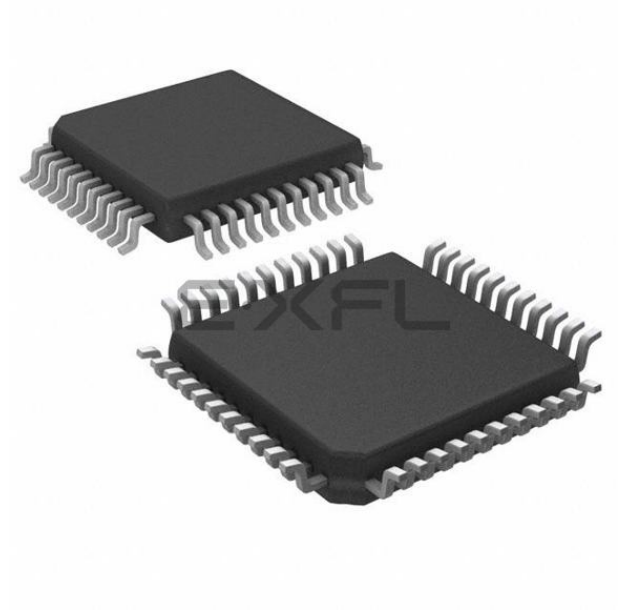
Infineon Technologies - C505CA4EMCAKXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505ca4emcakxuma1

Data Sheet, Dec. 2000

C505

C505C

C505A

C505CA

8-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

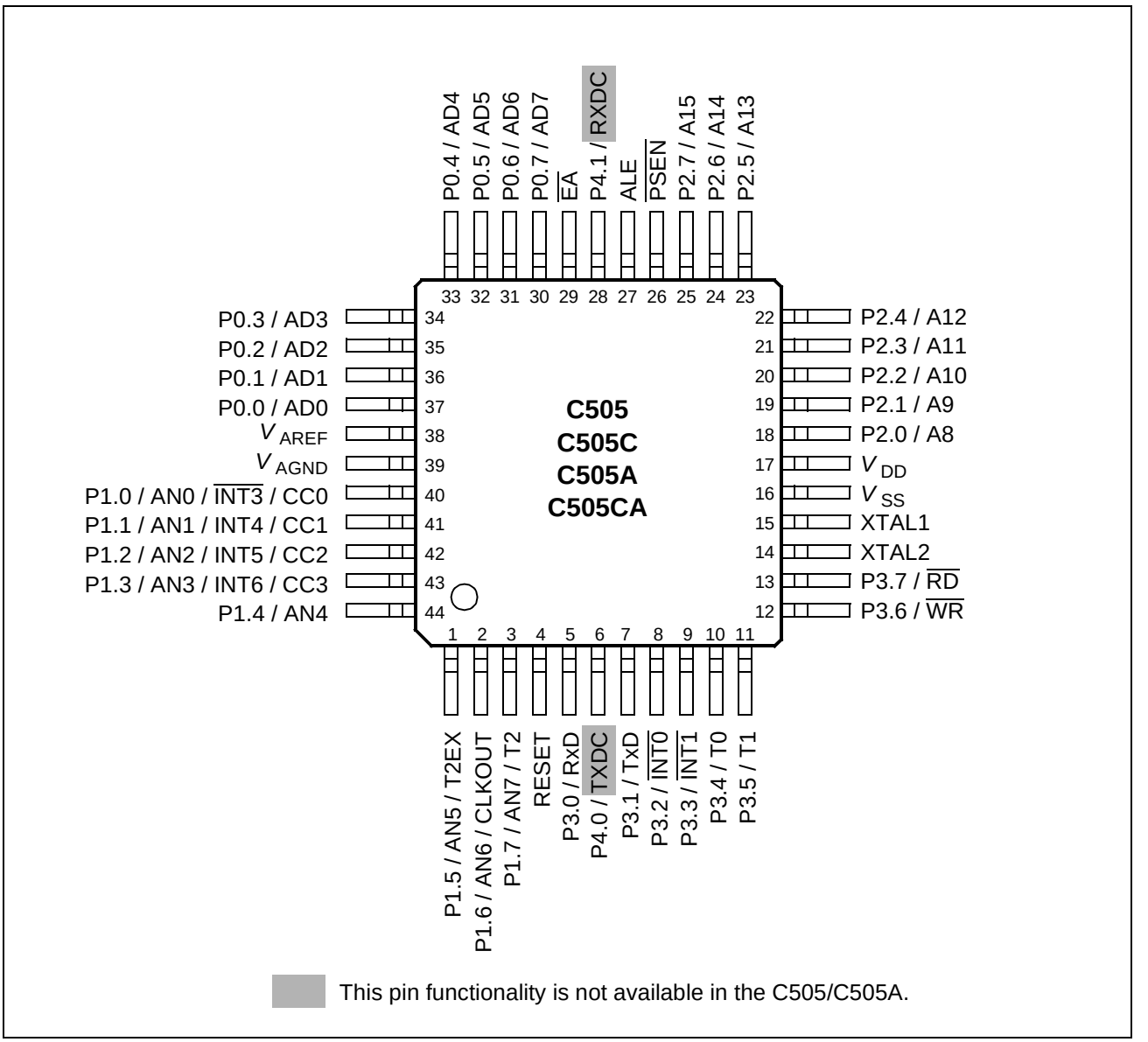


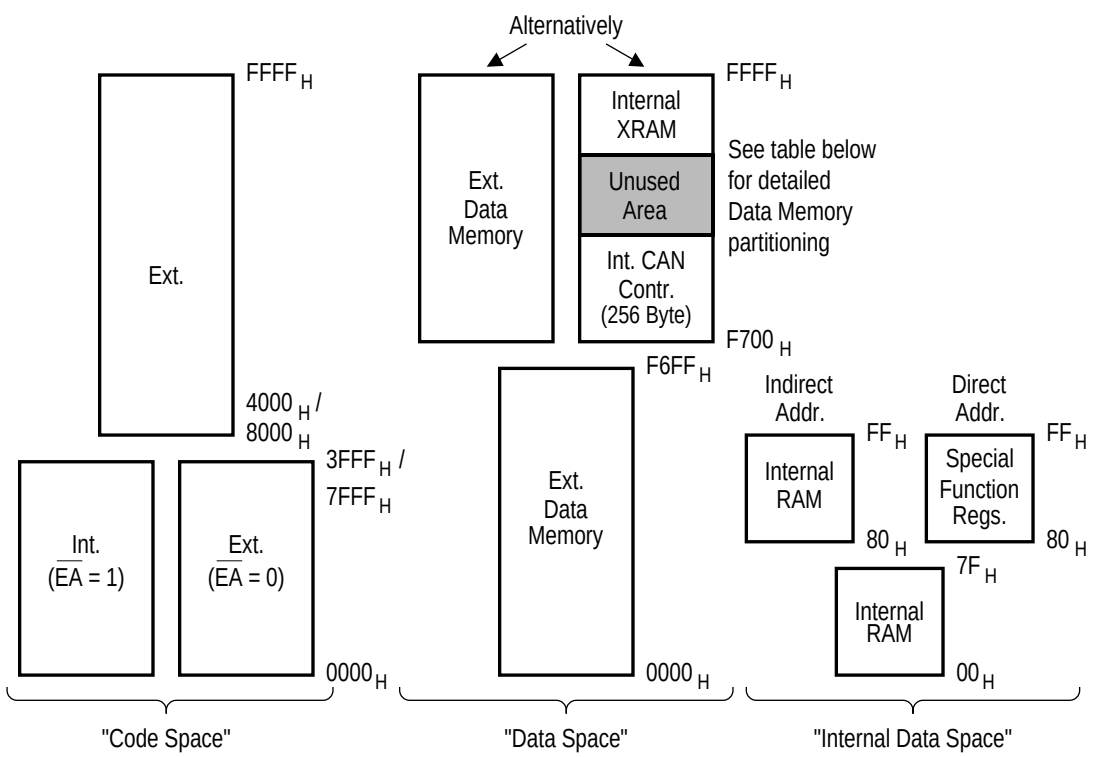
Figure 3
C505 Pin Configuration P-MQFP-44 Package (Top View)

Memory Organization

The C505 CPU manipulates operands in the following four address spaces:

- On-chip program memory : 16K byte ROM (C505(C)(A)-2R) or
  32K byte ROM (C505A-4R/C505CA-4R) or
  32K byte OTP (C505A-4E/C505CA-4E)
- Totally up to 64K byte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- Internal XRAM data memory : 256 byte (C505/C505C)
  1K byte (C505A/C505CA)
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C505 versions.



"Data Space" $F700_H$ to $FFFF_H$:

Device	CAN Area	Unused Area	XRAM Area
C505	–	$F700_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505C	$F700_H$–$F7FF_H$	$F800_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505A	–	$F700_H$–$FBFF_H$	$FC00_H$–$FFFF_H$
C505CA	$F700_H$–$F7FF_H$	$F800_H$–$FBFF_H$	$FC00_H$–$FFFF_H$

Figure 5
C505 Memory Map Memory Map

Table 3
Special Function Registers - Functional Blocks

Block	Symbol	Name	Address	Contents after Reset
CPU	ACC	Accumulator	**$E0_H$** [1]	00_H
	B	B-Register	**$F0_H$** [1]	00_H
	DPH	Data Pointer, High Byte	83_H	00_H
	DPL	Data Pointer, Low Byte	82_H	00_H
	DPSEL	Data Pointer Select Register	92_H	$XXXXX000_B$ [3]
	PSW	Program Status Word Register	**$D0_H$** [1]	00_H
	SP	Stack Pointer	81_H	07_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100001_B$ [3] [7]
	VR0 [4]	Version Register 0	FC_H	$C5_H$
	VR1 [4]	Version Register 1	FD_H	05_H
	VR2 [4]	Version Register 2	FE_H	[5]
A/D-Converter	ADCON0 [2]	A/D Converter Control Register 0	**$D8_H$** [1]	$00X00000_B$ [3]
	ADCON1	A/D Converter Control Register 1	DC_H	$01XXX000_B$ [3]
	ADDAT	A/D Converter Data Reg. (C505/C505C)	$D9_H$	00_H
	ADST	A/D Converter Start Reg. (C505/C505C)	DA_H	XX_H [3]
	ADDATH	A/D Converter High Byte Data Register (C505A/C505CA)	$D9_H$	00_H
	ADDATL	A/D Converter Low Byte Data Register (C505A/C505CA)	DA_H	$00XXXXXX_B$ [3]
	P1ANA [2] [4]	Port 1 Analog Input Selection Register	90_H	FF_H
Interrupt System	IEN0 [2]	Interrupt Enable Register 0	**$A8_H$** [1]	00_H
	IEN1 [2]	Interrupt Enable Register 1	**$B8_H$** [1]	00_H
	IP0 [2]	Interrupt Priority Register 0	$A9_H$	00_H
	IP1	Interrupt Priority Register 1	$B9_H$	$XX000000_B$ [3]
	TCON [2]	Timer Control Register	**88_H** [1]	00_H
	T2CON [2]	Timer 2 Control Register	**$C8_H$** [1]	$00X00000_B$
	SCON [2]	Serial Channel Control Register	**98_H** [1]	00_H
	IRCON	Interrupt Request Control Register	**$C0_H$** [1]	00_H
XRAM	XPAGE	Page Address Register for Extended on-chip XRAM and CAN Controller	91_H	00_H
	SYSCON[2]	System Control Register	$B1_H$	$XX100X01_B$ [3] [6] $XX100001_B$ [3] [7]

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) “X“ means that the value is undefined and the location is reserved
4) This SFR is a mapped SFR. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
5) The content of this SFR varies with the actual step of the C505 (eg. 01_H for the first step)
6) C505 / C505A/C505C only
7) C505CA only

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$B0_H$[2)]	P3	FF_H	$\overline{RD}$	$\overline{WR}$	T1	T0	$\overline{INT1}$	$\overline{INT0}$	TxD	RxD
$B1_H$	SYSCON[3)]	$XX10\text{-}0X01_B$	–	–	EALE	RMAP	CMOD	–	XMAP1	XMAP0
$B1_H$	SYSCON[4)]	$XX10\text{-}0001_B$	–	–	EALE	RMAP	CMOD	CSWO	XMAP1	XMAP0
$B8_H$[2)]	IEN1	00_H	EXEN2	SWDT	EX6	EX5	EX4	EX3	ECAN	EADC
$B9_H$	IP1	$XX00\text{-}0000_B$	–	–	.5	.4	.3	.2	.1	.0
BA_H	SRELH	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	.1	.0
$C0_H$[2)]	IRCON	00_H	EXF2	TF2	IEX6	IEX5	IEX4	IEX3	SWI	IADC
$C1_H$	CCEN	00_H	COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0
$C2_H$	CCL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C3_H$	CCH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C4_H$	CCL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C5_H$	CCH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C6_H$	CCL3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C7_H$	CCH3	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$C8_H$[2)]	T2CON	$00X0\text{-}0000_B$	T2PS	I3FR	–	T2R1	T2R0	T2CM	T2I1	T2I0
CA_H	CRCL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CB_H	CRCH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CC_H	TL2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
CD_H	TH2	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D0_H$[2)]	PSW	00_H	CY	AC	F0	RS1	RS0	OV	F1	P
$D8_H$[2)]	ADCON0	$00X0\text{-}0000_B$	BD	CLK	–	BSY	ADM	MX2	MX1	MX0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) C505 /C505C/C505A only
4) C505CA only

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{osc}/6x32	f_{osc}/12x32
1	16-bit timer/counter	0	1	f_{osc}/6	f_{osc}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{osc}/6.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{osc}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

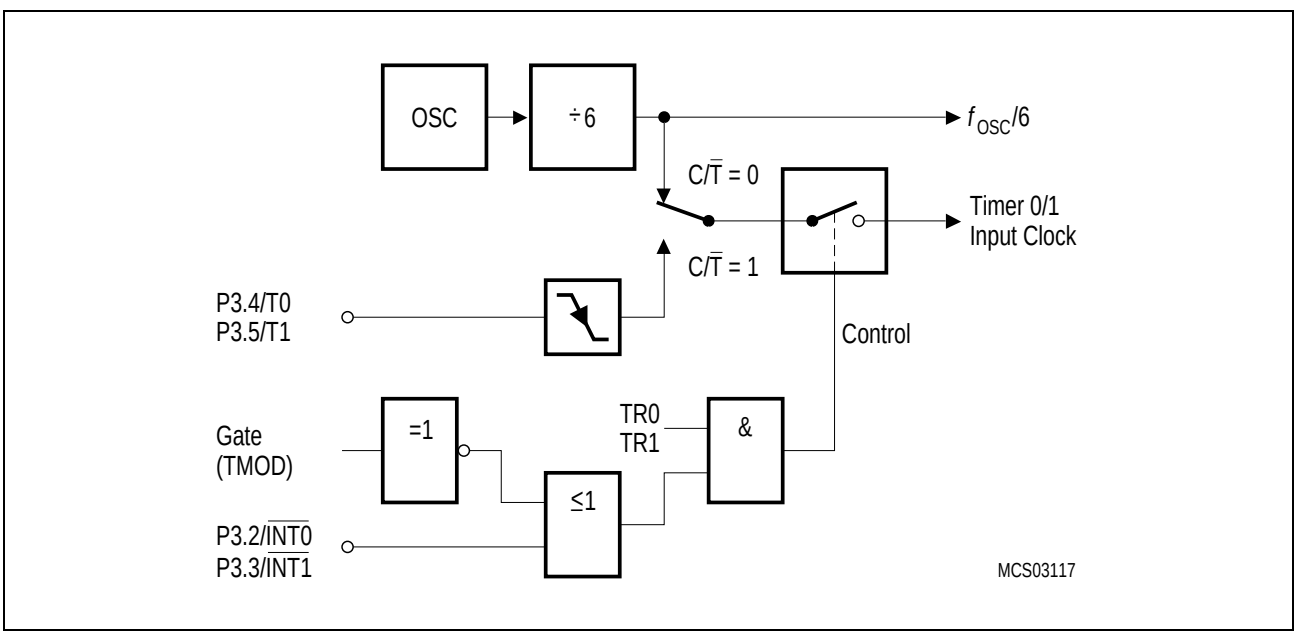


Figure 10
Timer/Counter 0 and 1 Input Clock Logic

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 12** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

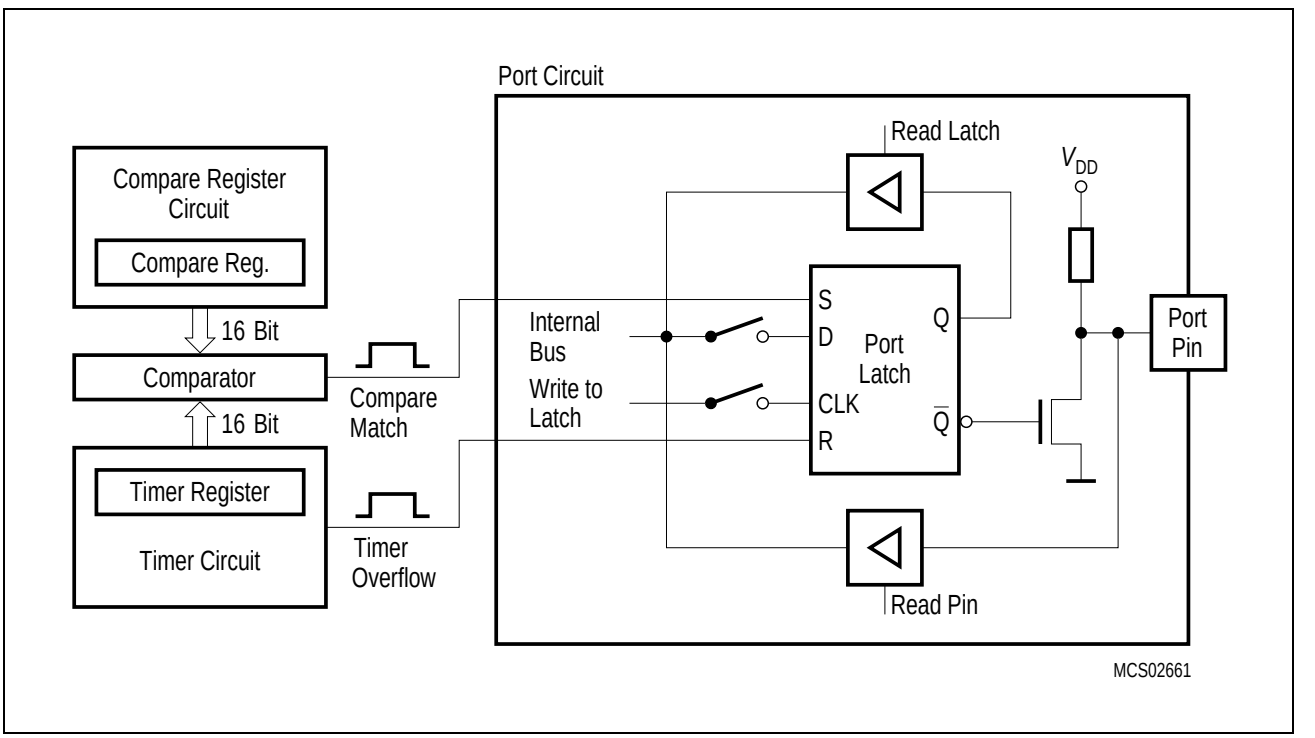


Figure 12
Port Latch in Compare Mode 0

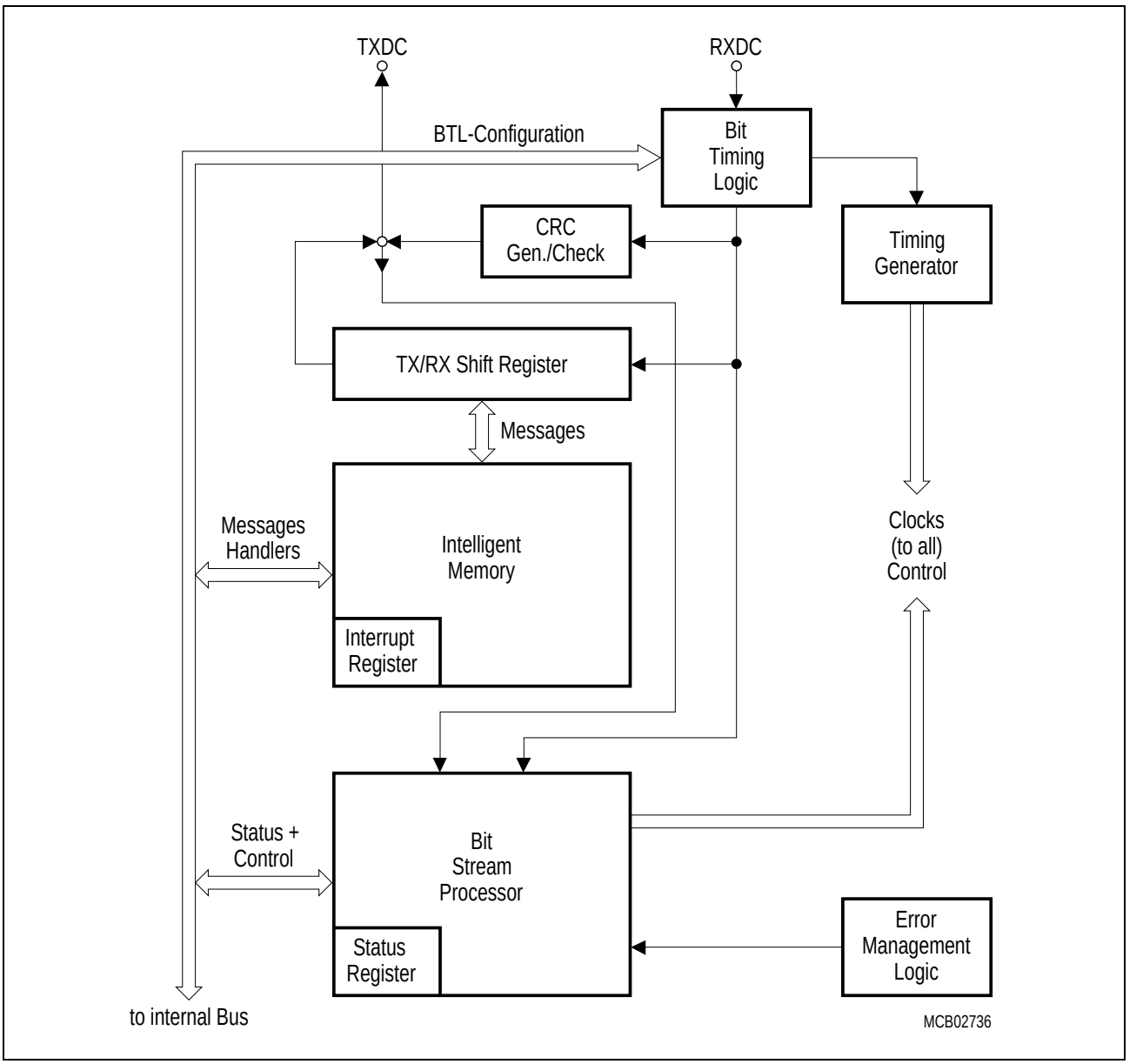


Figure 15
CAN Controller Block Diagram

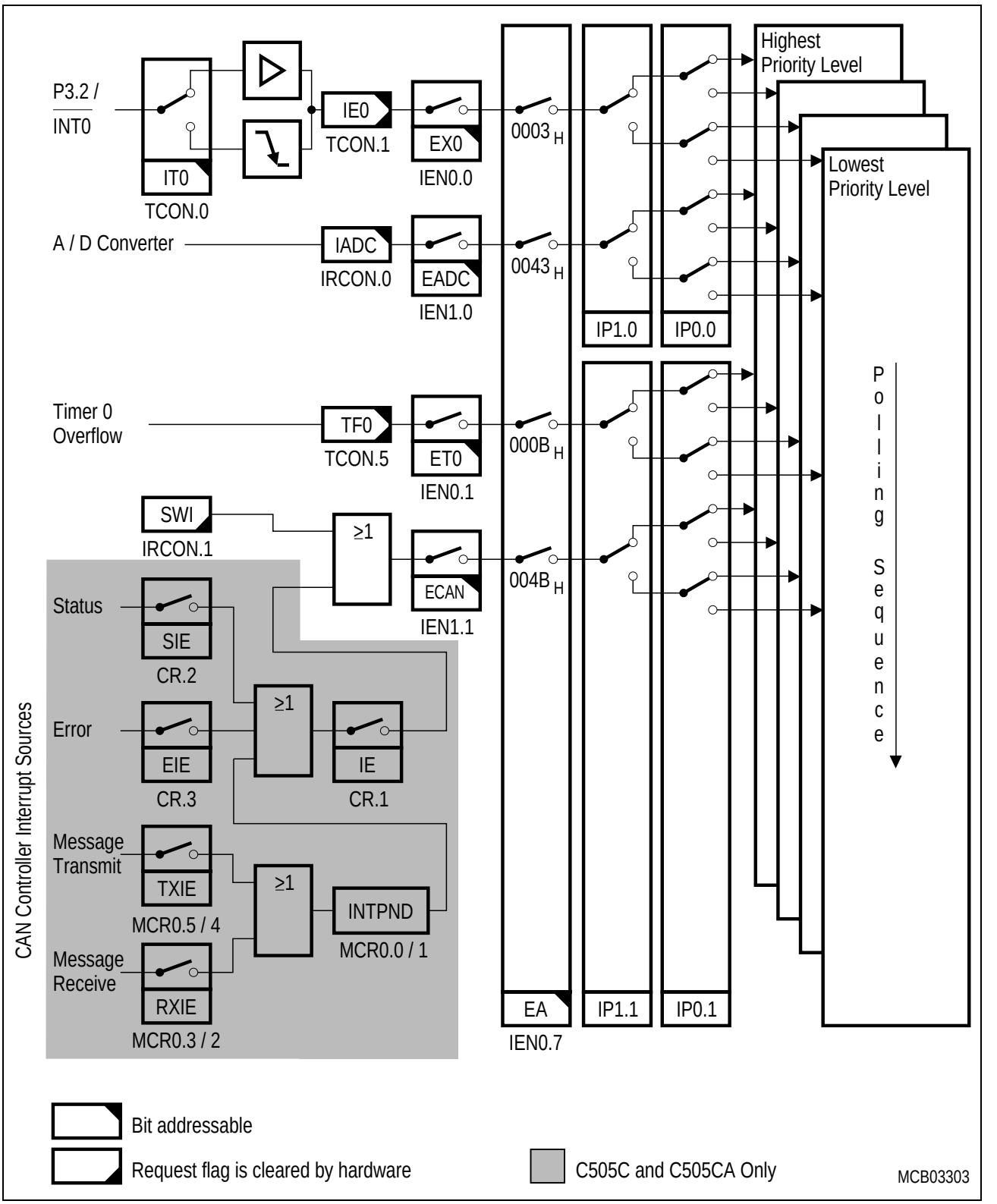


Figure 21
Interrupt Structure, Overview Part 1

*Note: Each of the 15 CAN controller message objects (C505C and C505CA only), shown in the shaded area of **Figure 21** provides the bits/flags.*

Oscillator Watchdog

The oscillator watchdog unit serves for three functions:

- **Monitoring of the on-chip oscillator's function**
  The watchdog supervises the on-chip oscillator's frequency; if it is lower than the frequency of the auxiliary RC oscillator in the watchdog unit, the internal clock is supplied by the RC oscillator and the device is brought into reset; if the failure condition disappears (i.e. the on-chip oscillator has a higher frequency than the RC oscillator), the part, in order to allow the oscillator to stabilize, executes a final reset phase of typ. 1 ms; then the oscillator watchdog reset is released and the part starts program execution from address 0000_H again.
- **Fast internal reset after power-on**
  The oscillator watchdog unit provides a clock supply for the reset before the on-chip oscillator has started. The oscillator watchdog unit also works identically to the monitoring function.
- **Control of external wake-up from software power-down mode**
  When the power-down mode is left by a low level at the P3.2/$\overline{\text{INT0}}$ pin or the P4.1/RXDC pin, the oscillator watchdog unit assures that the microcontroller resumes operation (execution of the power-down wake-up interrupt) with the nominal clock rate. In the power-down mode the RC oscillator and the on-chip oscillator are stopped. Both oscillators are started again when power-down mode is released. When the on-chip oscillator has a higher frequency than the RC oscillator, the microcontroller starts program execution by processing a power down interrupt after a final delay of typ. 1 ms in order to allow the on-chip oscillator to stabilize.

Power Saving Modes

The C505 provides two basic power saving modes, the idle mode and the power down mode. Additionally, a slow down mode is available. This power saving mode reduces the internal clock rate in normal operating mode and it can be also used for further power reduction in idle mode.

- **Idle mode**
  In the idle mode the main oscillator of the C505 continues to run, but the CPU is gated off from the clock signal. All peripheral units are further provided with the clock. The CPU status is preserved in its entirety. The idle mode can be terminated by any enabled interrupt of a peripheral unit or by a hardware reset.
- **Power down mode**
  The operation of the C505 is completely stopped and the oscillator is turned off. This mode is used to save the contents of the internal RAM with a very low standby current. Power down mode is entered by software and can be left by reset or by a short low pulse at pin P3.2/$\overline{\text{INT0}}$.or P4.1/RXDC.
- **Slow down mode**
  The controller keeps up the full operating functionality, but its normal clock frequency is internally divided by 32. This slows down all parts of the controller, the CPU and all peripherals, to 1/32-th of their normal operating frequency. Slowing down the frequency significantly reduces power consumption.

In the power down mode of operation, V_{DD} can be reduced to minimize power consumption. It must be ensured, however, that V_{DD} is not reduced before the power down mode is invoked, and that V_{DD} is restored to its normal operating level, before the power down mode is terminated. **Table 10** gives a general overview of the entry and exit procedures of the power saving modes.

Table 10
Power Saving Modes Overview

Mode	Entering (Instruction Example)	Leaving by	Remarks
Idle Mode	ORL PCON, #01H ORL PCON, #20H	Ocurrence of an interrupt from a peripheral unit	CPU clock is stopped; CPU maintains their data; peripheral units are active (if enabled) and provided with clock
		Hardware Reset	
Power Down Mode	ORL PCON, #02H ORL PCON, #40H	Hardware Reset	Oscillator is stopped; contents of on-chip RAM and SFR's are maintained;
		Short low pulse at pin P3.2/$\overline{\text{INT0}}$ or P4.1/RXDC	
Slow Down Mode	ORL PCON,#10H	ANL PCON,#0EFH or Hardware Reset	Oscillator frequency is reduced to 1/32 of its nominal frequency

Operating Conditions

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	4.25	5.5	V	Active mode, $f_{osc\ max}$ = 20 MHz
		2	5.5	V	PowerDown mode
Ground voltage	V_{SS}	0		V	Reference voltage
Ambient temperature				°C	–
SAB-C505	T_A	0	70		
SAF-C505	T_A	-40	85		
SAH-C505	T_A	-40	110		
SAK-C505	T_A	-40	125		
Analog reference voltage	V_{AREF}	4	V_{DD} + 0.1	V	–
Analog ground voltage	V_{AGND}	V_{SS} – 0.1	V_{SS} + 0.2	V	–
Analog input voltage	V_{AIN}	V_{AGND} -0.2	V_{AREF} +0.2	V	–
XTAL clock	f_{osc}	2	20 (with 50% duty cycle)	MHz	1)

1) For the extended temperature range -40 °C to 110 °C (SAH) and -40 °C to 125 °C (SAK), the devices C505-2R, C505-L, C505C-2R and C505C-L have the max. operating frequency of 16MHz with 50% clock duty cycle.

Parameter Interpretation

The parameters listed in the following partly represent the characteristics of the C505 and partly its demands on the system. To aid in interpreting the parameters right, when evaluating them for a design, they are marked in column “Symbol”:

CC (**C**ontroller **C**haracteristics):

The logic of the C505 will provide signals with the respective characteristics.

SR (**S**ystem **R**equirement):

The external system must provide signals with the respective characteristics to the C505.

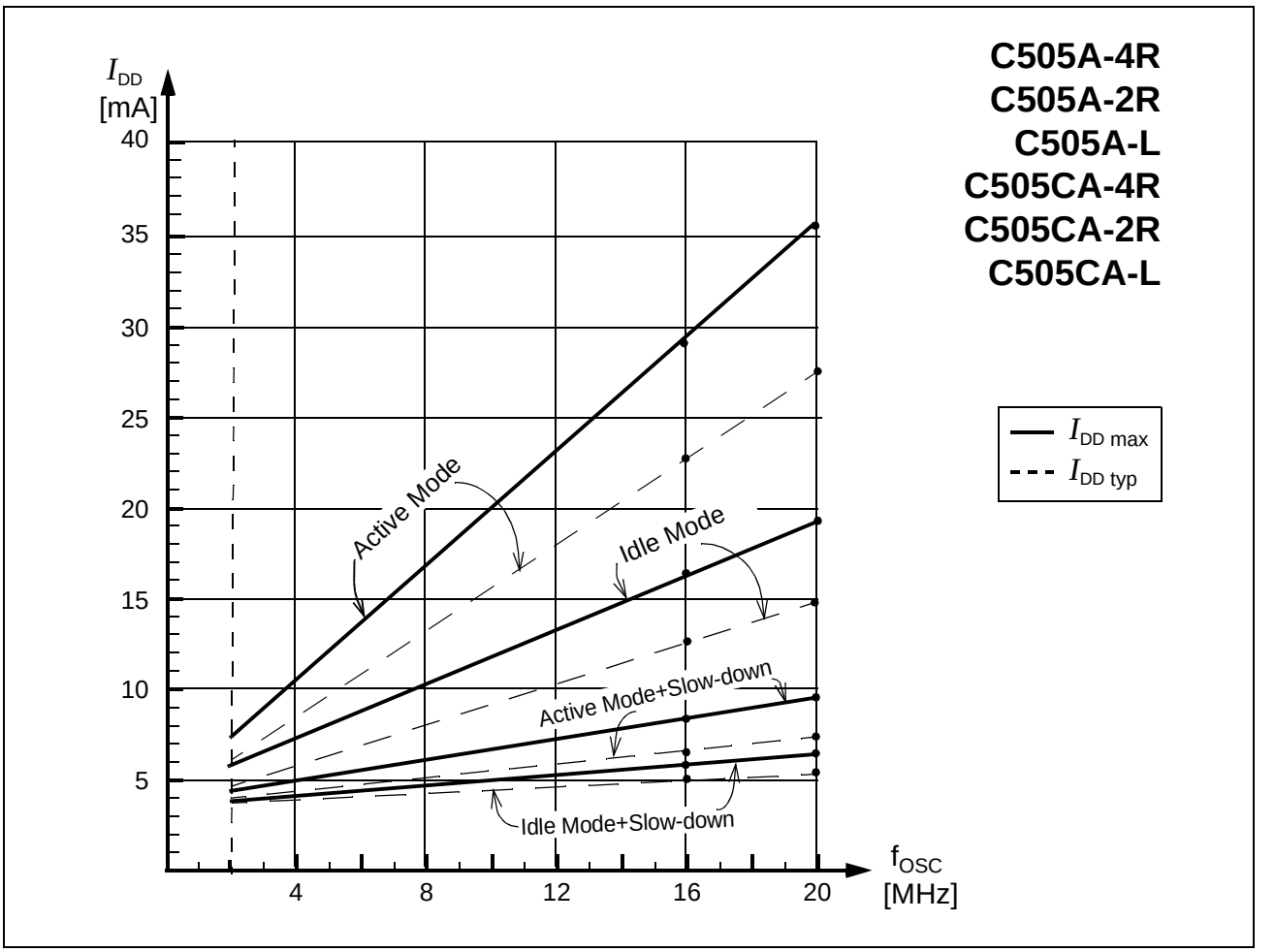


Figure 31
I_{DD} Diagram of C505A-4R/C505A-2R/C505A-L/C505CA-4R/C505CA-2R/C505CA-L

C505A-4R/C505A-2R/C505A-L/C505CA-4R/C505CA-2R/C505CA-L :
Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.19 * f_{OSC} + 3.77$ $1.54 * f_{OSC} + 4.47$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.57 * f_{OSC} + 3.55$ $0.75 * f_{OSC} + 4.26$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.18 * f_{OSC} + 3.74$ $0.28 * f_{OSC} + 3.67$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.07 * f_{OSC} + 3.91$ $0.14 * f_{OSC} + 3.64$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

A/D Converter Characteristics of C505 and C505C

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND} - 0.2	V_{AREF} + 0.2	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	320 x t_{IN} 160 x t_{IN} 80 x t_{IN} 40 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{DD}-0.5V 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 500 - 1	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 1	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	320 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	160 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	80 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	40 x t_{IN}

Further timing conditions : t_{ADC} min = 800 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} (max.) is tested at $-40 \le T_A \le 125$ °C ; $V_{DD} \le 5.5$ V; $V_{AREF} \le V_{DD} + 0.1$ V and $V_{SS} \le V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle, cont'd)

External Clock Drive Characteristics

Parameter	Symbol	CPU Clock = 16 MHz Duty Cycle 0.4 to 0.6		Variable CPU Clock 1/CLP = 2 to 16 MHz		Unit
		min.	max.	min.	max.	
Oscillator period	CLP	62.5	62.5	62.5	500	ns
High time	TCL_H	25	–	25	CLP - TCL_L	ns
Low time	TCL_L	25	–	25	CLP - TCL_H	ns
Rise time	t_R	–	10	–	10	ns
Fall time	t_F	–	10	–	10	ns
Oscillator duty cycle	DC	0.4	0.6	25 / CLP	1 - 25 / CLP	–
Clock cycle	TCL	25	37.5	CLP * DC_{min}	CLP * DC_{max}	ns

Note: The 16 MHz values in the tables are given as an example for a typical duty cycle variation of the oscillator clock from 0.4 to 0.6.

AC Characteristics (20 MHz, 0.5 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	35	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	CLP/2 - 15	–	ns
Address hold after ALE	t_{LLAX}	10	–	CLP/2 - 15	–	ns
ALE to valid instruction in	t_{LLIV}	–	55	–	2 CLP - 45	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	CLP/2 - 15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	60	–	3/2 CLP - 15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	25	–	3/2 CLP - 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	20	–	CLP/2 - 5	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	CLP/2 - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	65	–	5/2 CLP - 60	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	- 5	–	- 5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics (20 MHz, 0.5 Duty Cycle, cont'd)

External Data Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		20 MHz clock 0.5 Duty Cycle		Variable Clock 1/CLP = 2 MHz to 20 MHz		
		min.	max.	min.	max.	
$\overline{RD}$ pulse width	t_{RLRH}	120	–	3 CLP - 30	–	ns
$\overline{WR}$ pulse width	t_{WLWH}	120	–	3 CLP - 30	–	ns
Address hold after ALE	t_{LLAX2}	35	–	CLP - 15	–	ns
$\overline{RD}$ to valid data in	t_{RLDV}	–	75	–	5/2 CLP- 50	ns
Data hold after $\overline{RD}$	t_{RHDX}	0	–	0	–	ns
Data float after $\overline{RD}$	t_{RHDZ}	–	38	–	CLP - 12	ns
ALE to valid data in	t_{LLDV}	–	150	–	4 CLP - 50	ns
Address to valid data in	t_{AVDV}	–	150	–	9/2 CLP - 75	ns
ALE to $\overline{WR}$ or $\overline{RD}$	t_{LLWL}	60	90	3/2 CLP - 15	3/2 CLP + 15	ns
Address valid to $\overline{WR}$	t_{AVWL}	70	–	2 CLP - 30	–	ns
$\overline{WR}$ or $\overline{RD}$ high to ALE high	t_{WHLH}	10	40	CLP/2 - 15	CLP/2 + 15	ns
Data valid to $\overline{WR}$ transition	t_{QVWX}	5	–	CLP/2 - 20	–	ns
Data setup before $\overline{WR}$	t_{QVWH}	125	–	7/2 CLP - 50	–	ns
Data hold after $\overline{WR}$	t_{WHQX}	5	–	CLP/2 - 20	–	ns
Address float after $\overline{RD}$	t_{RLAZ}	–	0	–	0	ns

External Clock Drive Characteristics

Parameter	Symbol	Limit Values		Unit
		Variable Clock Freq. = 2 MHz to 20 MHz		
		min.	max.	
Oscillator period	CLP	50	500	ns
High time	TCL_H	15	$CLP-TCL_L$	ns
Low time	TCL_L	15	$CLP-TCL_H$	ns
Rise time	t_R	–	10	ns
Fall time	t_F	–	10	ns
Oscillator duty cycle	DC	0.5	0.5	–

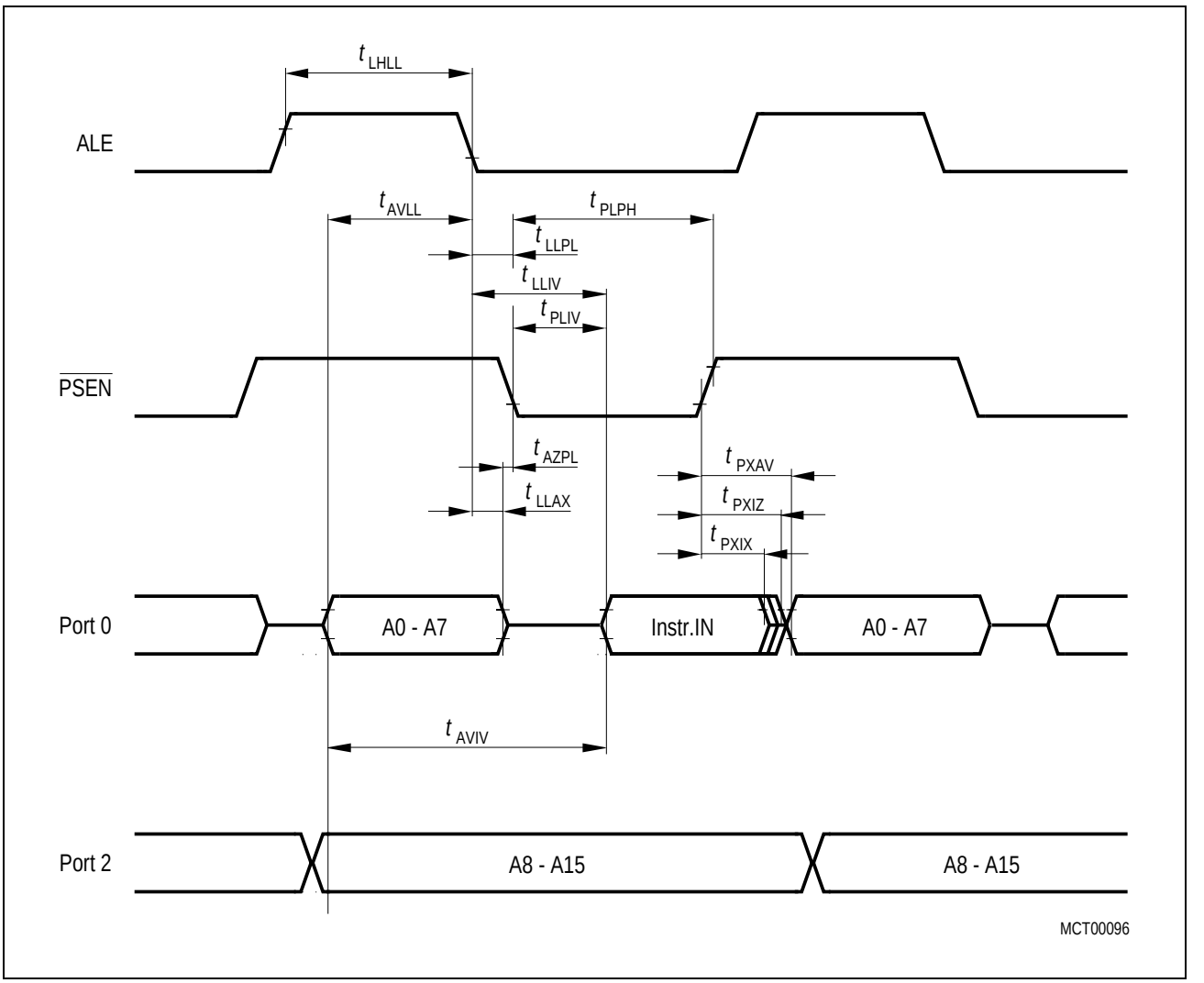


Figure 32
Program Memory Read Cycle

Infineon goes for Business Excellence

“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
Better operating results and business excellence mean less idleness and wastefulness for all of us, more professional success, more accurate information, a better overview and, thereby, less frustration and more satisfaction.”

Dr. Ulrich Schumacher

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