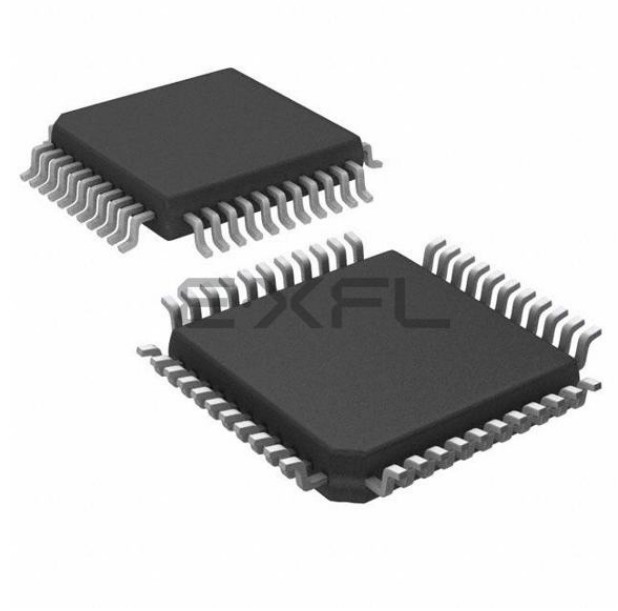
Infineon Technologies - C505CALMCAFXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505calmcafxqma1

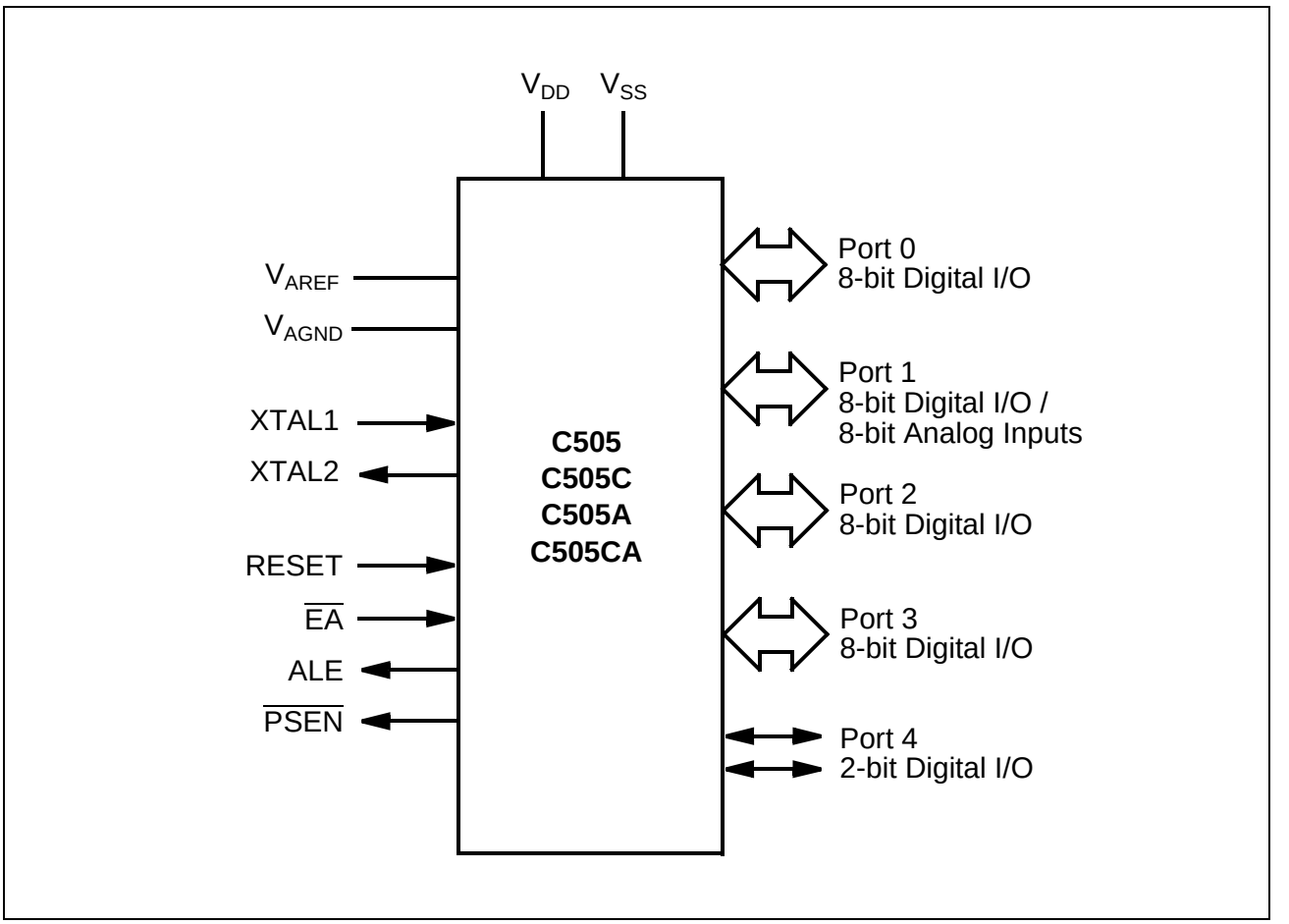


Figure 2
Logic Symbol

Note: The ordering codes for the Mask-ROM versions are defined for each product after verification of the respective ROM code.

Table 2
Pin Definitions and Functions

Symbol	Pin Number	I/O *)	Function
P1.0-P1.7	40-44,1-3	I/O	**Port 1** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 1 pins can be used for digital input/output or as analog inputs of the A/D converter. Port 1 pins that have 1's written to them are pulled high by internal pull-up transistors and in that state can be used as inputs. As inputs, port 1 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. Port 1 pins are assigned to be used as analog inputs via the register P1ANA. As secondary digital functions, port 1 contains the interrupt, timer, clock, capture and compare pins. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for compare functions). The secondary functions are assigned to the pins of port 1 as follows:
	40		P1.0 / AN0 / $\overline{\text{INT3}}$ / CC0 — Analog input channel 0 interrupt 3 input / capture/compare channel 0 I/O
	41		P1.1 / AN1 / INT4 / CC1 — Analog input channel 1/ interrupt 4 input / capture/compare channel 1 I/O
	42		P1.2 / AN2 / INT5 / CC2 — Analog input channel 2 / interrupt 5 input / capture/compare channel 2 I/O
	43		P1.3 / AN3 / INT6 / CC3 — Analog input channel 3 interrupt 6 input / capture/compare channel 3 I/O
	44		P1.4 / AN4 — Analog input channel 4
	1		P1.5 / AN5 / T2EX — Analog input channel 5 / Timer 2 external reload / trigger input
	2		P1.6 / AN6 / CLKOUT — Analog input channel 6 / system clock output
	3		P1.7 / AN7 / T2 — Analog input channel 7 / counter 2 input
			Port 1 is used for the low-order address byte during program verification of the C505 ROM versions (i.e. C505(C)(A)-2R/ C505A-4R/C505CA-4R).

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P4.0 P4.1	6 28	I/O I/O	**Port 4** is a 2-bit quasi-bidirectional port with internal pull-up arrangement. Port 4 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 4 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to the secondary function RXDC must be programmed to a one (1) for that function to operate. The secondary functions are assigned to the two pins of port 4 as follows (C505C and C505CA only) : P4.0 / TXDC Transmitter output of CAN controller P4.1 / RXDC Receiver input of CAN controller
XTAL2	14	O	**XTAL2** Output of the inverting oscillator amplifier.
XTAL1	15	I	**XTAL1** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected. To operate above a frequency of 16 MHz, a duty cycle of the etxernal clock signal of 50 % should be maintained. Minimum and maximum high and low times as well as rise/ fall times specified in the AC characteristics must be observed.

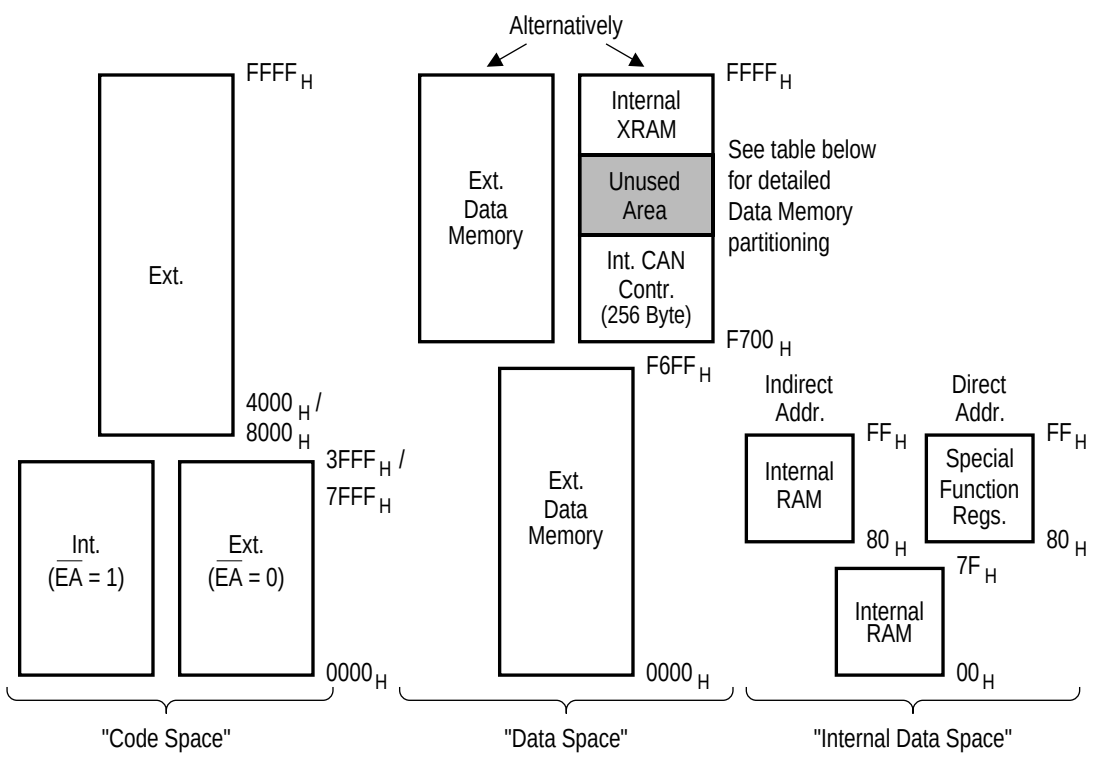
*) I = Input
O = Output

Memory Organization

The C505 CPU manipulates operands in the following four address spaces:

- On-chip program memory : 16K byte ROM (C505(C)(A)-2R) or
  32K byte ROM (C505A-4R/C505CA-4R) or
  32K byte OTP (C505A-4E/C505CA-4E)
- Totally up to 64K byte internal/external program memory
- up to 64 Kbyte of external data memory
- 256 bytes of internal data memory
- Internal XRAM data memory : 256 byte (C505/C505C)
  1K byte (C505A/C505CA)
- a 128 byte special function register area

Figure 5 illustrates the memory address spaces of the C505 versions.



"Data Space" $F700_H$ to $FFFF_H$:

Device	CAN Area	Unused Area	XRAM Area
C505	–	$F700_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505C	$F700_H$–$F7FF_H$	$F800_H$–$FEFF_H$	$FF00_H$–$FFFF_H$
C505A	–	$F700_H$–$FBFF_H$	$FC00_H$–$FFFF_H$
C505CA	$F700_H$–$F7FF_H$	$F800_H$–$FBFF_H$	$FC00_H$–$FFFF_H$

Figure 5
C505 Memory Map Memory Map

Table 3
Special Function Registers - Functional Blocks (cont'd)

Block	Symbol	Name	Address	Contents after Reset
Ports	P0	Port 0	**80_H** 1)	FF_H
	P1	Port 1	**90_H** 1)	FF_H
	P1ANA 2) 4)	Port 1 Analog Input Selection Register	**90_H** 1)	FF_H
	P2	Port 2	**$A0_H$** 1)	FF_H
	P3	Port 3	**$B0_H$** 1)	FF_H
	P4	Port 4	**E8H** 1)	$XXXXXX11_B$
Serial Channel	ADCON0 2)	A/D Converter Control Register 0	**$D8_H$** 1)	$00X00000_B$ 3)
	PCON 2)	Power Control Register	87_H	00_H
	SBUF	Serial Channel Buffer Register	99_H	XX_H 3)
	SCON	Serial Channel Control Register	**98_H** 1)	00_H
	SRELL	Serial Channel Reload Register, low byte	AA_H	$D9_H$
	SRELH	Serial Channel Reload Register, high byte	BA_H	$XXXXXX11_B$ 3)
Timer 0/ Timer 1	TCON	Timer 0/1 Control Register	**88_H** 1)	00_H
	TH0	Timer 0, High Byte	$8C_H$	00_H
	TH1	Timer 1, High Byte	$8D_H$	00_H
	TL0	Timer 0, Low Byte	$8A_H$	00_H
	TL1	Timer 1, Low Byte	$8B_H$	00_H
	TMOD	Timer Mode Register	89_H	00_H
Compare/ Capture Unit / Timer 2	CCEN	Comp./Capture Enable Reg.	$C1_H$	00_H 3)
	CCH1	Comp./Capture Reg. 1, High Byte	$C3_H$	00_H
	CCH2	Comp./Capture Reg. 2, High Byte	$C5_H$	00_H
	CCH3	Comp./Capture Reg. 3, High Byte	$C7_H$	00_H
	CCL1	Comp./Capture Reg. 1, Low Byte	$C2_H$	00_H
	CCL2	Comp./Capture Reg. 2, Low Byte	$C4_H$	00_H
	CCL3	Comp./Capture Reg. 3, Low Byte	$C6_H$	00_H
	CRCH	Reload Register High Byte	CB_H	00_H
	CRCL	Reload Register Low Byte	CA_H	00_H
	TH2	Timer 2, High Byte	CD_H	00_H
	TL2	Timer 2, Low Byte	CC_H	00_H
	T2CON	Timer 2 Control Register	**$C8_H$** 1)	$00X00000_B$ 3)
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
Watchdog	WDTREL	Watchdog Timer Reload Register	86_H	00_H
	IEN0 2)	Interrupt Enable Register 0	**$A8_H$** 1)	00_H
	IEN1 2)	Interrupt Enable Register 1	**$B8_H$** 1)	00_H
	IP0 2)	Interrupt Priority Register 0	$A9_H$	00_H
Pow. Save Modes	PCON 2)	Power Control Register	87_H	00_H
	PCON1 4)	Power Control Register 1	**88_H** 1)	$0XX0XXXX_B$ 3)

1) Bit-addressable special function registers
2) This special function register is listed repeatedly since some bits of it also belong to other functional blocks.
3) "X" means that the value is undefined and the location is reserved
4) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses (cont'd)

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$D9_H$	ADDAT [6)]	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$D9_H$	ADDATH [7)]	00_H	.9	.8	.7	.6	.5	.4	.3	.2
DA_H	ADST [6)]	$XXXX\text{-}XXXX_B$	–	–	–	–	–	–	–	–
DA_H	ADDATL [7)]	$00XX\text{-}XXXX_B$	.1	.0	–	–	–	–	–	–
DC_H	ADCON1	$01XX\text{-}X000_B$	ADCL1	ADCL0	–	–	–	MX2	MX1	MX0
$E0_H$[2)]	ACC	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$E8_H$[2)]	P4	$XXXX\text{-}XX11_B$	–	–	–	–	–	–	RXDC	TXDC
$F0_H$[2)]	B	00_H	.7	.6	.5	.4	.3	.2	.1	.0
FC_H[3)4)]	VR0	$C5_H$	1	1	0	0	0	1	0	1
FD_H[3)4)]	VR1	05_H	0	0	0	0	0	1	0	1
FE_H[3)4)]	VR2 [5)]	01_H[8)] 12_H[9)] 33_H[10)]	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.
4) These are read-only registers
5) The content of this SFR varies with the actual of the step C505 (eg. 01_H or 11_H or 21_H for the first step)
6) C505 / C505C only
7) C505A / C505CA only
8) C505 / C505C AB step only
9) C505A-4E / C505CA-4E BA step only (11_H for the AA step)
10) C505A-4R / C505CA-4R BB step only (32_H for the BA step)

Timer/Counter 2 with Compare/Capture/Reload

The timer 2 of the C505 provides additional compare/capture/reload features. which allow the selection of the following operating modes:

- Compare : up to 4 PWM signals with 16-bit/300 ns resolution (@ 20 MHz clock)
- Capture : up to 4 high speed capture inputs with 300 ns resolution
- Reload : modulation of timer 2 cycle time

The block diagram in **Figure 11** shows the general configuration of timer 2 with the additional compare/capture/reload registers. The I/O pins which can used for timer 2 control are located as multifunctional port functions at port 1.

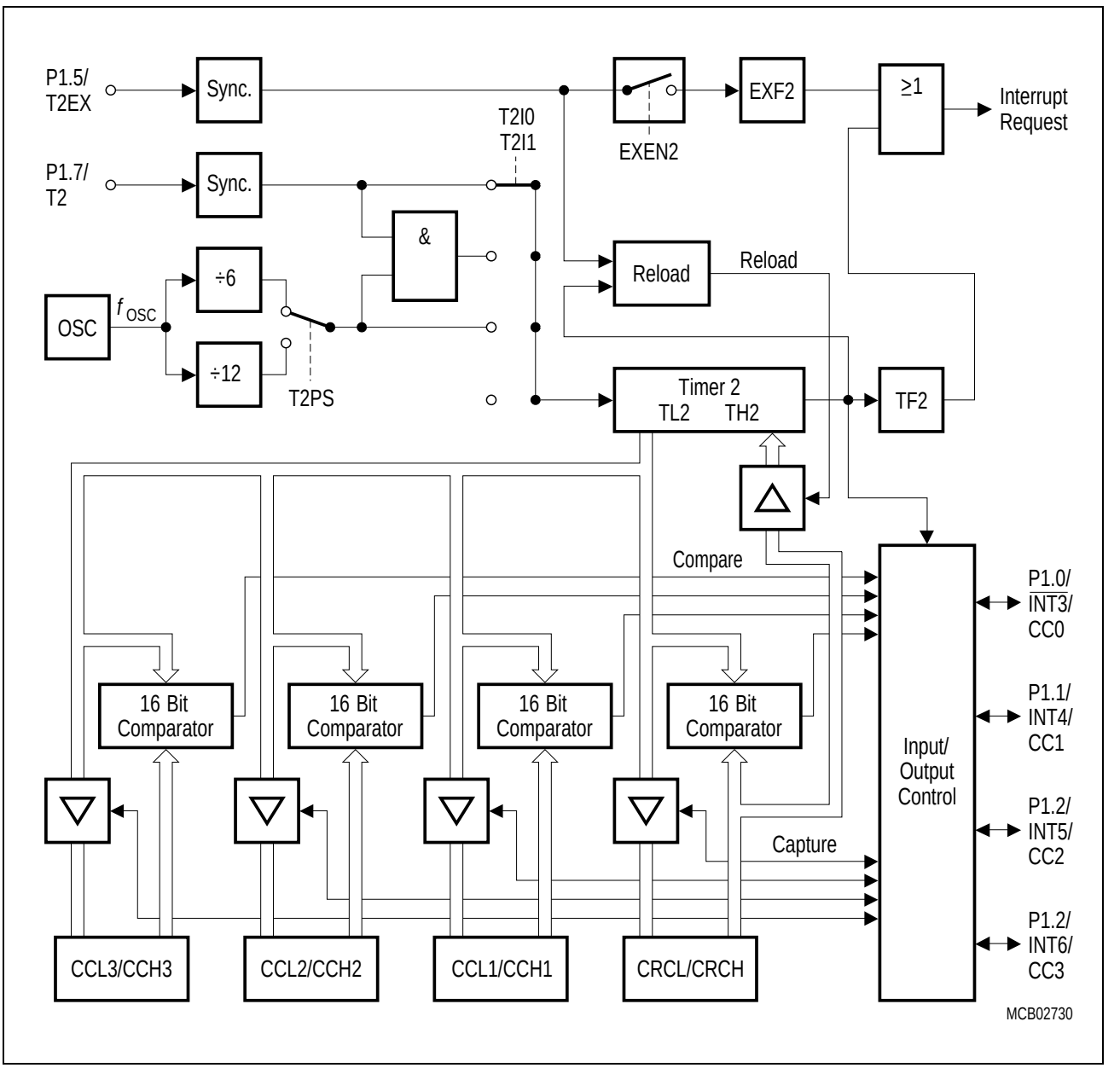


Figure 11
Timer 2 Block Diagram

Timer 2 Operating Modes

The timer 2, which is a 16-bit-wide register, can operate as timer, event counter, or gated timer. A roll-over of the count value in TL2/TH2 from all 1’s to all 0’s sets the timer overflow flag TF2 in SFR IRCON, which can generate an interrupt. The bits in register T2CON are used to control the timer 2 operation.

Timer Mode : In timer function, the count rate is derived from the oscillator frequency. A prescaler offers the possibility of selecting a count rate of 1/6 or 1/12 of the oscillator frequency.

Gated Timer Mode : In gated timer function, the external input pin T2 (P1.7) functions as a gate to the input of timer 2. If T2 is high, the internal clock input is gated to the timer. T2 = 0 stops the counting procedure. This facilitates pulse width measurements. The external gate signal is sampled once every machine cycle.

Event Counter Mode : In the event counter function. the timer 2 is incremented in response to a 1-to-0 transition at its corresponding external input pin T2 (P1.7). In this function, the external input is sampled every machine cycle. Since it takes two machine cycles (12 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/6 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it must be held for at least one full machine cycle.

Reload of Timer 2 : Two reload modes are selectable:
In mode 0, when timer 2 rolls over from all 1’s to all 0’s, it not only sets TF2 but also causes the timer 2 registers to be loaded with the 16-bit value in the CRC register, which is preset by software.
In mode 1, a 16-bit reload from the CRC register is caused by a negative transition at the corresponding input pin P1.5/T2EX. This transition will also set flag EXF2 if bit EXEN2 in SFR IEN1 has been set.

Timer 2 Compare Modes

The compare function of a timer/register combination operates as follows : the 16-bit value stored in a compare or compare/capture register is compared with the contents of the timer register; if the count value in the timer register matches the stored value, an appropriate output signal is generated at a corresponding port pin and an interrupt can be generated.

Compare Mode 0

In compare mode 0, upon matching the timer and compare register contents, the output signal changes from low to high. It goes back to a low level on timer overflow. As long as compare mode 0 is enabled, the appropriate output pin is controlled by the timer circuit only and writing to the port will have no effect. **Figure 12** shows a functional diagram of a port circuit when used in compare mode 0. The port latch is directly controlled by the timer overflow and compare match signals. The input line from the internal bus and the write-to-latch line of the port latch are disconnected when compare mode 0 is enabled.

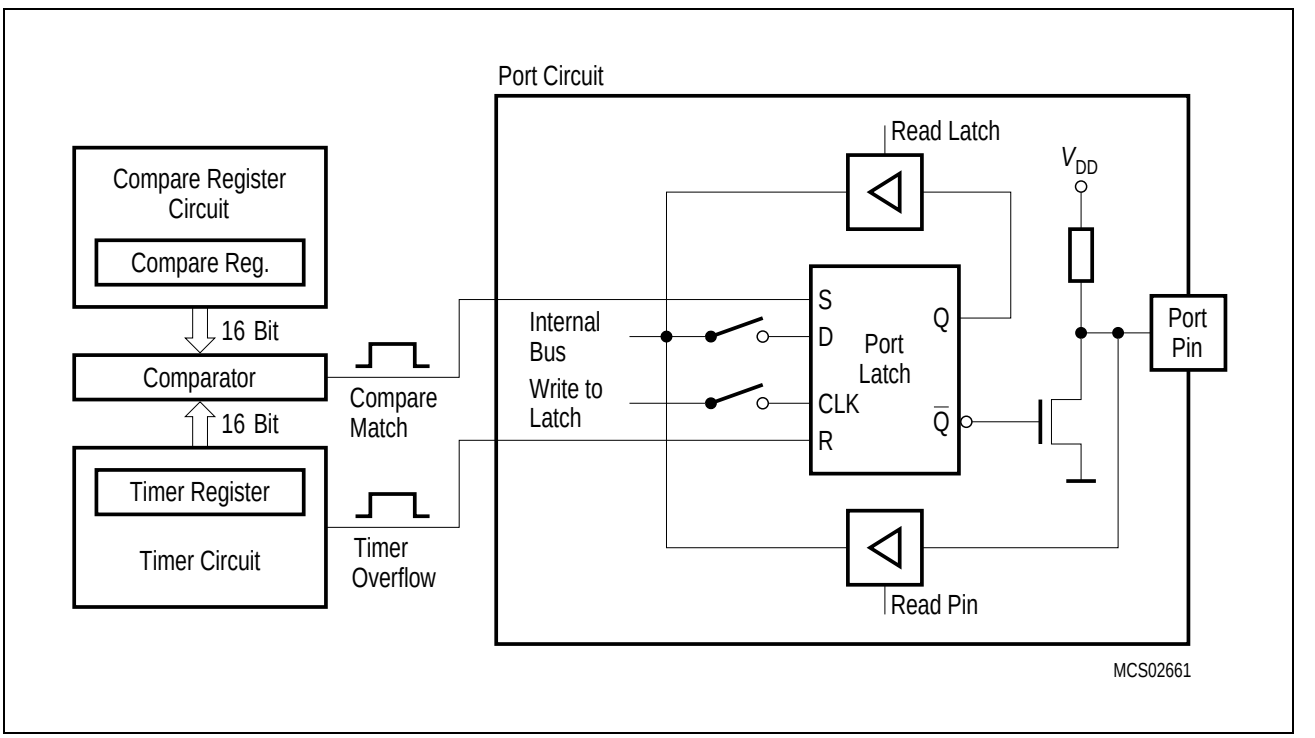


Figure 12
Port Latch in Compare Mode 0

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 7**.

Table 7
USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode, fixed baud rate Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	9-bit UART, variable baud rate Like mode 2

For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **Figure 14** to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abbrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a decdicated baud rate generator (see **Figure 14**).

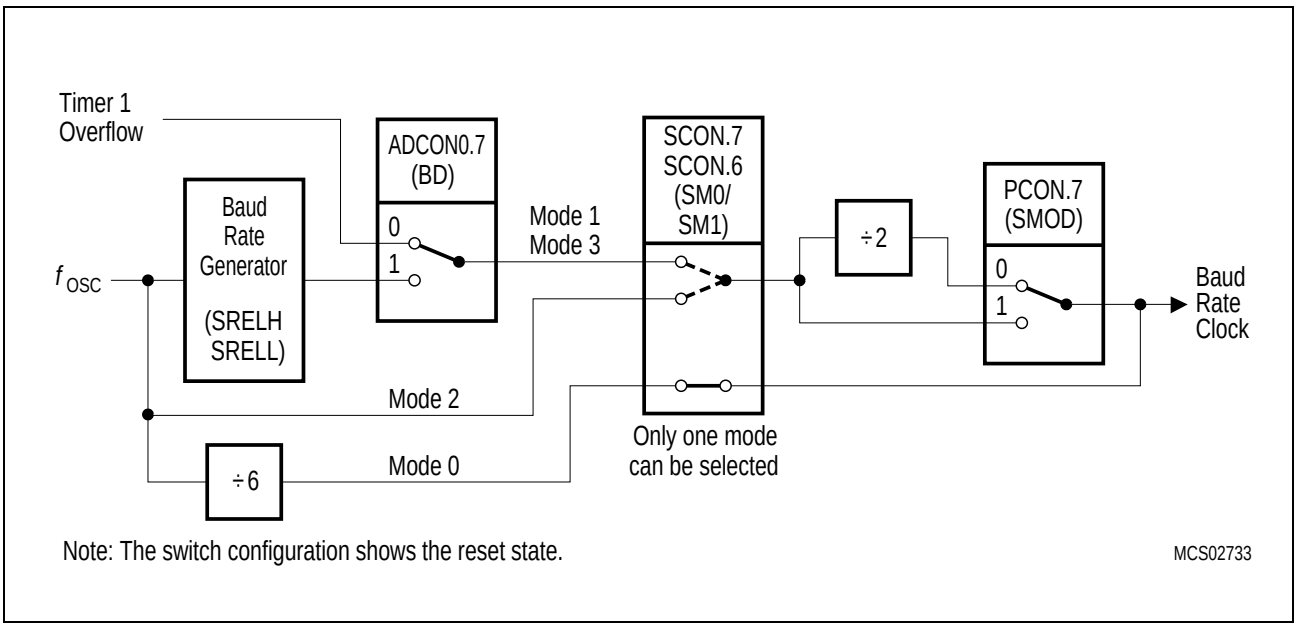


Figure 14
Block Diagram of Baud Rate Generation for the Serial Interface

Table 8 below lists the values/formulas for the baud rate calculation of the serial interface with its dependencies of the control bits BD and SMOD.

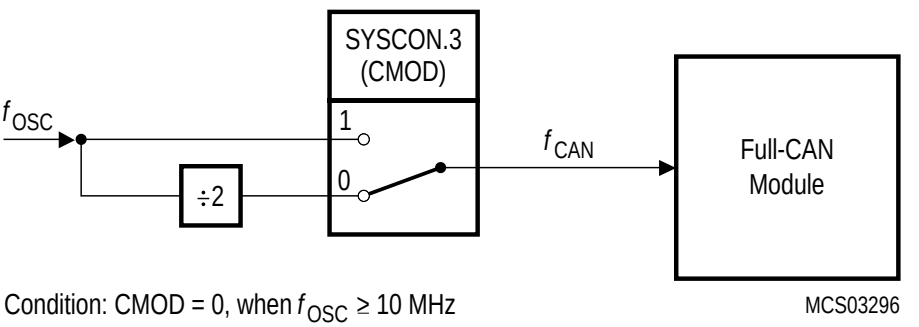
Table 8
Serial Interface - Baud Rate Dependencies

Serial Interface Operating Modes	Active Control Bits		Baud Rate Calculation
	BD	SMOD	
Mode 0 (Shift Register)	–	–	f_{OSC} / 6
Mode 1 (8-bit UART) Mode 3 (9-bit UART)	0	X	Controlled by timer 1 overflow : (2^{SMOD} × timer 1 overflow rate) / 32
	1	X	Controlled by baud rate generator (2^{SMOD} × f_{OSC}) / (32 × baud rate generator overflow rate)
Mode 2 (9-bit UART)	–	0 1	f_{OSC} / 32 f_{OSC} / 16

CAN Controller Software Initialization

The very first step of the initialization is the CAN controller input clock selection. A divide-by-2 prescaler is enabled by default after reset (**Figure 16**). Setting bit CMOD (SYSCON.3) disables the prescaler. The purpose of the prescaler selection is:

– to ensure that the CAN controller is operable when f_{OSC} is over 10 MHz (bit CMOD =0)
– to achieve the maximum CAN baudrate of 1 Mbaud when f_{OSC} is 8 MHz (bit CMOD=1)



Frequency (MHz)		CMOD (SYSCON.3)	BRP (BTR0.0-5)	CAN baudrate (Mbaud/sec)
f_{OSC}	f_{CAN}			
8	8	1	000000_B	1
8	4	0	000000_B	0.5
16	8	0	000000_B	1

Note : The switch configuration shows the reset state of bit CMOD.

Figure 16
CAN controller Input Clock Selection

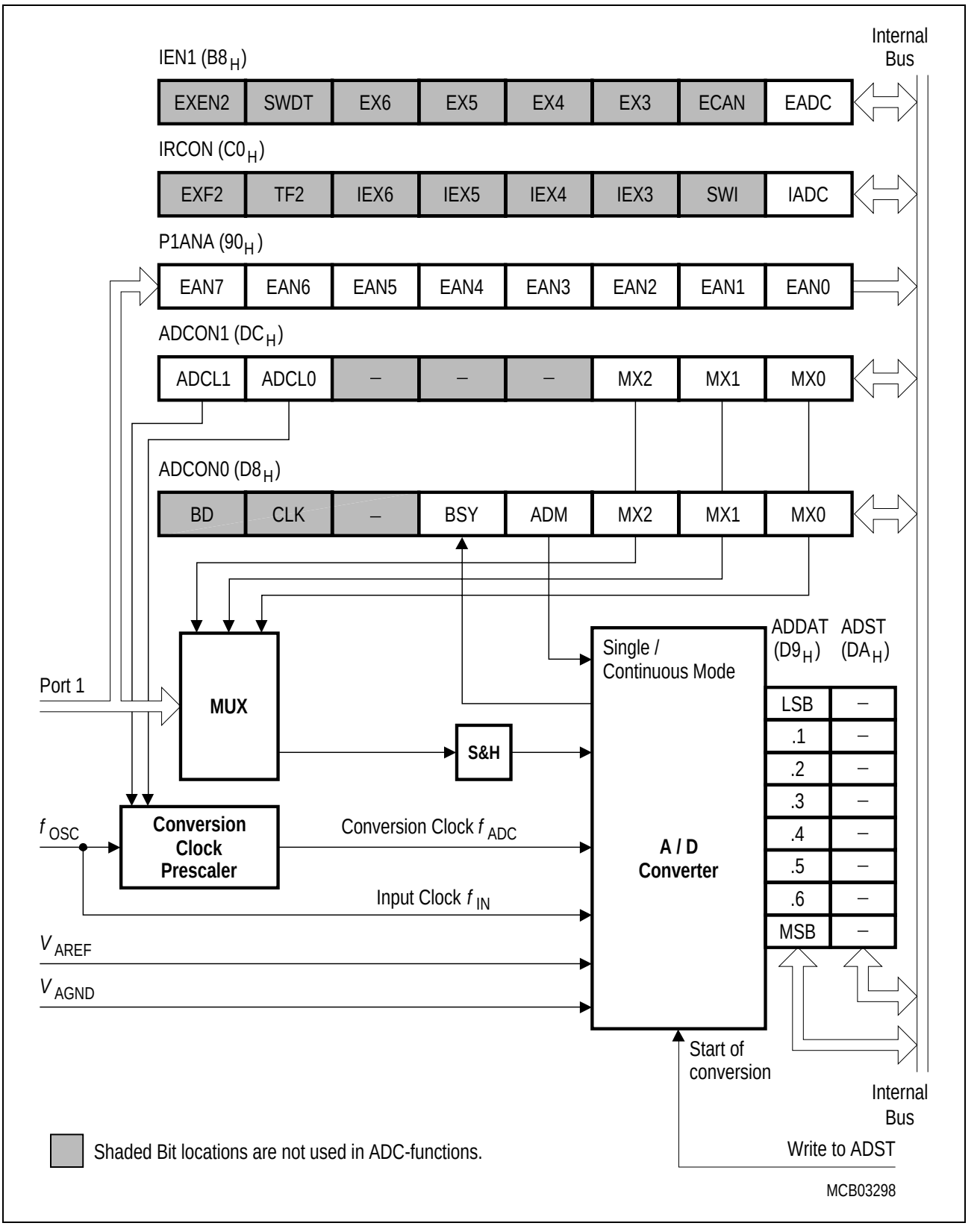


Figure 18
Block Diagram of the 8-Bit A/D Converter

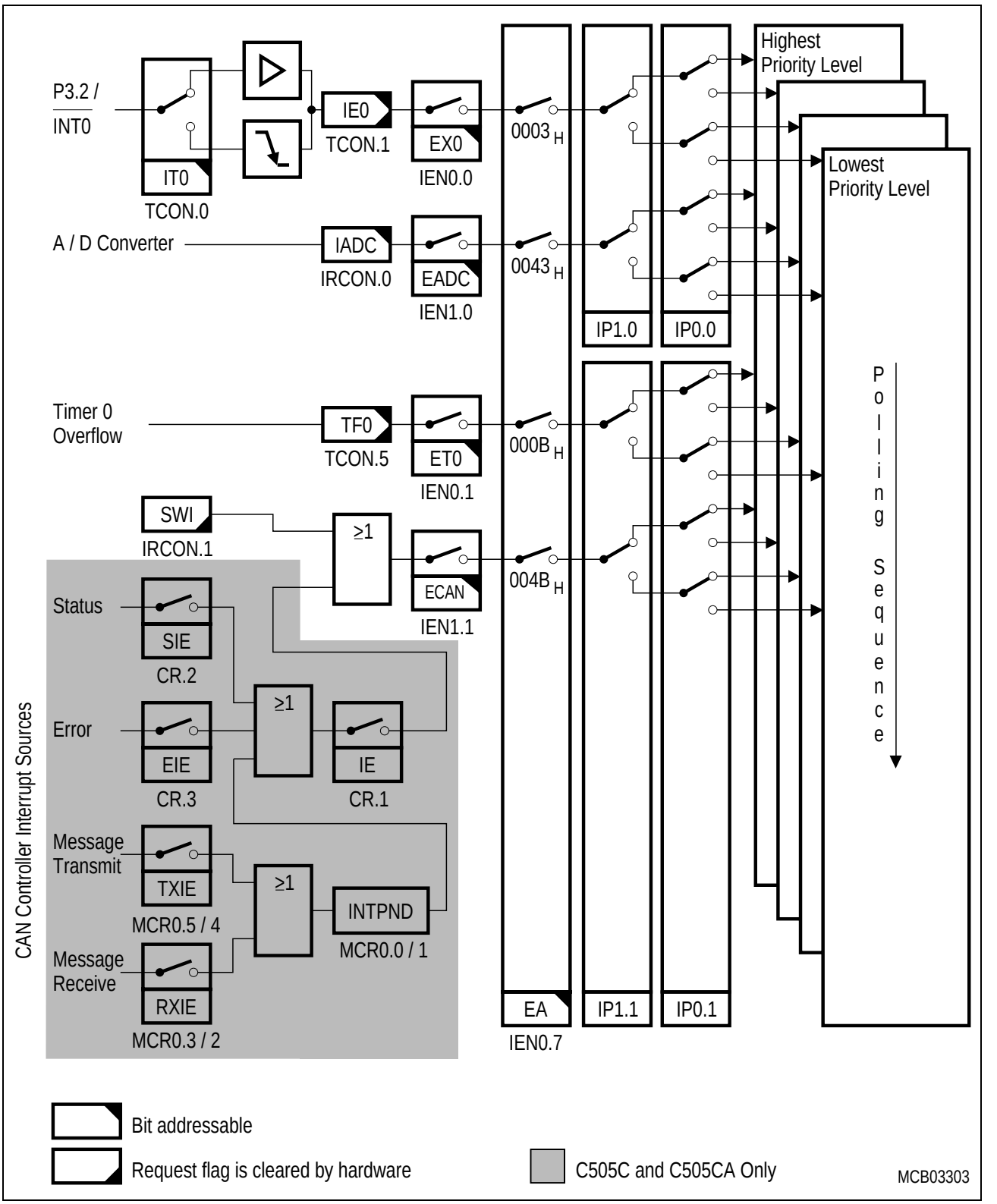


Figure 21
Interrupt Structure, Overview Part 1

*Note: Each of the 15 CAN controller message objects (C505C and C505CA only), shown in the shaded area of **Figure 21** provides the bits/flags.*

Power Supply Currents

Parameter			Symbol	Limit Values		Unit	Test Condition
				typ.[12]	max.[13]		
C505 / C505C	Active Mode	12 MHz 20 MHz	I_{DD} I_{DD}	19.3 31.3	27.0 39	mA	[7]
	Idle Mode	12 MHz 20 MHz	I_{DD} I_{DD}	10.3 16.2	13.0 21.0	mA	[8]
	Active Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.9 4.8	5.5 7.5	mA	[9]
	Idle Mode with slow-down enabled	12 MHz 20 MHz	I_{DD} I_{DD}	3.2 4.0	5.0 7.0	mA	[10]
	Power down mode		I_{PD}	10	50	µA	V_{DD} = 2..5.5 V [11]
C505A-4E /C505CA-4E	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	28.7 35.2	30.7 37.6	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	14.9 17.7	15.9 18.9	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	9.9 12.3	12.8 15.6	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.1 6.3	5.6 6.8	mA	[10]
	Power down mode		I_{PD}	5.6	20	µA	V_{DD} = 2..5.5 V [11]
C505A-4R / C505CA-4R /C505A-2R / C505CA-2R /C505A-L / C505CA-L	Active Mode	16 MHz 20 MHz	I_{DD} I_{DD}	22.8 27.6	29.2 35.3	mA	[7]
	Idle Mode	16 MHz 20 MHz	I_{DD} I_{DD}	12.7 15.0	16.3 19.3	mA	[8]
	Active Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	6.6 7.3	8.2 9.3	mA	[9]
	Idle Mode with slow-down enabled	16 MHz 20 MHz	I_{DD} I_{DD}	5.0 5.3	5.9 6.5	mA	[10]
	Power down mode		I_{PD}	5.3	30	µA	V_{DD} = 2..5.5 V [11]

Notes see **Page 60**

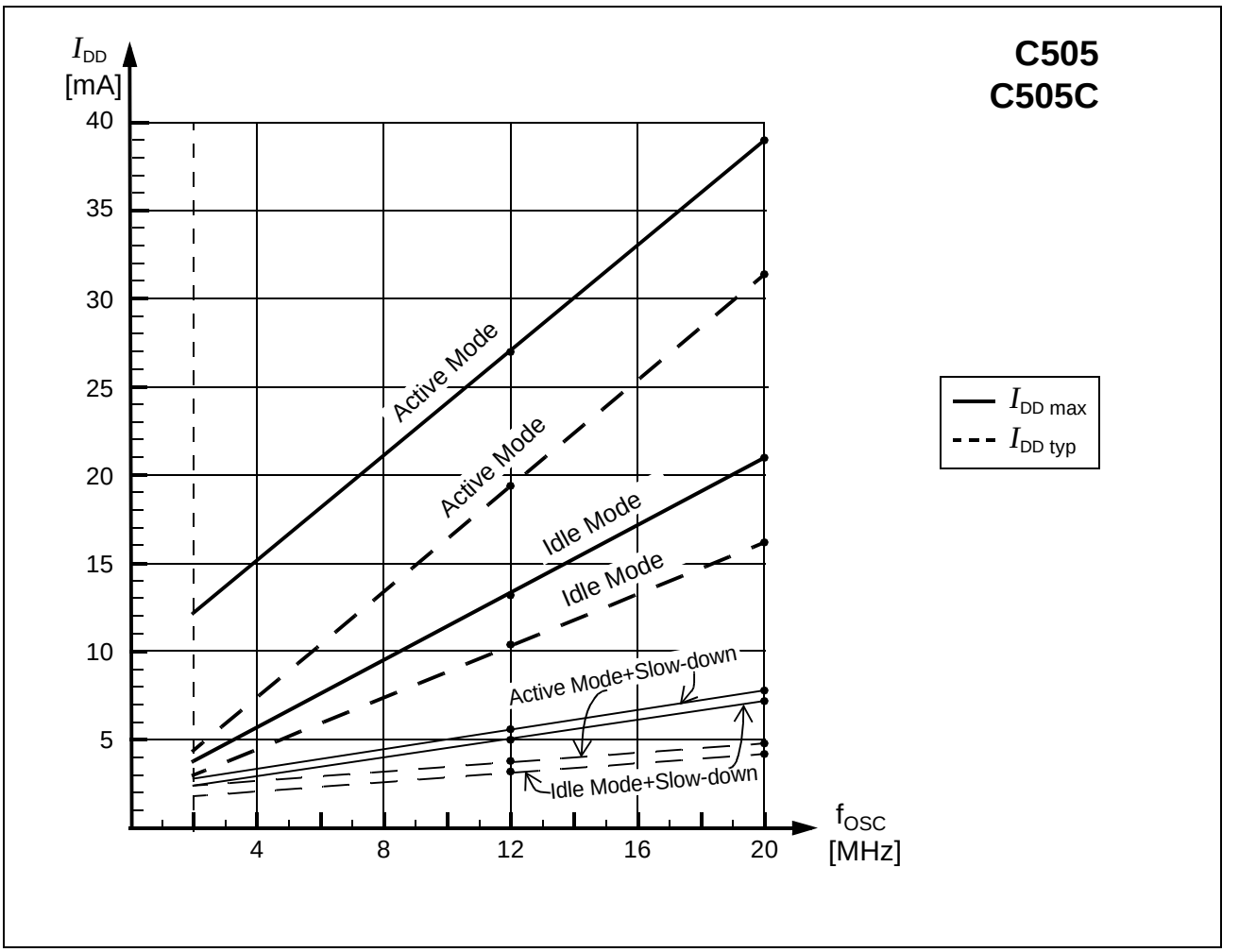


Figure 29
I_{DD} Diagram of C505 and C505C

C505/C505C : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.5 * f_{OSC} + 1.3$ $1.5 * f_{OSC} + 9.0$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.74 * f_{OSC} + 1.4$ $1.0 * f_{OSC} + 1.0$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.11 * f_{OSC} + 2.6$ $0.25 * f_{OSC} + 2.5$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.1 * f_{OSC} + 2.0$ $0.25 * f_{OSC} + 2.0$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

Note:

1) V_{AIN} may exeed V_{AGND} or V_{AREF} up to the absolute maximum ratings. However, the conversion result in these cases will be 00_H or FF_H, respectively.

2) During the sample time the input capacitance C_{AIN} must be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach their final voltage level within t_S. After the end of the sample time t_S, changes of the analog input voltage have no effect on the conversion result.

3) This parameter includes the sample time t_S, the time for determining the digital result. Values for the conversion clock t_{ADC} depend on programming and can be taken from the table on the previous page.

4) T_{UE} (max.) is tested at $-40 \le T_A \le 125$ °C ; $V_{DD} \le 5.5$ V; $V_{AREF} \le V_{DD} + 0.1$ V and $V_{SS} \le V_{AGND}$. It is guaranteed by design characterization for all other voltages within the defined voltage range.
If an overload condition occurs on maximum 2 unused analog input pins and the absolute sum of input overload currents on all analog input pins does not exceed 10 mA, an additional conversion error of 1/2 LSB is permissible.

5) During the conversion the ADC's capacitance must be repeatedly charged or discharged. The internal resistance of the reference source must allow the capacitance to reach their final voltage level within the indicated time. The maximum internal resistance results from the programmed conversion timing.

6) Not 100% tested, but guaranteed by design characterization.

AC Characteristics (16 MHz, 0.4 to 0.6 Duty Cycle)

(Operating Conditions apply)

(C_L for port 0, ALE and $\overline{\text{PSEN}}$ outputs = 100 pF; C_L for all other outputs = 80 pF)

Program Memory Characteristics

Parameter	Symbol	Limit Values				Unit
		16-MHz clock Duty Cycle 0.4 to 0.6		Variable Clock 1/CLP= 2 MHz to 16 MHz		
		min.	max.	min.	max.	
ALE pulse width	t_{LHLL}	48	–	CLP - 15	–	ns
Address setup to ALE	t_{AVLL}	10	–	TCL_{Hmin} -15	–	ns
Address hold after ALE	t_{LLAX}	10	–	TCL_{Hmin} -15	–	ns
ALE to valid instruction in	t_{LLIV}	–	75	–	2 CLP - 50	ns
ALE to $\overline{\text{PSEN}}$	t_{LLPL}	10	–	TCL_{Lmin} -15	–	ns
$\overline{\text{PSEN}}$ pulse width	t_{PLPH}	73	–	CLP+ TCL_{Hmin} -15	–	ns
$\overline{\text{PSEN}}$ to valid instruction in	t_{PLIV}	–	38	–	CLP+ TCL_{Hmin}- 50	ns
Input instruction hold after $\overline{\text{PSEN}}$	t_{PXIX}	0	–	0	–	ns
Input instruction float after $\overline{\text{PSEN}}$	t_{PXIZ} *)	–	15	–	TCL_{Lmin} -10	ns
Address valid after $\overline{\text{PSEN}}$	t_{PXAV} *)	20	–	TCL_{Lmin} - 5	–	ns
Address to valid instruction in	t_{AVIV}	–	95	–	2 CLP + TCL_{Hmin} -55	ns
Address float to $\overline{\text{PSEN}}$	t_{AZPL}	-5	–	-5	–	ns

*) Interfacing the C505 to devices with float times up to 20 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

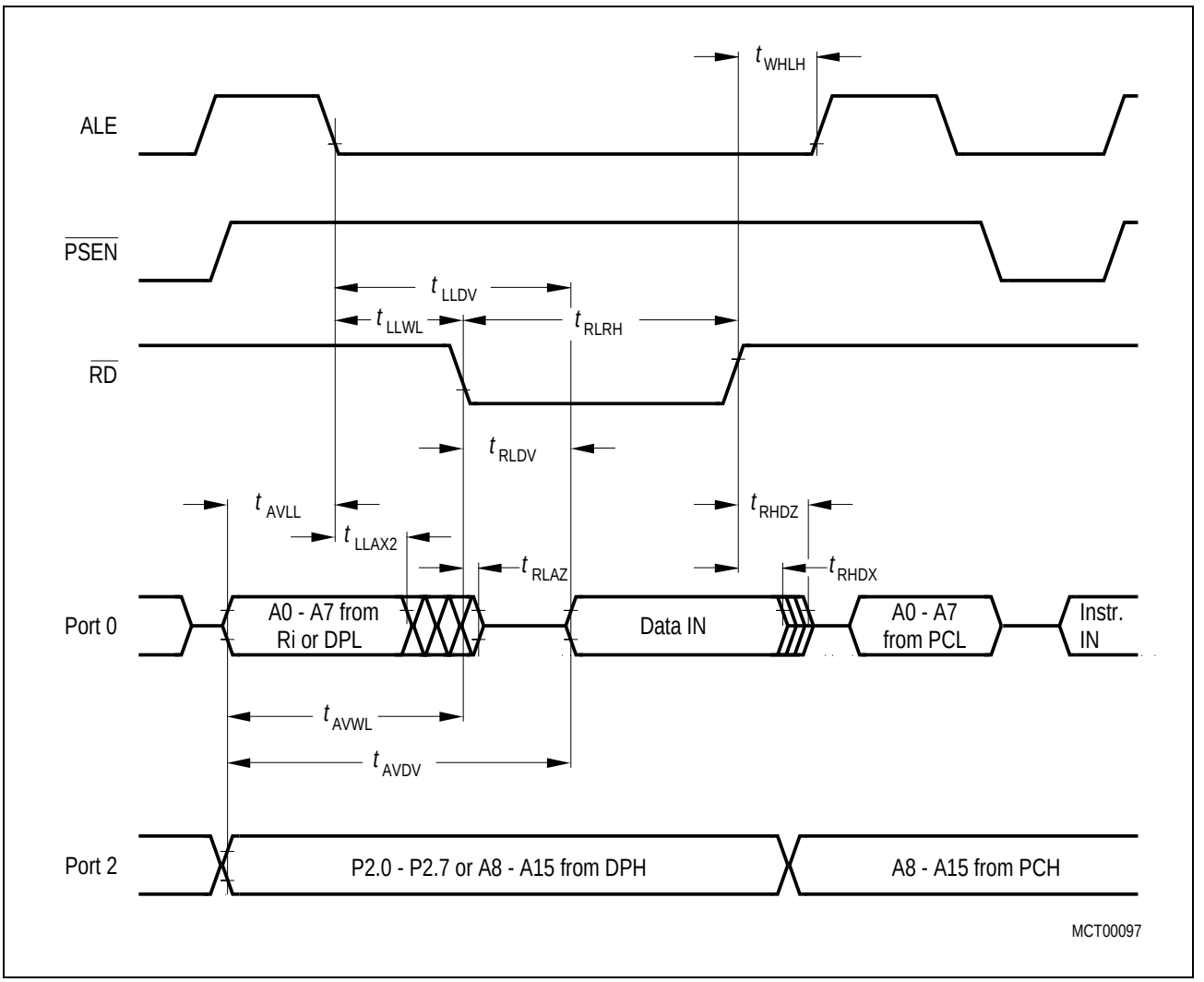


Figure 33
Data Memory Read Cycle

ROM/OTP Verification Characteristics for C505 (cont'd)

ROM/OTP Verification Mode 2

Parameter	Symbol	Limit Values			Unit
		min.	typ	max.	
ALE pulse width	t_{AWD}	–	CLP	–	ns
ALE period	t_{ACY}	–	6 CLP	–	ns
Data valid after ALE	t_{DVA}	–	–	2 CLP	ns
Data stable after ALE	t_{DSA}	4 CLP	–	–	ns
P3.5 setup to ALE low	t_{AS}	–	t_{CL}	–	ns
Oscillator frequency	1/ CLP	4	–	6	MHz

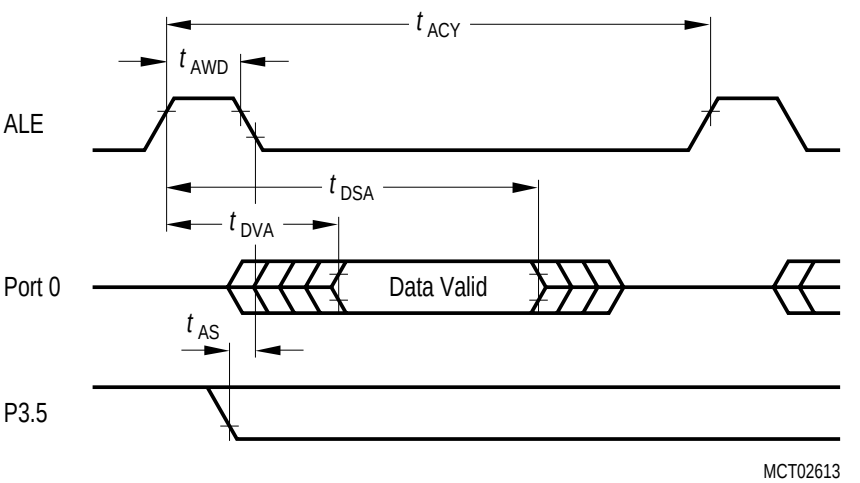


Figure 41
ROM/OTP Verification Mode 2