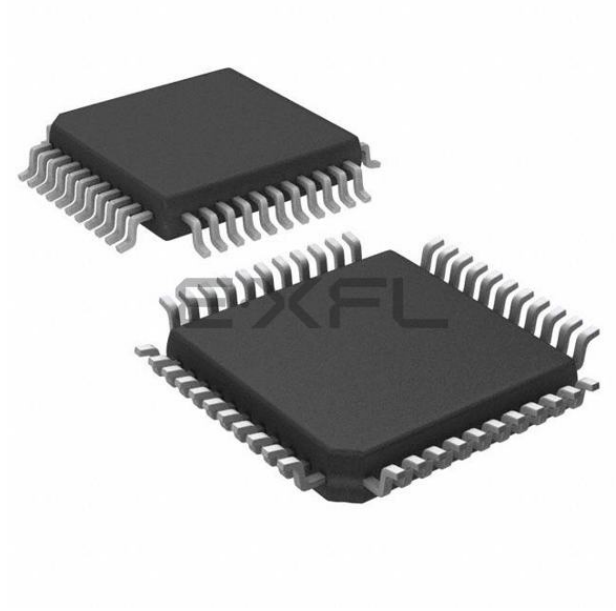
Infineon Technologies - C505CALMCAFXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C500
Core Size	8-Bit
Speed	20MHz
Connectivity	CANbus, EBI/EMI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	34
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	4.25V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	PG-MQFP-44-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/c505calmcafxuma1

Data Sheet, Dec. 2000

C505

C505C

C505A

C505CA

8-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking.

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
RESET	4	I	**RESET** A high level on this pin for two machine cycle while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits power-on reset using only an external capacitor to V_{DD}.
P3.0-P3.7	5, 7-13	I/O	**Port 3** is an 8-bit quasi-bidirectional port with internal pull-up arrangement. Port 3 pins that have 1's written to them are pulled high by the internal pull-up transistors and in that state can be used as inputs. As inputs, port 3 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup transistors. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate (except for TxD and $\overline{WR}$). The secondary functions are assigned to the pins of port 3 as follows:
	5		P3.0 / RxD — Receiver data input (asynch.) or data input/output (synch.) of serial interface
	7		P3.1 / TxD — Transmitter data output (asynch.) or clock output (synch.) of serial interface
	8		P3.2 / $\overline{INT0}$ — External interrupt 0 input / timer 0 gate control input
	9		P3.3 / $\overline{INT1}$ — External interrupt 1 input / timer 1 gate control input
	10		P3.4 / T0 — Timer 0 counter input
	11		P3.5 / T1 — Timer 1 counter input
	12		P3.6 / $\overline{WR}$ — $\overline{WR}$ control output; latches the data byte from port 0 into the external data memory
	13		P3.7 / $\overline{RD}$ — $\overline{RD}$ control output; enables the external data memory

*) I = Input
O = Output

Table 2
Pin Definitions and Functions (cont'd)

Symbol	Pin Number	I/O *)	Function
P2.0-P2.7	18-25	I/O	**Port 2** is a an 8-bit quasi-bidirectional I/O port with internal pullup resistors. Port 2 pins that have 1's written to them are pulled high by the internal pullup resistors, and in that state can be used as inputs. As inputs, port 2 pins being externally pulled low will source current (I_{IL}, in the DC characteristics) because of the internal pullup resistors. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullup transistors when issuing 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), port 2 issues the contents of the P2 special function register and uses only the internal pullup resistors.
$\overline{\text{PSEN}}$	26	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every three oscillator periods except during external data memory accesses. Remains high during internal program execution. This pin should not be driven during reset operation.
ALE	27	O	The **Address Latch Enable** output is used for latching the low-byte of the address into external memory during normal operation. It is activated every three oscillator periods except during an external data memory access. When instructions are executed from internal ROM or OTP ($\overline{\text{EA}}$=1) the ALE generation can be disabled by bit EALE in SFR SYSCON. ALE should not be driven during reset operation.

*) I = Input
O = Output

Figure 7 shows the recommended oscillator circuits for crystal and external clock operation.

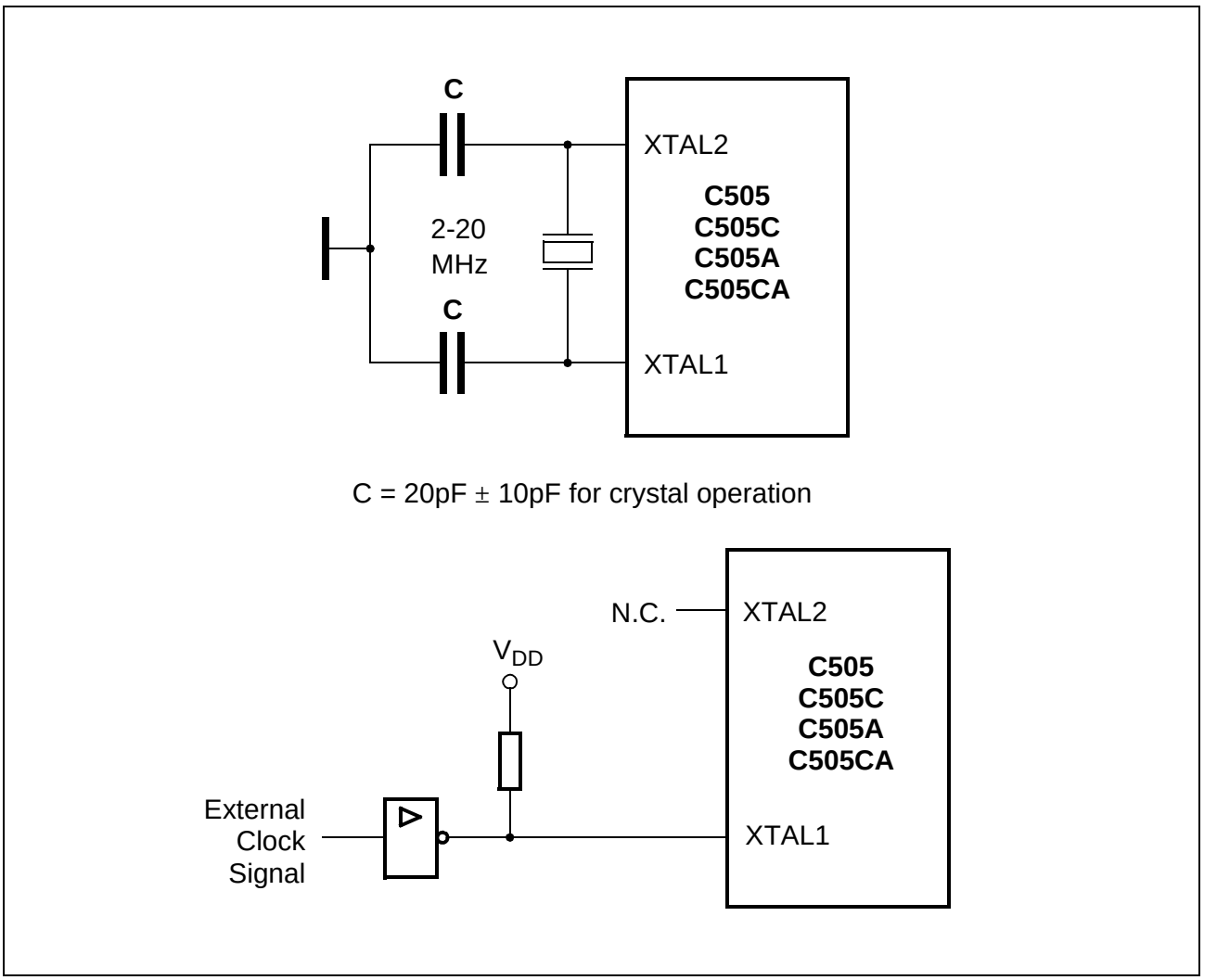


Figure 7
Recommended Oscillator Circuitries

Enhanced Hooks Emulation Concept

The Enhanced Hooks Emulation Concept of the C500 microcontroller family is a new, innovative way to control the execution of C500 MCUs and to gain extensive information on the internal operation of the controllers. Emulation of on-chip ROM based programs is possible, too.

Each production chip has built-in logic for the supprt of the Enhanced Hooks Emulation Concept. Therefore, no costly bond-out chips are necessary for emulation. This also ensure that emulation and production chips are identical.

The Enhanced Hooks Technology™ [1], which requires embedded logic in the C500 allows the C500 together with an EH-IC to function similar to a bond-out chip. This simplifies the design and reduces costs of an ICE-system. ICE-systems using an EH-IC and a compatible C500 are able to emulate all operating modes of the different versions of the C500 microcontrollers. This includes emulation of ROM, ROM with code rollover and ROMless modes of operation. It is also able to operate in single step mode and to read the SFRs after a break.

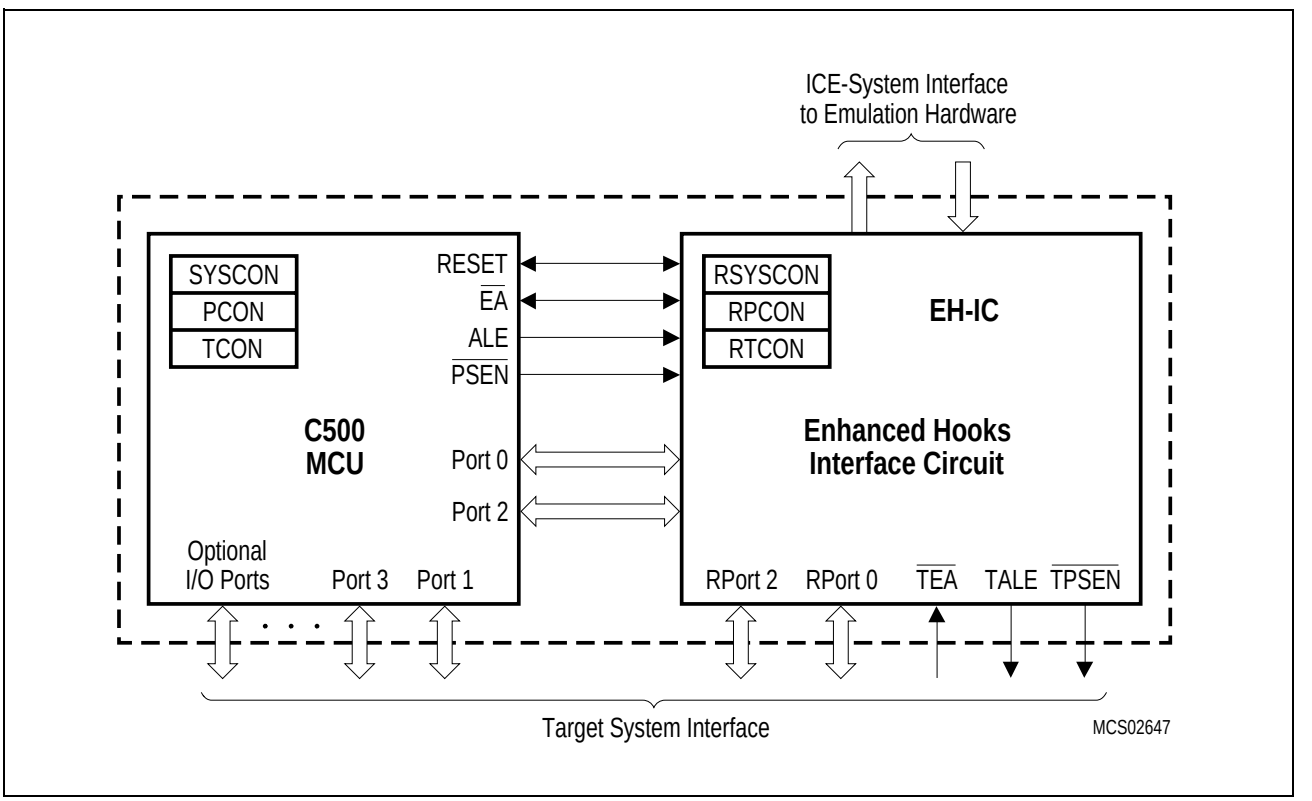


Figure 9
Basic C500 MCU Enhanced Hooks Concept Configuration

Port 0, port 2 and some of the control lines of the C500 based MCU are used by Enhanced Hooks Emulation Concept to control the operation of the device during emulation and to transfer informations about the programm execution and data transfer between the external emulation hardware (ICE-system) and the C500 MCU.

[1] "Enhanced Hooks Technology" is a trademark and patent of Metalink Corporation licensed to Infineon Technologies.

Table 4
Contents of the SFRs, SFRs in numeric order of their addresses

Addr	Register	Content after Reset[1)]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80_H [2)]	P0	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
81_H	SP	07_H	.7	.6	.5	.4	.3	.2	.1	.0
82_H	DPL	00_H	.7	.6	.5	.4	.3	.2	.1	.0
83_H	DPH	00_H	.7	.6	.5	.4	.3	.2	.1	.0
86_H	WDTREL	00_H	WDT PSEL	.6	.5	.4	.3	.2	.1	.0
87_H	PCON	00_H	SMOD	PDS	IDLS	SD	GF1	GF0	PDE	IDLE
88_H [2)]	TCON	00_H	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
88_H [3)]	PCON1	$0XX0\text{-}XXXX_B$	EWPD	–	–	WS	–	–	–	–
89_H	TMOD	00_H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
$8A_H$	TL0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8B_H$	TL1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8C_H$	TH0	00_H	.7	.6	.5	.4	.3	.2	.1	.0
$8D_H$	TH1	00_H	.7	.6	.5	.4	.3	.2	.1	.0
90_H [2)]	P1	FF_H	T2	CLK-OUT	T2EX	.4	INT6	INT5	INT4	.$\overline{INT3}$
90_H [3)]	P1ANA	FF_H	EAN7	EAN6	EAN5	EAN4	EAN3	EAN2	EAN1	EAN0
91_H	XPAGE	00_H	.7	.6	.5	.4	.3	.2	.1	.0
92_H	DPSEL	$XXXX\text{-}X000_B$	–	–	–	–	–	.2	.1	.0
98_H [2)]	SCON	00_H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99_H	SBUF	XX_H	.7	.6	.5	.4	.3	.2	.1	.0
$A0_H$ [2)]	P2	FF_H	.7	.6	.5	.4	.3	.2	.1	.0
$A8_H$ [2)]	IEN0	00_H	EA	WDT	ET2	ES	ET1	EX1	ET0	EX0
$A9_H$	IP0	00_H	OWDS	WDTS	.5	.4	.3	.2	.1	.0
AA_H	SRELL	$D9_H$	.7	.6	.5	.4	.3	.2	.1	.0

1) X means that the value is undefined and the location is reserved
2) Bit-addressable special function registers
3) SFR is located in the mapped SFR area. For accessing this SFR, bit RMAP in SFR SYSCON must be set.

I/O Ports

The C505 has four 8-bit I/O ports and one 2-bit I/O port. Port 0 is an open-drain bidirectional I/O port, while ports 1 to 4 are quasi-bidirectional I/O ports with internal pullup resistors. That means, when configured as inputs, ports 1 to 4 will be pulled high and will source current when externally pulled low. Port 0 will float when configured as input.

The output drivers of port 0 and 2 and the input buffers of port 0 are also used for accessing external memory. In this application, port 0 outputs the low byte of the external memory address, time multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise, the port 2 pins continue emitting the P2 SFR contents. In this function, port 0 is not an open-drain port, but uses a strong internal pullup FET .

Port 4 is 2-bit I/O port with CAN controller specific alternate functions. The eight analog input lines are realized as mixed digital/analog inputs. The 8 analog inputs, AN0-AN7, are located at the port 1 pins P1.0 to P1.7. After reset, all analog inputs are disabled and the related pins of port 1 are configured as digital inputs. The analog function of a specific port 1 pin is enabled by bits in the SFR P1ANA. Writing a 0 to a bit position of P1ANA assigns the corresponding pin to operate as analog input.

Note : P1ANA is a mapped SFR and can be only accessed if bit RMAP in SFR SYSCON is set.

Timer / Counter 0 and 1

Timer/Counter 0 and 1 can be used in four operating modes as listed in **Table 6** :

Table 6
Timer/Counter 0 and 1 Operating Modes

Mode	Description	TMOD		Input Clock	
		M1	M0	internal	external (max)
0	8-bit timer/counter with a divide-by-32 prescaler	0	0	f_{osc}/6x32	f_{osc}/12x32
1	16-bit timer/counter	0	1	f_{osc}/6	f_{osc}/12
2	8-bit timer/counter with 8-bit autoreload	1	0		
3	Timer/counter 0 used as one 8-bit timer/counter and one 8-bit timer Timer 1 stops	1	1		

In the “timer” function (C/$\overline{T}$ = ‘0’) the register is incremented every machine cycle. Therefore the count rate is f_{osc}/6.

In the “counter” function the register is incremented in response to a 1-to-0 transition at its corresponding external input pin (P3.4/T0, P3.5/T1). Since it takes two machine cycles to detect a falling edge the max. count rate is f_{osc}/12. External inputs $\overline{INT0}$ and $\overline{INT1}$ (P3.2, P3.3) can be programmed to function as a gate to facilitate pulse width measurements. **Figure 10** illustrates the input clock logic.

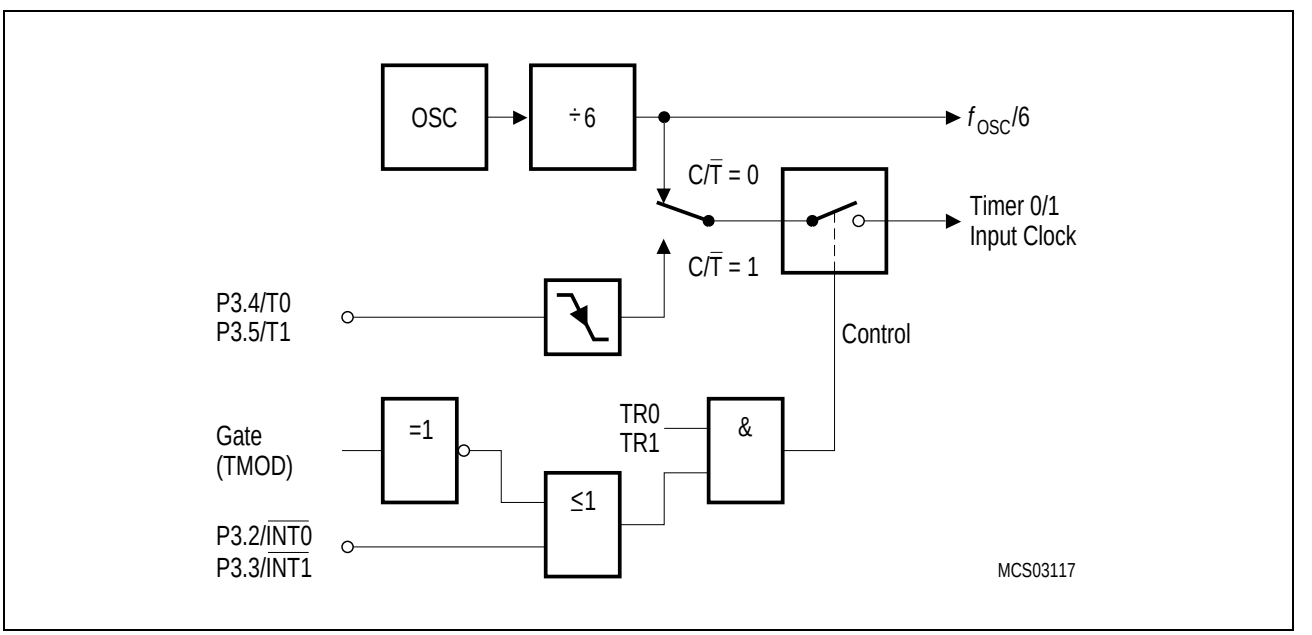


Figure 10
Timer/Counter 0 and 1 Input Clock Logic

Serial Interface (USART)

The serial port is full duplex and can operate in four modes (one synchronous mode, three asynchronous modes) as illustrated in **Table 7**.

Table 7
USART Operating Modes

Mode	SCON		Description
	SM0	SM1	
0	0	0	Shift register mode, fixed baud rate Serial data enters and exits through R×D; T×D outputs the shift clock; 8-bit are transmitted/received (LSB first)
1	0	1	8-bit UART, variable baud rate 10 bits are transmitted (through T×D) or received (at R×D)
2	1	0	9-bit UART, fixed baud rate 11 bits are transmitted (through T×D) or received (at R×D)
3	1	1	9-bit UART, variable baud rate Like mode 2

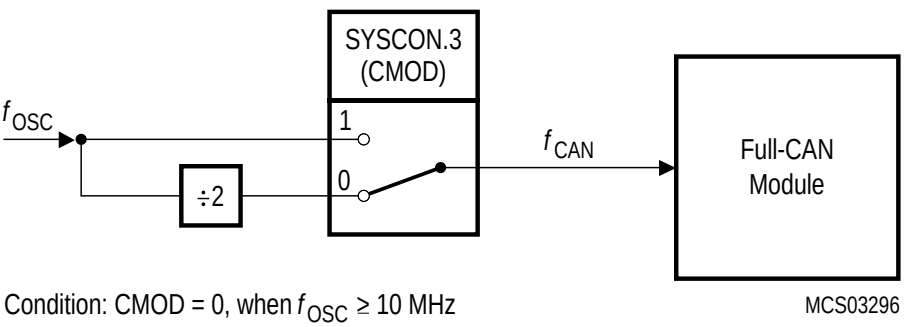
For clarification some terms regarding the difference between "baud rate clock" and "baud rate" should be mentioned. In the asynchronous modes the serial interfaces require a clock rate which is 16 times the baud rate for internal synchronization. Therefore, the baud rate generators/timers have to provide a "baud rate clock" (output signal in **Figure 14** to the serial interface which - there divided by 16 - results in the actual "baud rate". Further, the abbrevation f_{OSC} refers to the oscillator frequency (crystal or external clock operation).

The variable baud rates for modes 1 and 3 of the serial interface can be derived either from timer 1 or from a decdicated baud rate generator (see **Figure 14**).

CAN Controller Software Initialization

The very first step of the initialization is the CAN controller input clock selection. A divide-by-2 prescaler is enabled by default after reset (**Figure 16**). Setting bit CMOD (SYSCON.3) disables the prescaler. The purpose of the prescaler selection is:

– to ensure that the CAN controller is operable when f_{OSC} is over 10 MHz (bit CMOD =0)
– to achieve the maximum CAN baudrate of 1 Mbaud when f_{OSC} is 8 MHz (bit CMOD=1)



Frequency (MHz)		CMOD (SYSCON.3)	BRP (BTR0.0-5)	CAN baudrate (Mbaud/sec)
f_{OSC}	f_{CAN}			
8	8	1	000000_B	1
8	4	0	000000_B	0.5
16	8	0	000000_B	1

Note : The switch configuration shows the reset state of bit CMOD.

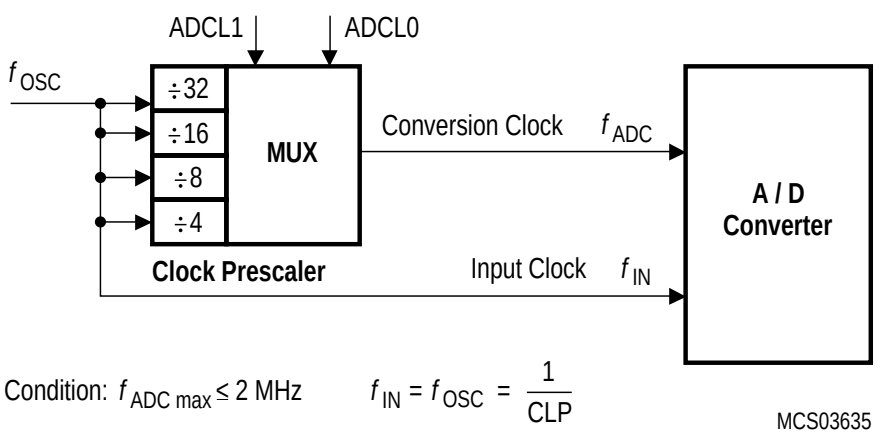
Figure 16
CAN controller Input Clock Selection

10-Bit A/D Converter (C505A and C505CA only)

The C505A/C505CA includes a high performance / high speed 10-bit A/D-Converter (ADC) with 8 analog input channels. It operates with a successive approximation technique and uses self calibration mechanisms for reduction and compensation of offset and linearity errors. The A/D converter provides the following features:

- 8 multiplexed input channels (port 1), which can also be used as digital inputs/outputs
- 10-bit resolution
- Single or continuous conversion mode
- Internal start-of-conversion trigger capability
- Interrupt request generation after each conversion
- Using successive approximation conversion technique via a capacitor array
- Built-in hidden calibration of offset and linearity errors

The 10-bit ADC uses two clock signals for operation : the conversion clock f_{ADC} (=1/t_{ADC}) and the input clock f_{IN} (=1/t_{IN}). f_{ADC} is derived from the C505 system clock f_{OSC} which is applied at the XTAL pins. The input clock f_{IN} is equal to f_{OSC} The conversion f_{ADC} clock is limited to a maximum frequency of 2 MHz. Therefore, the ADC clock prescaler must be programmed to a value which assures that the conversion clock does not exceed 2 MHz. The prescaler ratio is selected by the bits ADCL1 and ADCL0 of SFR ADCON1.



MCU System Clock Rate (f_{OSC})	f_{IN} [MHz]	Prescaler Ratio	f_{ADC} [MHz]	ADCL1	ADCL0
2 MHz	2	÷ 4	0.5	0	0
6 MHz	6	÷ 4	1.5	0	0
8 MHz	8	÷ 4	2	0	0
12 MHz	12	÷ 8	1.5	0	1
16 MHz	16	÷ 8	2	0	1
20 MHz	20	÷ 16	1.25	1	0

Figure 19
10-Bit A/D Converter Clock Selection

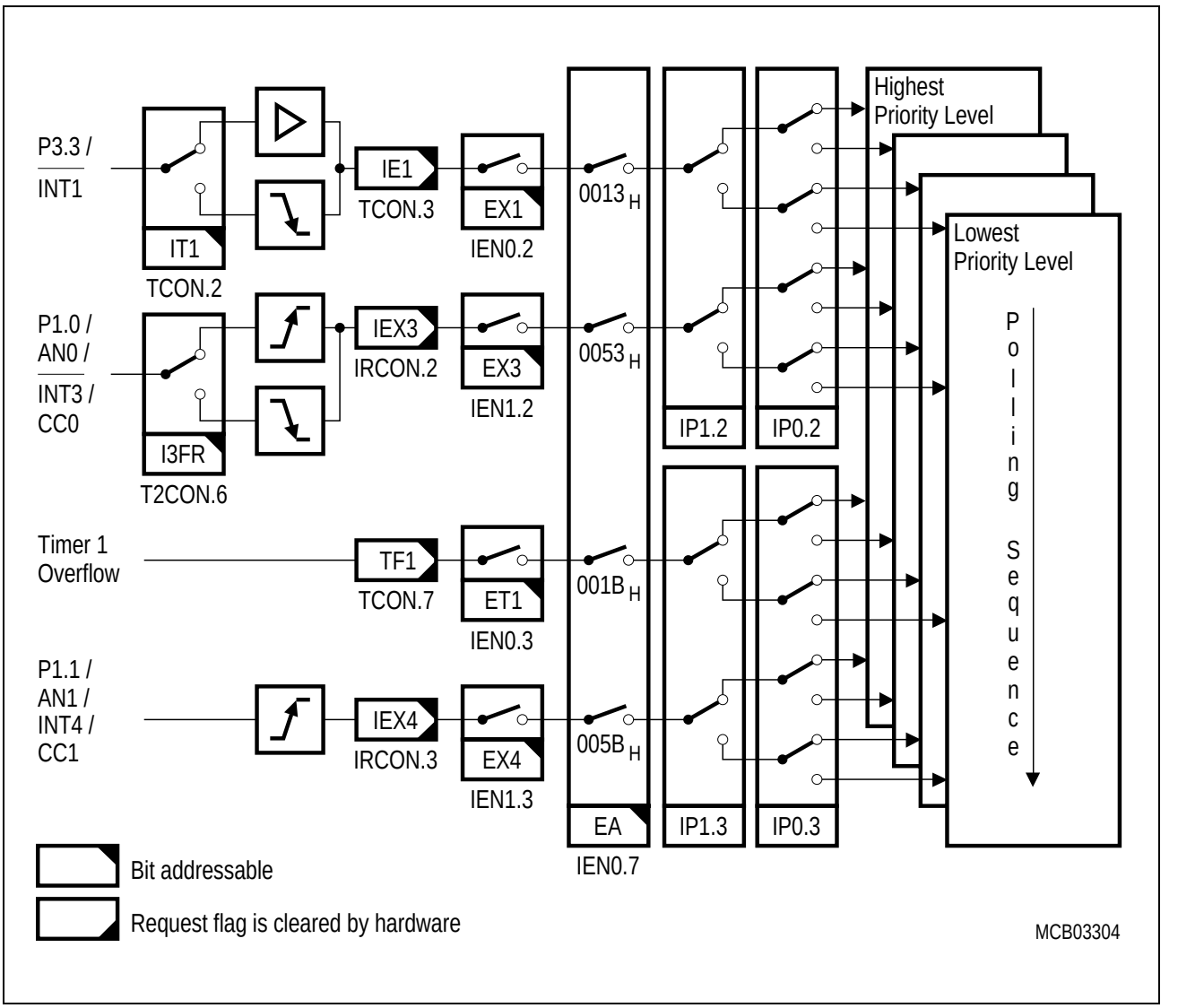


Figure 22
Interrupt Structure, Overview Part 2

Basic Programming Mode Selection

The basic programming mode selection scheme is shown in **Figure 28**.

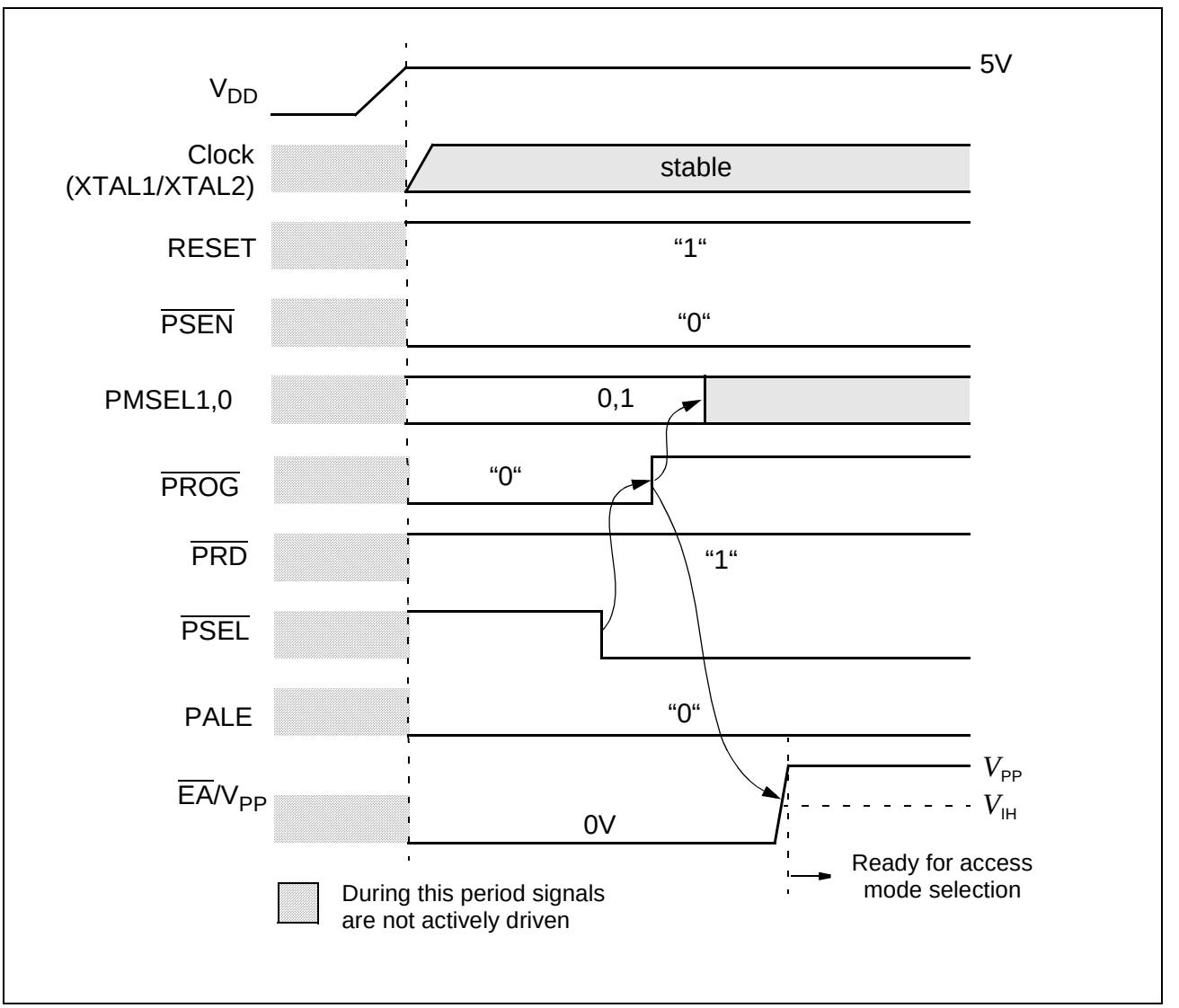


Figure 28
Basic Programming Mode Selection

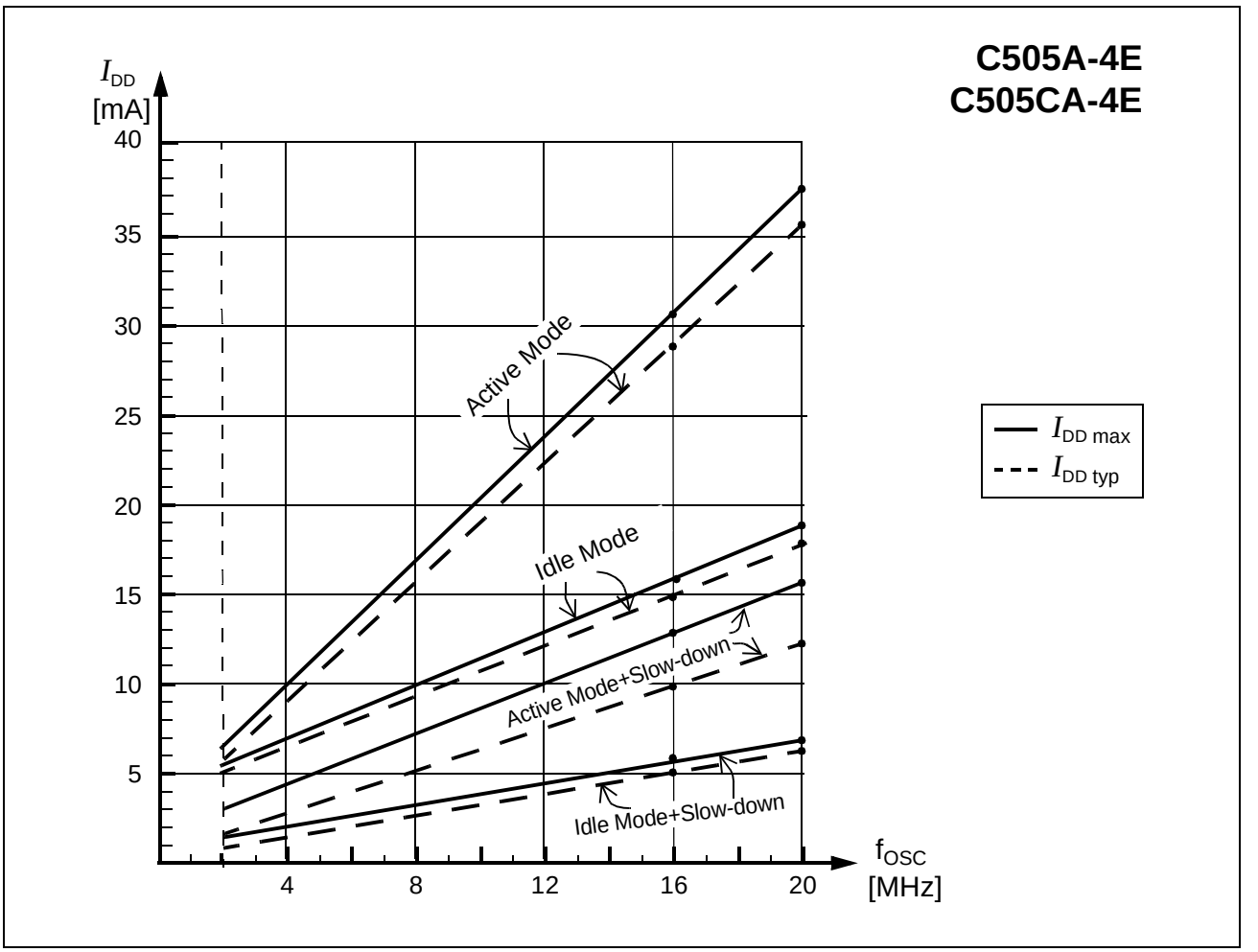


Figure 30
I_{DD} Diagram of C505A-4E and C505CA-4E

C505A-4E/C505CA-4E : Power Supply Current Calculation Formulas

Parameter	Symbol	Formula
Active mode	$I_{DD\ typ}$ $I_{DD\ max}$	$1.63 * f_{OSC} + 2.6$ $1.74 * f_{OSC} + 2.8$
Idle mode	$I_{DD\ typ}$ $I_{DD\ max}$	$0.69 * f_{OSC} + 3.9$ $0.74 * f_{OSC} + 4.1$
Active mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.6 * f_{OSC} + 0.3$ $0.7 * f_{OSC} + 1.6$
Idle mode with slow-down enabled	$I_{DD\ typ}$ $I_{DD\ max}$	$0.3 * f_{OSC} + 0.3$ $0.3 * f_{OSC} + 0.8$

Note: f_{osc} is the oscillator frequency in MHz. I_{DD} values are given in mA.

A/D Converter Characteristics of C505 and C505C

(Operating Conditions apply)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Analog input voltage	V_{AIN}	V_{AGND} - 0.2	V_{AREF} + 0.2	V	1)
Sample time	t_S	–	64 x t_{IN} 32 x t_{IN} 16 x t_{IN} 8 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 2)
Conversion cycle time	t_{ADCC}	–	320 x t_{IN} 160 x t_{IN} 80 x t_{IN} 40 x t_{IN}	ns	Prescaler ÷ 32 Prescaler ÷ 16 Prescaler ÷ 8 Prescaler ÷ 4 3)
Total unadjusted error	T_{UE}	–	± 2	LSB	V_{SS}+0.5V ≤ V_{AIN} ≤ V_{DD}-0.5V 4)
Internal resistance of reference voltage source	R_{AREF}	–	t_{ADC} / 500 - 1	kΩ	t_{ADC} in [ns] 5) 6)
Internal resistance of analog source	R_{ASRC}	–	t_S / 500 - 1	kΩ	t_S in [ns] 2) 6)
ADC input capacitance	C_{AIN}	–	50	pF	6)

Notes see next page.

Clock calculation table :

Clock Prescaler Ratio	ADCL1, 0		t_{ADC}	t_S	t_{ADCC}
÷ 32	1	1	32 x t_{IN}	64 x t_{IN}	320 x t_{IN}
÷ 16	1	0	16 x t_{IN}	32 x t_{IN}	160 x t_{IN}
÷ 8	0	1	8 x t_{IN}	16 x t_{IN}	80 x t_{IN}
÷ 4	0	0	4 x t_{IN}	8 x t_{IN}	40 x t_{IN}

Further timing conditions : t_{ADC} min = 800 ns
$t_{IN} = 1 / f_{OSC} = t_{CLP}$

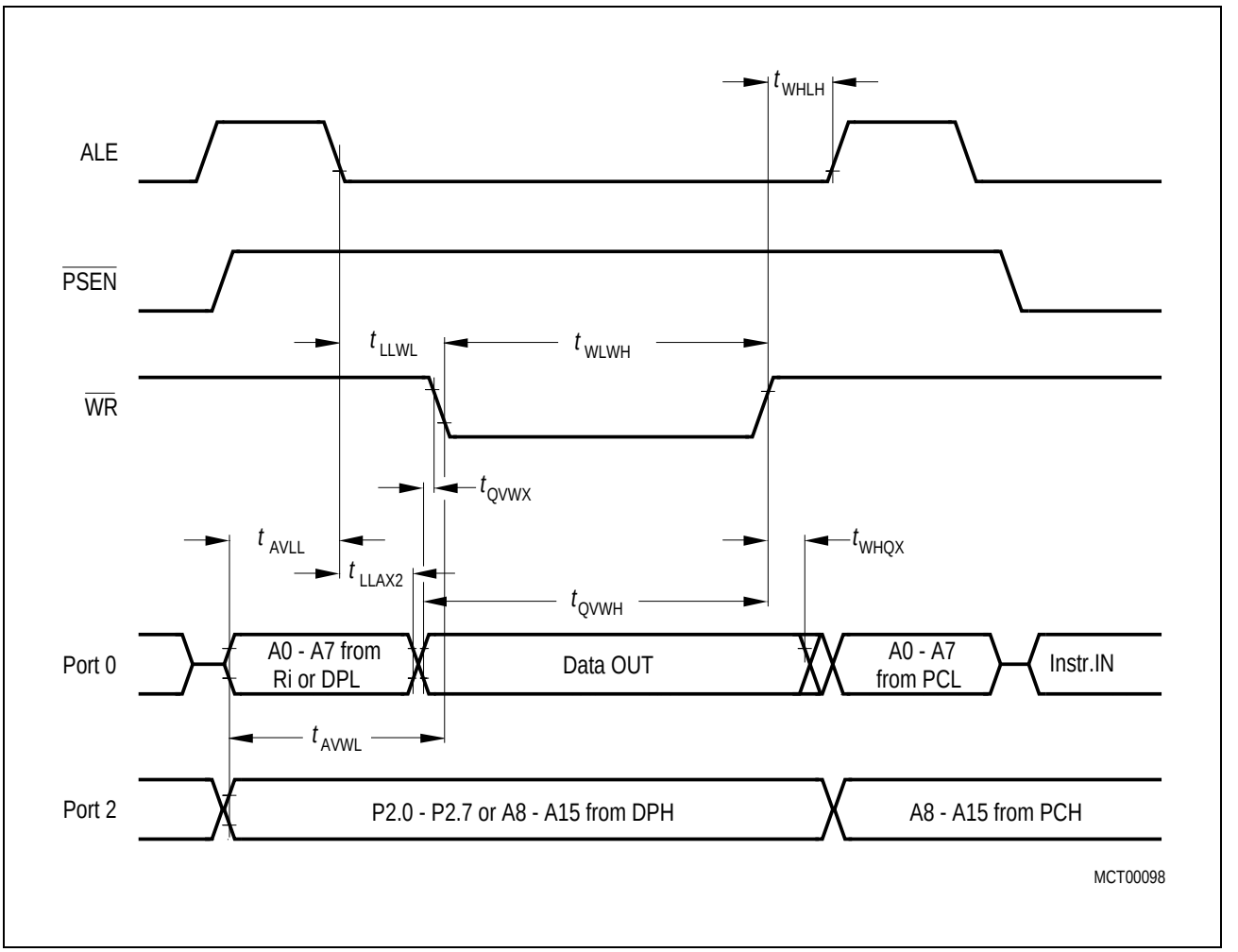


Figure 34
Data Memory Write Cycle

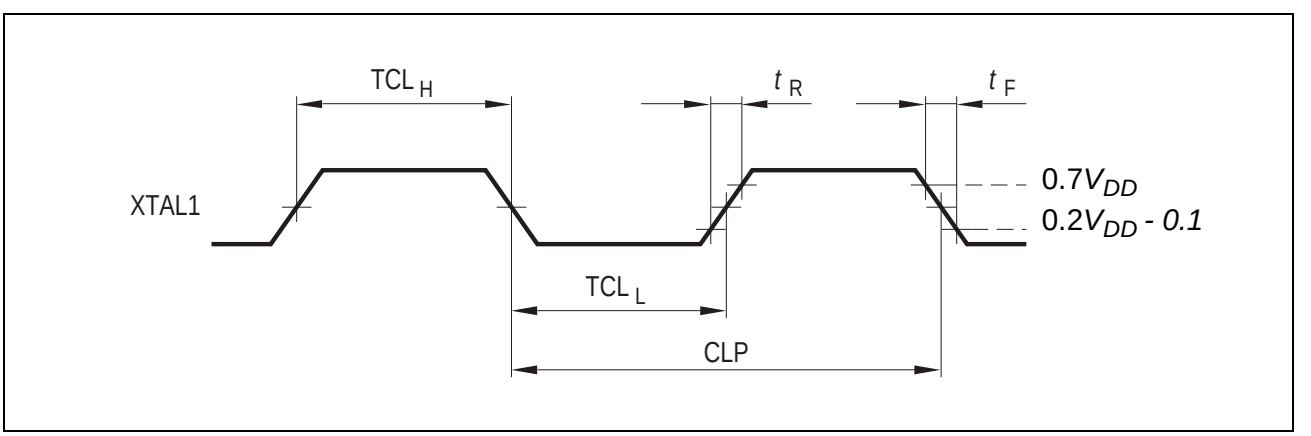


Figure 35
External Clock Drive on XTAL1

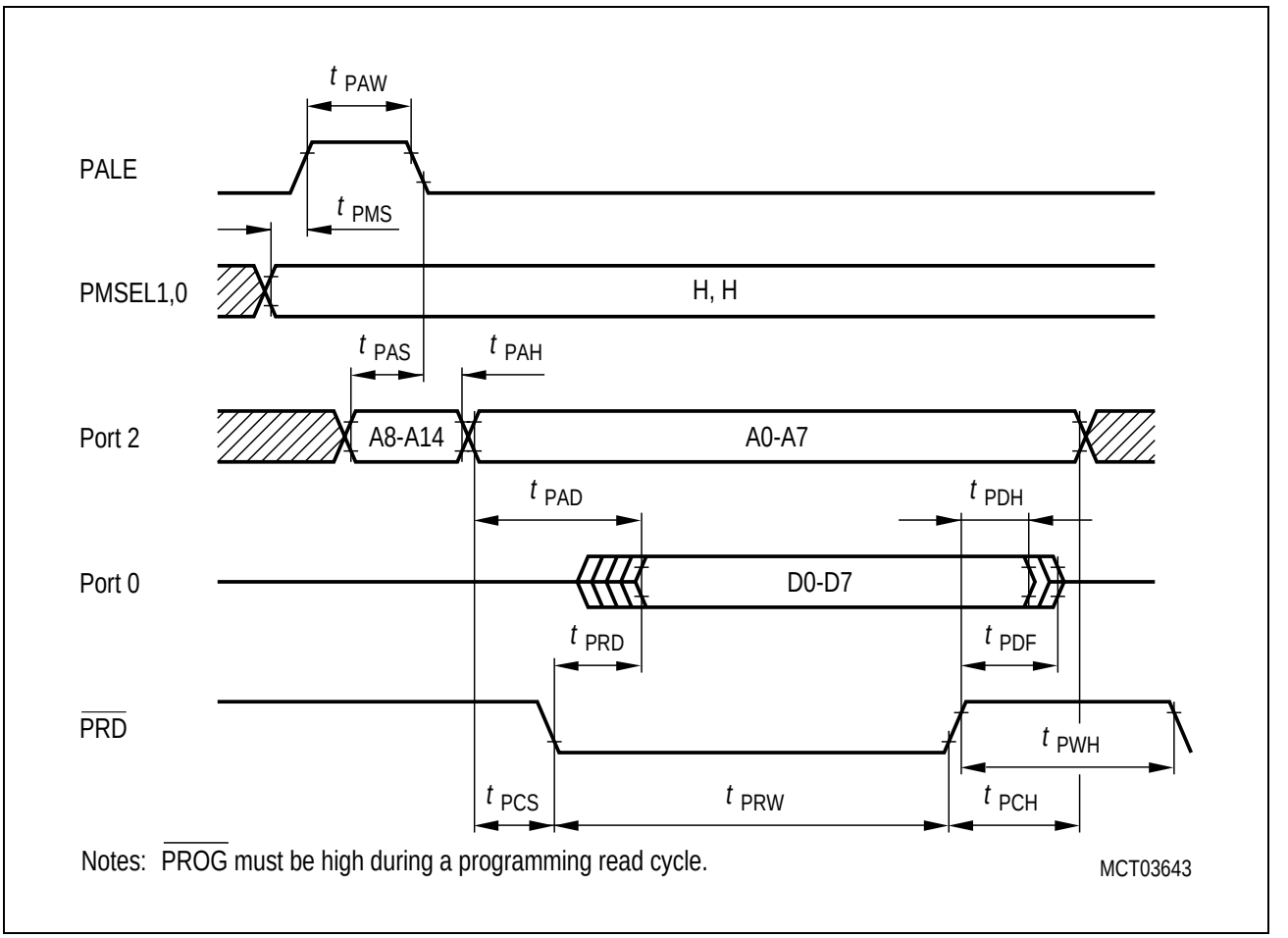
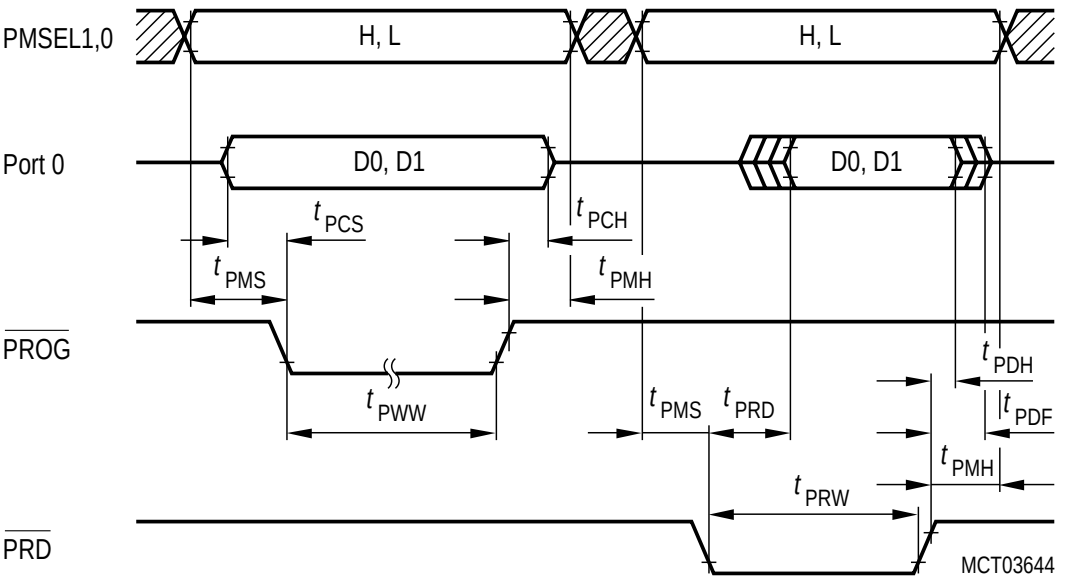
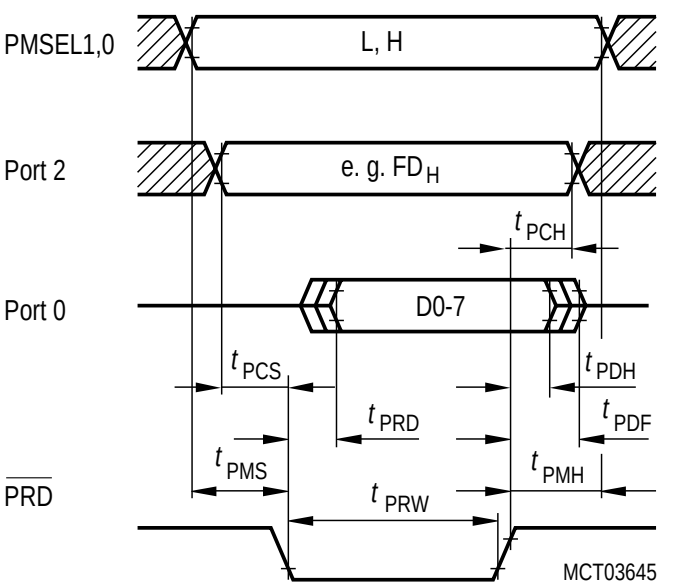


Figure 37
Verify Code Byte - Read Cycle Timing



Note: PALE should be low during a lock bit read / write cycle.

Figure 38
Lock Bit Access Timing



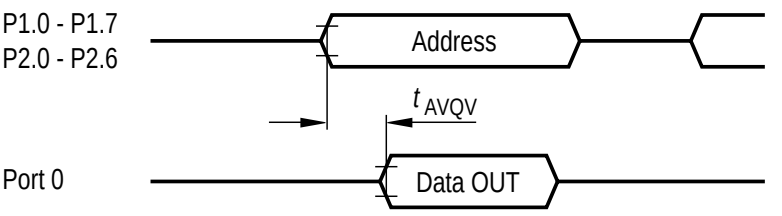
Note: $\overline{\text{PROG}}$ must be high during a programming read cycle.

Figure 39
Version Byte Read Timing

ROM/OTP Verification Characteristics for C505

ROM Verification Mode 1 (C505(C)(A)-2R and C505(C)A-4R only)

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address to valid data	t_{AVQV}	–	5 CLP	ns

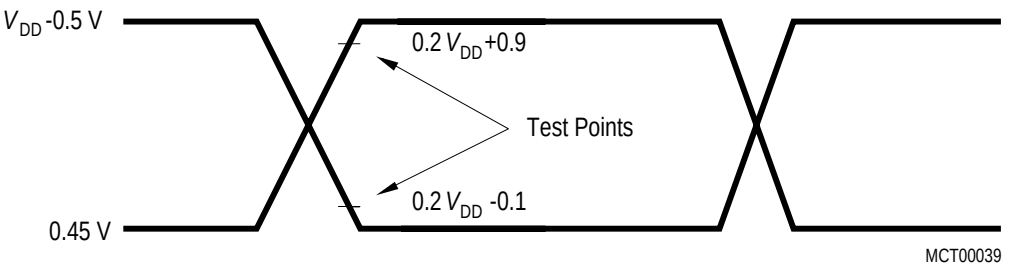


Address: P1.0 - P1.7 = A0 - A7
P2.0 - P2.6 = A8 - A14
Data: P0.0 - P0.7 = D0 - D7

Inputs: P2.7, $\overline{PSEN}$ = V_{SS}
ALE, $\overline{EA}$ = V_{IH}
RESET = V_{IH2}

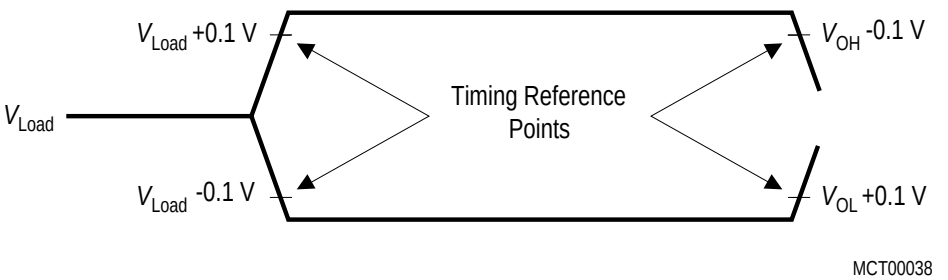
Note: P2.6 should be connected to V_{SS} for C505(C)(A)-2R

Figure 40
ROM Verification Mode 1



AC Inputs during testing are driven at V_{DD} - 0.5 V for a logic '1' and 0.45 V for a logic '0'. Timing measurements are made at V_{IHmin} for a logic '1' and V_{ILmax} for a logic '0'.

Figure 42
AC Testing: Input, Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm$ 20 mA

Figure 43
AC Testing : Float Waveforms

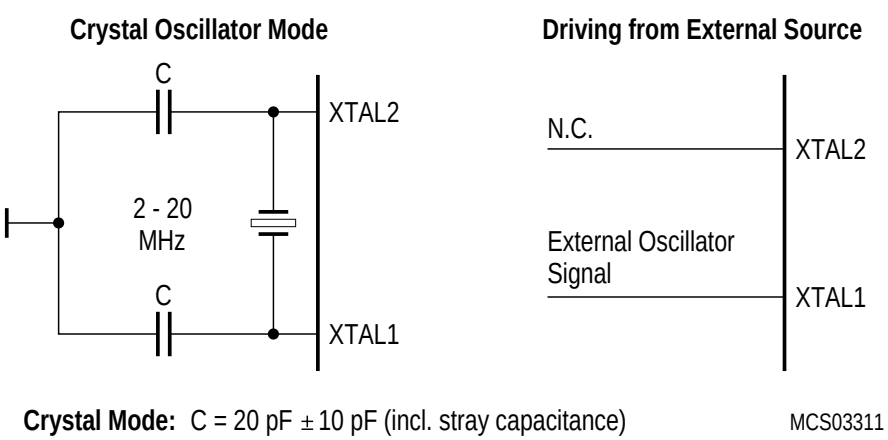


Figure 44
Recommended Oscillator Circuits for Crystal Oscillator