Details

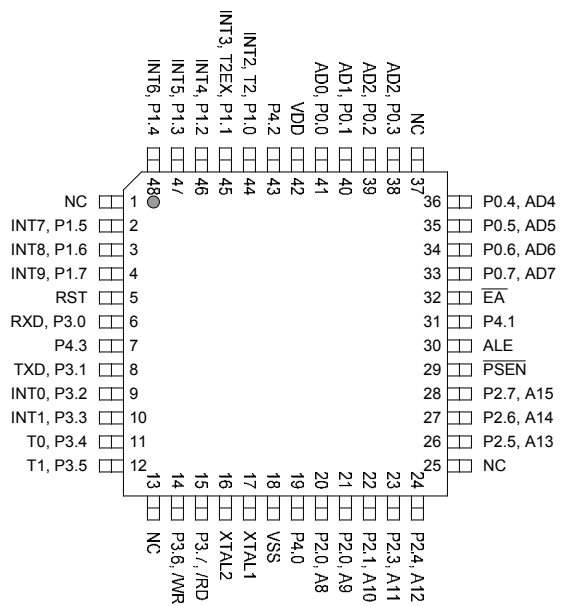|	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI
Peripherals	LED, WDT
Number of I/O	36
Program Memory Size	4KB (4K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l801a24fl

1. GENERAL DESCRIPTION

The W78L801 is an 8-bit microcontroller which can accommodate a wide range of supply voltages with low power consumption. The instruction set for the W78L801 is fully compatible with the standard 8051. The W78L801 contains an 4K bytes Mask ROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 6-bit I/O port P4; two 16-bit timer/counters; a hardware watchdog timer. These peripherals are supported by a twelve sources two-level interrupt capability. The W78L801 does not contain serial port.

The W78L801 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 1.8V to 5.5V
- DC-24 MHz operation
- 256 bytes of on-chip scratchpad RAM
- 4 KB Mask-ROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports; Port 0 has internal pull-up resisters enabled by software
- Two 16-bit timer/counters
- Watchdog Timer
- Direct LED drive outputs
- Twelve sources, two-level interrupt capability
- Wake-up via external interrupts at Port 1
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
  - DIP 40:   W78L801-24
  - PLCC 44:   W78L801P-24
  - PQFP 44:   W78L801F-24
  - Lead Free (RoHs)DIP 40:   W78L801A24DL
  - Lead Free (RoHs)PLCC 44: W78L801A24PL
  - Lead Free (RoHs)PQFP 44: W78L801A24FL
  - Lead Free (RoHs)LQFP 48: W78L801A24LL

W78L801

48-Pin LQFP

Pin labels (top, left to right pins 48–37):
INT6, P1.4 (48) / 47 / INT5, P1.3 (46) / INT4, P1.2 (45) / INT3, T2EX, P1.1 (44) / INT2, T2, P1.0 (43) / P4.2 (42) / VDD (41) / AD0, P0.0 (40) / AD1, P0.1 (39) / AD2, P0.2 (38) / AD2, P0.3 (37) / NC

Left side:
- NC — 1
- INT7, P1.5 — 2
- INT8, P1.6 — 3
- INT9, P1.7 — 4
- RST — 5
- RXD, P3.0 — 6
- P4.3 — 7
- TXD, P3.1 — 8
- INT0, P3.2 — 9
- INT1, P3.3 — 10
- T0, P3.4 — 11
- T1, P3.5 — 12

Right side:
- 36 — P0.4, AD4
- 35 — P0.5, AD5
- 34 — P0.6, AD6
- 33 — P0.7, AD7
- 32 — $\overline{EA}$
- 31 — P4.1
- 30 — ALE
- 29 — $\overline{PSEN}$
- 28 — P2.7, A15
- 27 — P2.6, A14
- 26 — P2.5, A13
- 25 — NC

Bottom (pins 13–24):
13 NC / 14 P3.6, /WR / 15 P3.7, /RD / 16 XTAL2 / 17 XTAL1 / 18 VSS / 19 P4.0 / 20 P2.0, A8 / 21 P2.0, A9 / 22 P2.1, A10 / 23 P2.3, A11 / 24 P2.4, A12

5. BLOCK DIAGRAM

6. FUNCTIONAL DESCRIPTION

The W78L801 architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, two timer/counters. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

Timers 0, 1

Timers 0, 1 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1. The TCON and TMOD registers provide control functions for timers 0 and 1. The operations of Timer 0 and Timer 1 are the same as in the W78C51.

I/O Port Options

The Port 0 and Port 3 of W78L801 may be configured with different types by setting the bits of the Port Options Register POR that is located at 86H. The pins of Port 0 can be configured with either the open drain or standard port with internal pull-up. By the default, Port 0 is an open drain bi-directional I/O port. When the PUP bit in the POR register is set, the pins of Port 0 will perform a quasi-bi-directional I/O port with internal pull-up that is structurally the same as Port 2. The high nibble of Port 3 (P3.4 to P3.7) can be selected to serve the direct LED displays drive outputs by setting the HDx bit in the PO register. When the HDx bit is set, the corresponding pin P3.x can sink about 20 mA current for driving LED display directly. After reset, the POR register is cleared and the pins of Ports 0 and 3 are the same as those of the standard 80C31. The POR register is shown below.

Port Options Register

Bit:	7	6	5	4	3	2	1	0
	EP6	EP5	-	HD7	HD6	HD5	HD4	P0UP

Mnemonic: POR   Address: 86H

P0UP : Enable Port 0 weak pull-up.

HD4-7: Enable pins P3.4 to P3.7 individually with High Drive outputs.

EP5   : Enable P4.5. To set this bit shifts ALE pin to the alternate function P4.5.

EP6   : Enable P4.6. To set this bit shifts $\overline{\text{PSEN}}$ pin to the alternate function P4.6

Port 4

The W78L801 has one additional bit-addressable I/O port P4 in which the port address is D8H. The Port 4 contains seven bits; P4.0 to P4.3 are only available on 44-pin PLCC/QFP package; P4.5 and P4.6 are the alternate function corresponding to pins ALE, $\overline{\text{PSEN}}$. When program is running in the internal memory without any access to external memory, ALE and PSEN may be individually configured to the alternate functions P4.5 and P4.6 that serve as general purpose I/O pins. To enable I/O port P4.5 and P4.6, the bits EP5 and EP6 in the POR register must be set. During reset, the ALE and $\overline{\text{PSEN}}$ perform as in the standard 80C32. The alternate functions P4.5 and P4.6 must be enabled by software. Care must be taken with the ALE pins when configured as the alternate functions. The ALE will emit pulses until either the EP5 bit in POR register or AO bit in AUXR register

is set to 1. i.e. User's applications should elude the ALE pulses before software configure it with I/O port P4.5.

Bit:	7	6	5	4	3	2	1	0
	-	P4.6	P4.5	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4   Address: D8H

6.1 Interrupt System

The W78L801 has twelve interrupt sources: $\overline{INT0}$ and $\overline{INT1}$; Timer 0,1; INT2 to INT9. Each interrupt vectors to a specific location in program memory for its interrupt service routine. Each of these sources can be individually enabled or disabled by setting or clearing the corresponding bit in Special Function Register IE0 and IE1. The individual interrupt priority level depends on the Interrupt Priority Register IP0 and IP1. Additional external interrupts INT2 to INT9 are level sensitive and may be used to awake the device from power down mode. The Port 1 interrupts can be initialized to either active HIGH or LOW via setting the Interrupt Polarity Register IX. The IRQ register contains the flags of Port 1 interrupts. Each flag in IRQ register will be set when an interrupt request is recognized but _must be cleared by software_. Note that the interrupt flags have to be cleared before the interrupt service routine is completed, or else another interrupt will be generated.

Interrupt Enable Register 0

Bit:	7	6	5	4	3	2	1	0
	EA	-	-	-	ET1	EX1	ET0	EX0

Mnemonic: IE   Address: A8H

EA : Global enable. Enable/disable all interrupts.
ET1: Enable Timer 1 interrupt
EX1: Enable external interrupt 1
ET0: Enable Timer 0 interrupt
EX0: Enable external interrupt 0

Interrupt Enable Register 1

Bit:	7	6	5	4	3	2	1	0
	EX9	EX8	EX7	EX6	EX5	EX4	EX3	EX2

Mnemonic: IE1   Address: E8H

EX9: Enable external interrupt 9
EX8: Enable external interrupt 8
EX7: Enable external interrupt 7
EX6: Enable external interrupt 6
EX5: Enable external interrupt 5
EX4: Enable external interrupt 4
EX3: Enable external interrupt 3
EX2: Enable external interrupt 2

Note: 0 = interrupt disabled, 1 = interrupt enabled.

Interrupt Priority Register 0

Bit:

7	6	5	4	3	2	1	0
-	PS1	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0   Address: B8h

IP.7: Unused.
PS1: This bit defines the Serial port 1 interrupt priority. PS = 1 sets it to higher priority level.
PT2: This bit defines the Timer 2 interrupt priority. PT2 = 1 sets it to higher priority level.
PS : This bit defines the Serial port 0 interrupt priority. PS = 1 sets it to higher priority level.
PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.
PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.
PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.
PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

Interrupt Priority Register 1

Bit:

7	6	5	4	3	2	1	0
PX9	PX8	PX7	PX6	PX5	PX4	PX3	PX2

Mnemonic: IP1   Address: F8h

PX9: This bit defines the External interrupt 9 priority. PX9 = 1 sets it to higher priority level.
PX8: This bit defines the External interrupt 8 priority. PX8 = 1 sets it to higher priority level.
PX7: This bit defines the External interrupt 7 priority. PX7 = 1 sets it to higher priority level.
PX6: This bit defines the External interrupt 6 priority. PX6 = 1 sets it to higher priority level.
PX5: This bit defines the External interrupt 5 priority. PX5 = 1 sets it to higher priority level.
PX4: This bit defines the External interrupt 4 priority. PX4 = 1 sets it to higher priority level.
PX3: This bit defines the External interrupt 3 priority. PX3 = 1 sets it to higher priority level.
PX2: This bit defines the External interrupt 2 priority. PX2 = 1 sets it to higher priority level.

Interrupt Polarity Register

Bit:

7	6	5	4	3	2	1	0
IL9	IL8	IL7	IL6	IL5	IL4	IL3	IL2

Mnemonic: IX   Address: E9H

IL9: External interrupt 9 polarity level.
IL8: External interrupt 8 polarity level.
IL7: External interrupt 7 polarity level.
IL6: External interrupt 6 polarity level.
IL5: External interrupt 5 polarity level.
IL4: External interrupt 4 polarity level.
IL3: External interrupt 3 polarity level.
IL2: External interrupt 2 polarity level.
Note: 0 = active LOW, 1 = active HIGH.

Interrupt Request Flag Register

Bit:	7	6	5	4	3	2	1	0
	IQ9	IQ8	IQ7	IQ6	IQ5	IQ4	IQ3	IQ2

Mnemonic: IRQ   Address: C0H

IQ9:   External interrupt 9 request flag.
IQ8:   External interrupt 8 request flag.
IQ7:   External interrupt 7 request flag.
IQ6:   External interrupt 6 request flag.
IQ5:   External interrupt 5 request flag.
IQ4:   External interrupt 4 request flag.
IQ3:   External interrupt 3 request flag.
IQ2:   External interrupt 2 request flag.

Table.1 Priority level for simultaneous requests of the same priority interrupt sources

SOURCE	FLAG	PRIORITY LEVEL	VECTOR ADDRESS
External Interrupt 0	IE0	(highest)	0003H
External Interrupt 5	IQ5		0053H
Timer 0 Overflow	TF0		000BH
External Interrupt 6	IQ6		005BH
External Interrupt 1	IE1		0013H
External Interrupt 2	IQ2		003BH
External Interrupt 7	IQ7		0063H
Timer 1 Overflow	TF1		001BH
External Interrupt 3	IQ3		0043H
External Interrupt 8	IQ8		006BH
External Interrupt 4	IQ4		004BH
External Interrupt 9	IQ9	(lowest)	0073H

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs, a system reset can be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will be disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC   Address: 8FH

ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2 − 0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 1 0	4
0 0 1	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

The time-out period is obtained using the following formula:

$$\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \ mS$$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.

Watchdog Timer Block Diagram
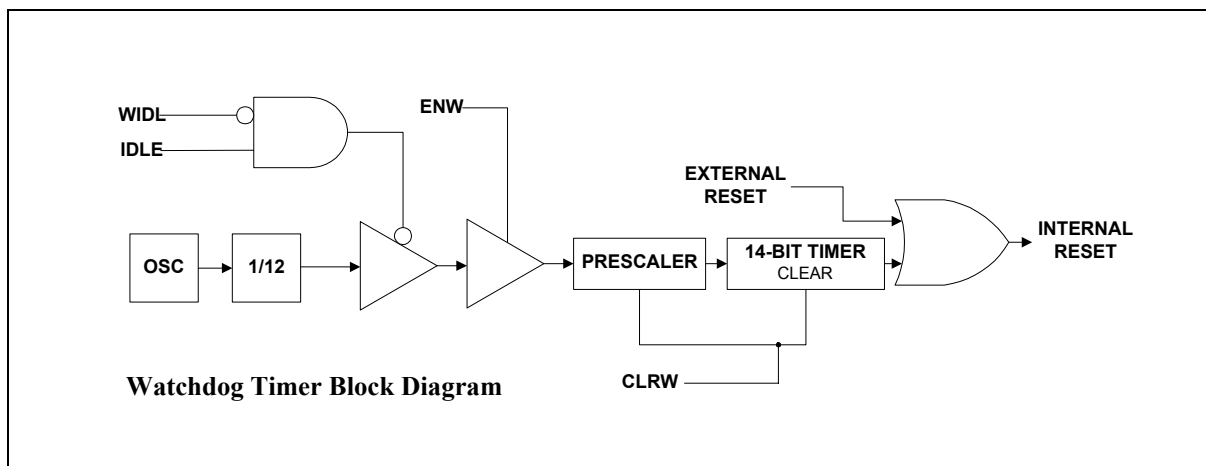
Typical Watch-Dog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 1 0	39.32 mS
0 0 1	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57 mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

Clock

The W78L801 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78L801 relatively insensitive to duty cycle variations in the clock. The W78L801 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground. An external clock source should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit in the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. To exit from power-down mode is by a hardware reset or external interrupts INT2 to INT9 when enabled.

AUXR – Auxiliary Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	AO

Mnemonic: AUXR   Address: 8Eh

AO: Turn off ALE signal.

Reduce EMI Emission

Because of the on-chip ROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is not needed. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running. An internal trigger circuit in the reset line is used to deglitch the reset line when the W78L801 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

7. ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+6.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 DC Characteristics

V_{SS} = 0V; T_A = 25° C; unless otherwise specified.

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	1.8	5.5	V	
Operating Current	I_{DD}	-	20	mA	V_{DD} = 5.5V, 24 MHz, no load, RST = 1
		-	3	mA	V_{DD} = 2.2V, 24 MHz, no load, RST = 1
Idle Current	I_{IDLE}	-	6	mA	V_{DD} = 5.5V, 24 MHz, no load
		-	1.5	mA	V_{DD} = 2.2V, 24 MHz, no load
Power Down Current	I_{PWDN}	-	50	μA	V_{DD} = 5.5V, no load
		-	30	μA	V_{DD} = 2.2V, no load
Input					
Input Current P1, P2, P3, P4	I_{IN}	-50	+10	μA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-60	+300	μA	V_{DD} = 5.5V 0 < V_{IN}< V_{DD}
Input Leakage Current P0, $\overline{EA}$	I_{LK1}	-10	+10	μA	V_{DD} = 5.5V 0V< V_{IN} < V_{DD}
Logic 1-to-0 Transition Current P1, P2, P3, P4	ITL	-500	-200	μA	VDD = 5.5V VIN = 2V
Input Low Voltage	VIL1	0	0.8	V	VDD = 5.5V
P1, P2, P3, P4, $\overline{EA}$		0	0.5	V	VDD = 2.2V

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input Low Voltage RST[*3]	V_{IL2}	0	0.8	V	V_{DD} = 5.5V
		0	0.3	V	V_{DD} = 2.2V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8		V_{DD} = 5.5V
		0	0.6	V	V_{DD} = 2.2V
Input High Voltage P1, P2, P3, P4	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.4	V_{DD} +0.2	V	V_{DD} = 2.2V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.7	V_{DD} +0.2	V	V_{DD} = 2.2V
Input High Voltage XTAL1[*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.6	V_{DD} +0.2	V	V_{DD} = 2.2V
Output					
Output Low Voltage P1, P2, P3, P4 <0:4>	V_{OL1}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +2 mA
		-	0.25	V	V_{DD} = 2.2V, I_{OL} = +1 mA
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*4]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V, I_{OL} = +4 mA
		-	0.25	V	V_{DD} = 2.2V, I_{OL} = +2 mA
Sink Current P1, P2, P3[5] , P4<0:4>	I_{SK1}	4	12	mA	V_{DD} = 4.5V, V_S = 0.45V
		1.8	5.4	mA	V_{DD} = 2.2V, Vin = 0.4V
Sink Current P0, ALE, $\overline{PSEN}$, P4<5:6>	I_{SK2}	10	20	mA	V_{DD} = 4.5V, V_S = 0.45V
		4.5	9	mA	V_{DD} = 2.2V, Vin = 0.4V
Sink Current P3.4 to P3.7 in High-drive Mode	I_{SK3}	15	24	mA	V_{DD} = 4.5V, V_S = 0.45V
		12	24	mA	V_{DD} = 4.5V, Vin = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V, I_{OH} = 100 μA
		1.4	-	V	V_{DD} = 2.2V, I_{OH} = -8 μA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*4]		2.4	-	V	VDD = 4.5V, IOH = 100 μA
		1.4	-	V	VDD = 2.2V, IOH = -400 μA

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Source Current P1, P2, P3, P4<0:4>	Isr1	-120	-250	μA	V_{DD} = 4.5V, Vs = 2.4V
		-12	-33	μA	V_{DD} = 2.2V, Vin = 1.4V
Source Current P0, ALE, $\overline{PSEN}$, P4<5:6>	Isr2	-8	-14	mA	V_{DD} = 4.5V, Vs = 2.4V
		-1.1	-2.4	mA	V_{DD} = 2.2V, Vin = 1.4V

Notes:

*1. RST pin has an internal pull-down.

*2. Pins of P1 and P3 can source a transition current when they are being externally driven from 1 to 0.

*3. RST is a Schmitt trigger input and XTAL1 is a CMOS input.

*4. P0, P2, ALE and /PSEN are tested in the external access mode.

*5. P3.4 to P3.7 are in normal mode.

7.3 AC Characteristics

Clock Input Waveform
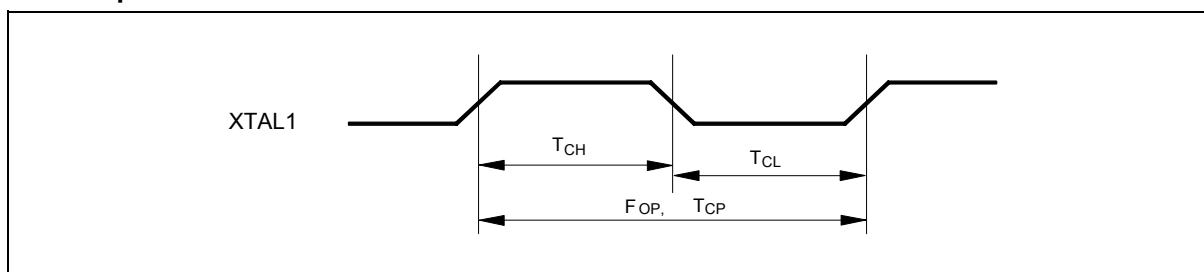
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	24	MHz	1
Clock Period	T_{CP}	41.6	-	-	nS	2
Clock High	T_{CH}	20	-	-	nS	3
Clock Low	T_{CL}	20	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.

2. The T_{CP} specification is used as a reference in other specifications.

3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	T_{AAS}	1 T_{CP} -Δ	-	-	nS	4
Address Hold from ALE Low	T_{AAH}	1 T_{CP} -Δ	-	-	nS	1, 4
ALE Low to $\overline{PSEN}$ Low	T_{APL}	1 T_{CP} -Δ	-	-	nS	4
$\overline{PSEN}$ Low to Data Valid	T_{PDA}	-	-	2 T_{CP}	nS	2
Data Hold after $\overline{PSEN}$ High	T_{PDH}	0	-	1 T_{CP}	nS	3
Data Float after $\overline{PSEN}$ High	T_{PDZ}	0	-	1 T_{CP}	nS	
ALE Pulse Width	T_{ALW}	2 T_{CP} -Δ	2 T_{CP}	-	nS	4
$\overline{PSEN}$ Pulse Width	T_{PSW}	3 T_{CP} -Δ	3 T_{CP}	-	nS	4

Notes:

1. P0.0 − P0.7, P2.0 − P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 T_{CP}.
3. Data have been latched internally prior to $\overline{PSEN}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{RD}$ Low	T_{DAR}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS	1, 2
$\overline{RD}$ Low to Data Valid	T_{DDA}	-	-	4 T_{CP}	nS	1
Data Hold from $\overline{RD}$ High	T_{DDH}	0	-	2 T_{CP}	nS	
Data Float from $\overline{RD}$ High	T_{DDZ}	0	-	2 T_{CP}	nS	
$\overline{RD}$ Pulse Width	T_{DRD}	6 T_{CP} -Δ	6 T_{CP}	-	nS	2

Notes:

1. Data memory access time is 8 T_{CP}.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	T_{DAW}	3 T_{CP} -Δ	-	3 T_{CP} +Δ	nS
Data Valid to $\overline{WR}$ Low	T_{DAD}	1 T_{CP} -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	T_{DWD}	1 T_{CP} -Δ	-	-	nS
$\overline{WR}$ Pulse Width	T_{DWR}	6 T_{CP} -Δ	6 T_{CP}	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Port Access Cycle

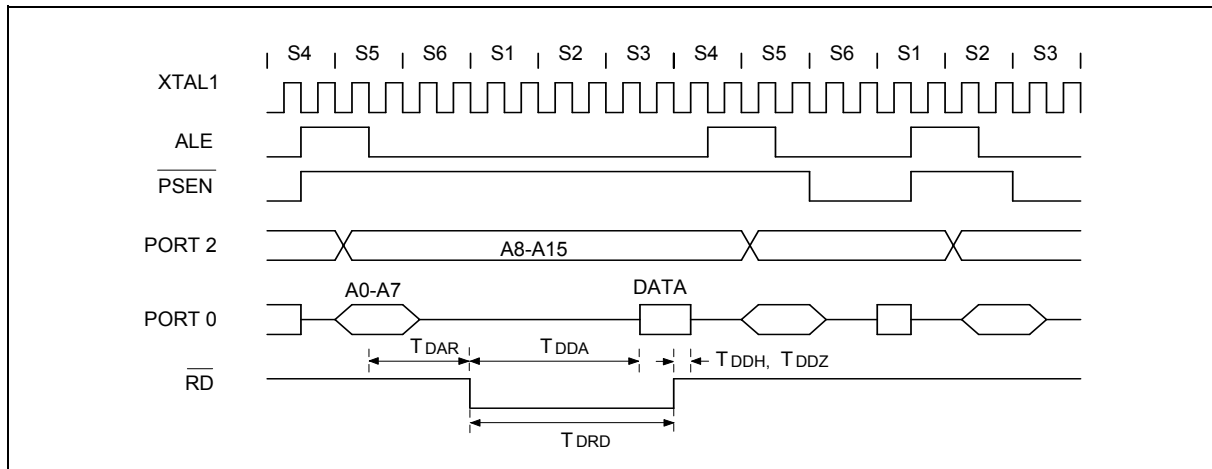| PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	T_{PDS}	1 T_{CP}	-	-	nS
Port Input Hold from ALE Low	T_{PDH}	0	-	-	nS
Port Output to ALE	T_{PDA}	1 T_{CP}	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

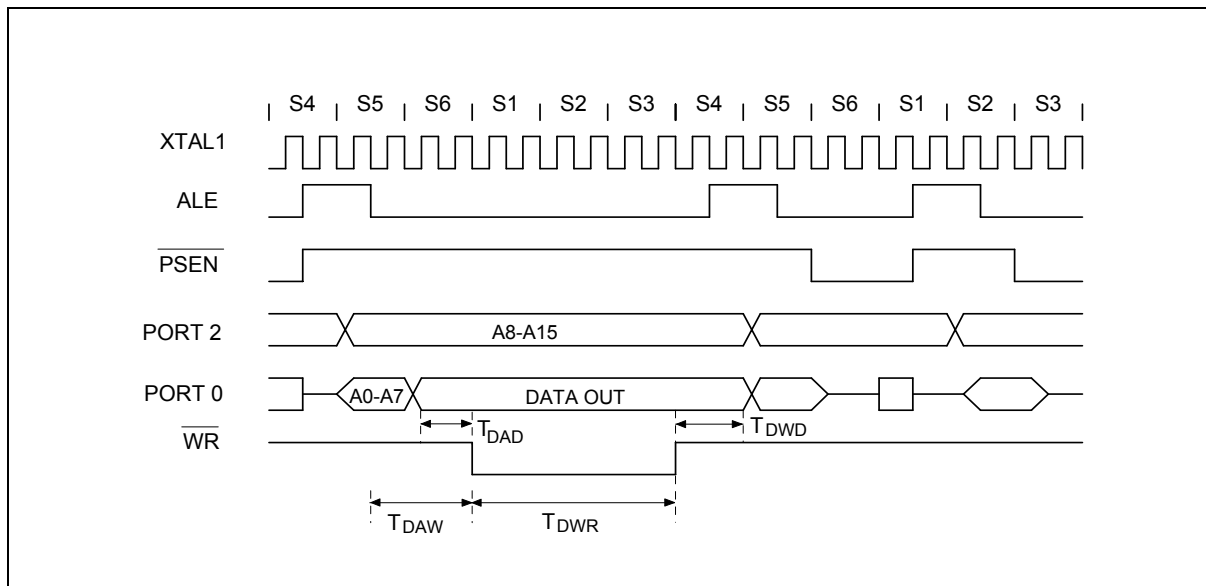## 8. TIMING WAVEFORMS

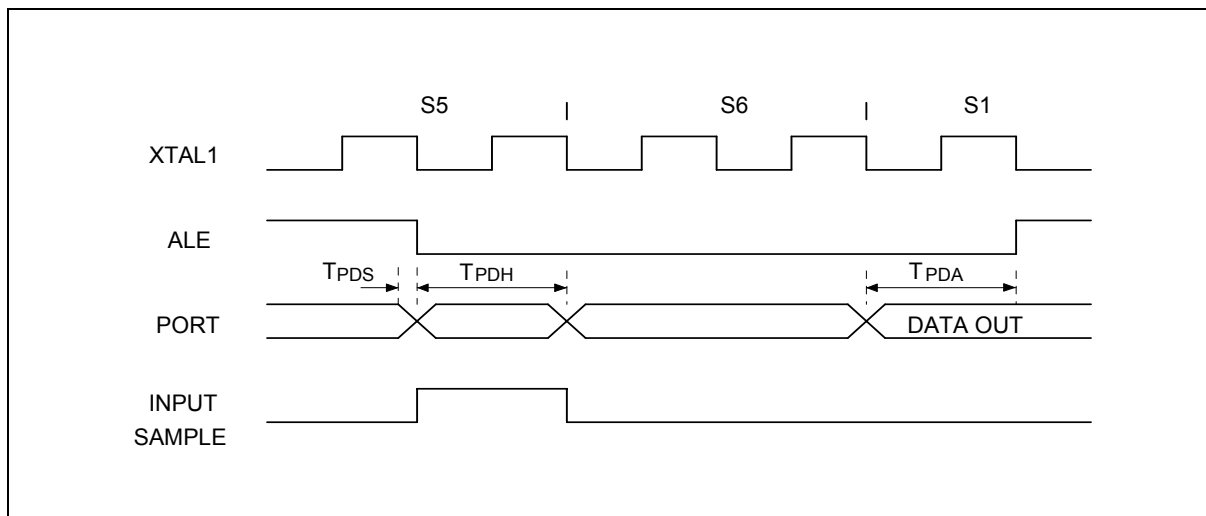### 8.1 Program Fetch Cycle
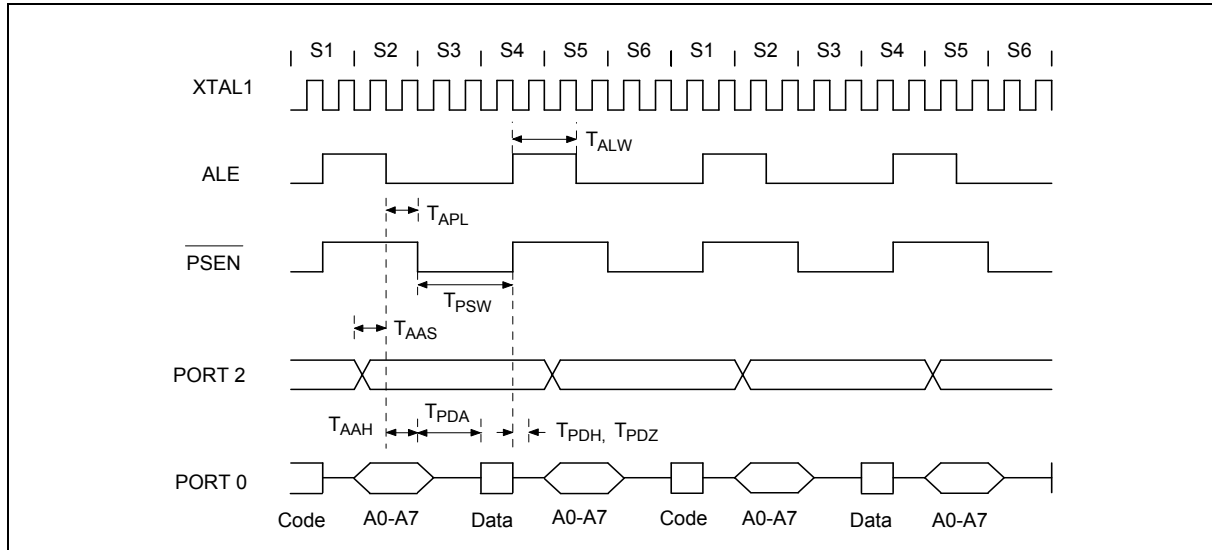
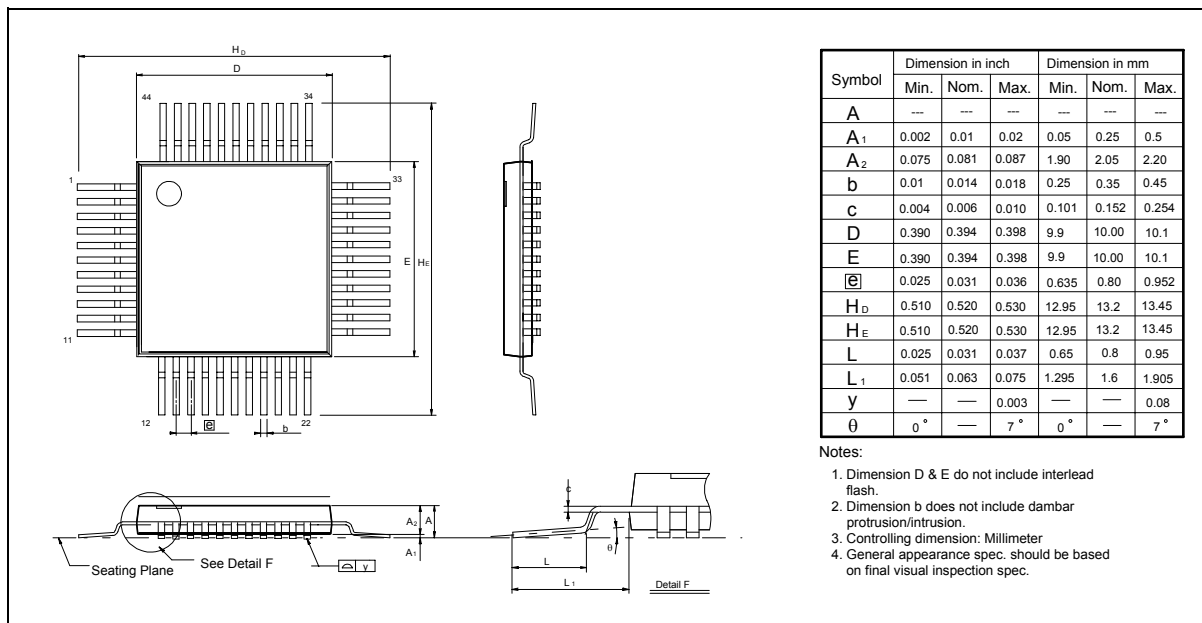### 8.2 Data Read Cycle

Timing Waveforms, continued
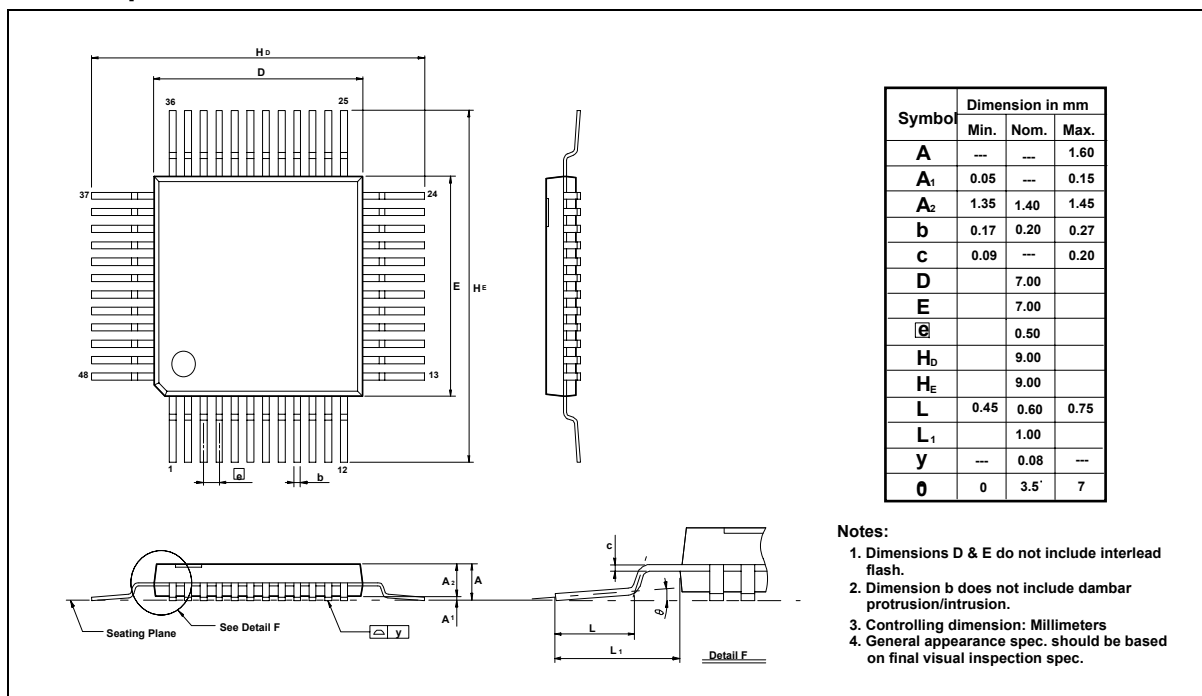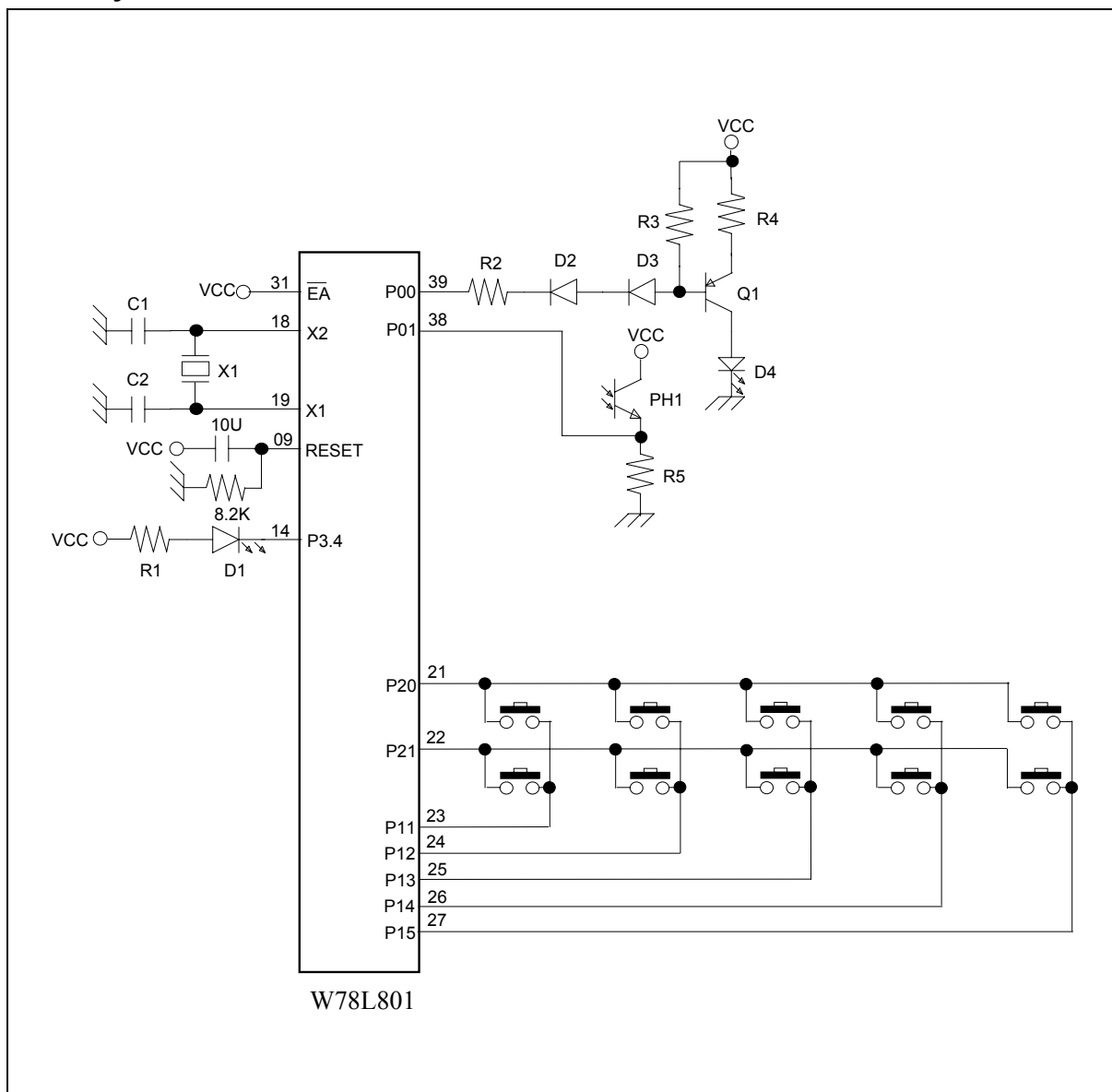
8.3　Data Write Cycle

8.4　Port Access Cycle

Winbond
Electronics Corp.

9.3 44-pin PQFP

Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A$_1$	0.002	0.01	0.02	0.05	0.25	0.5
A$_2$	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H$_D$	0.510	0.520	0.530	12.95	13.2	13.45
H$_E$	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L$_1$	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

9.4 48-pin LQFP

Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	---	---	1.60
A$_1$	0.05	---	0.15
A$_2$	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	---	0.20
D		7.00	
E		7.00	
e		0.50	
H$_D$		9.00	
H$_E$		9.00	
L	0.45	0.60	0.75
L$_1$		1.00	
y	---	0.08	---
θ	0	3.5°	7

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

10. TYPICAL APPLICATION CIRCUIT

10.1 Keyboard

11. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A5	July 8, 2002	-	Initial Issued
A6	Dec. 30, 2004	1	Add Lead Free Package
A7	April 19, 2005	21	Add Important Notice
A8	Aug. 25, 2005	2, 4	Add Port 0 pull-up resisters information
A9	Oct. 3, 2005	2	Modify Lead Free Part No.
A10	June 04, 2006	2,4	Add a part in 48-pin LQFP package
		22	Add package spec of 48-pin LQFP

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