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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	RL78
Core Size	16-Bit
Speed	20MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 4x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	10-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	10-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10y14asp-x0

○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	R5F10Y17	R5F10Y47
2 KB	256 B	R5F10Y16	R5F10Y46
1 KB	128 B	R5F10Y14	R5F10Y44

Note 16-pin products only

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G10

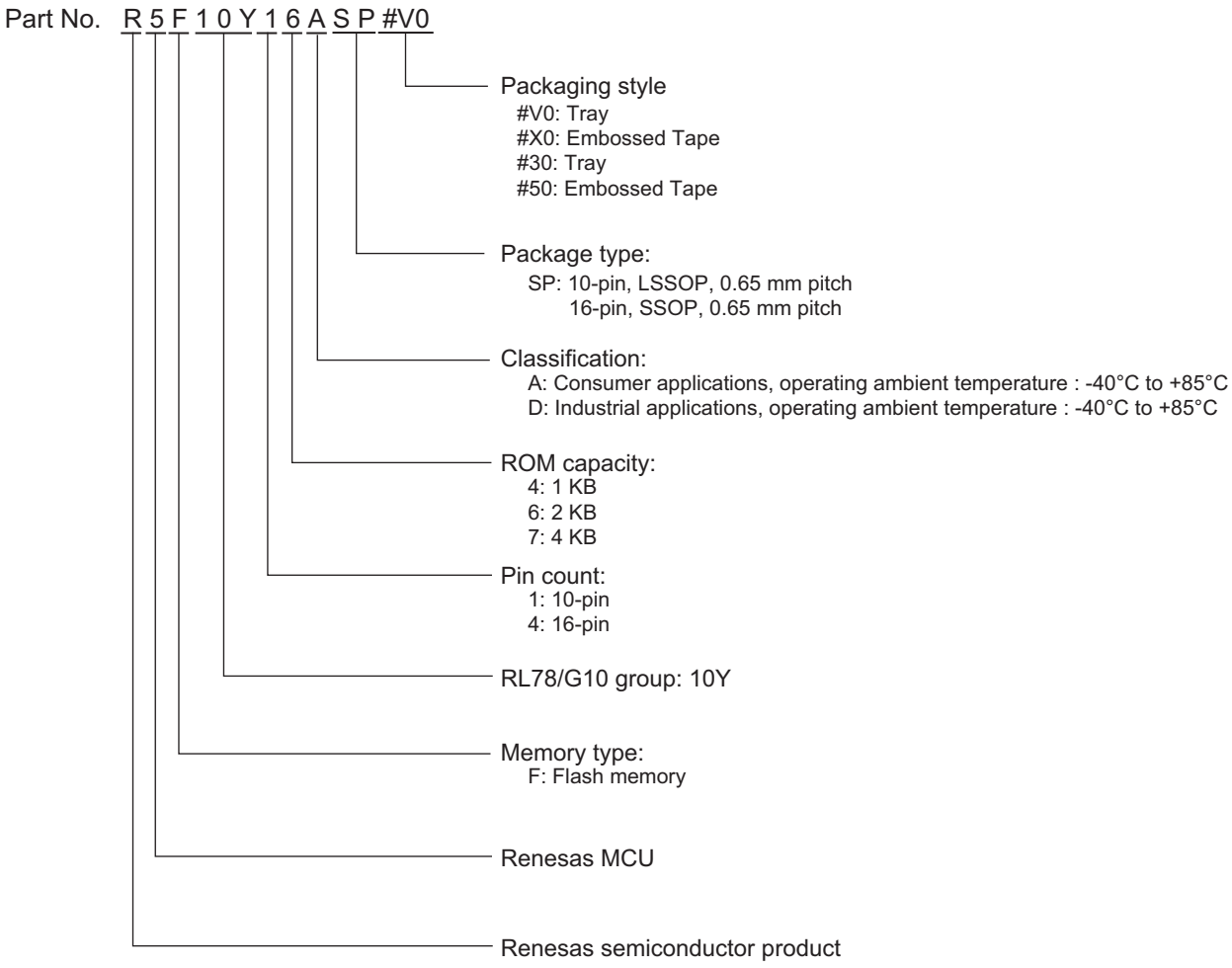


Table 1-1. List of Ordering Part Numbers

Pin count	Package	Fields of Application Note	Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65 mm pitch)	A	R5F10Y17ASP#30, R5F10Y17ASP#50 R5F10Y16ASP#V0, R5F10Y16ASP#X0 R5F10Y14ASP#V0, R5F10Y14ASP#X0
<R>		D	R5F10Y17DSP#30, R5F10Y17DSP#50 R5F10Y16DSP#30, R5F10Y16DSP#50 R5F10Y14DSP#30, R5F10Y14DSP#50
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65 mm pitch)	A	R5F10Y47ASP#30, R5F10Y47ASP#50 R5F10Y46ASP#30, R5F10Y46ASP#50 R5F10Y44ASP#30, R5F10Y44ASP#50
<R>		D	R5F10Y47DSP#30, R5F10Y47DSP#50 R5F10Y46DSP#30, R5F10Y46DSP#50 R5F10Y44DSP#30, R5F10Y44DSP#50

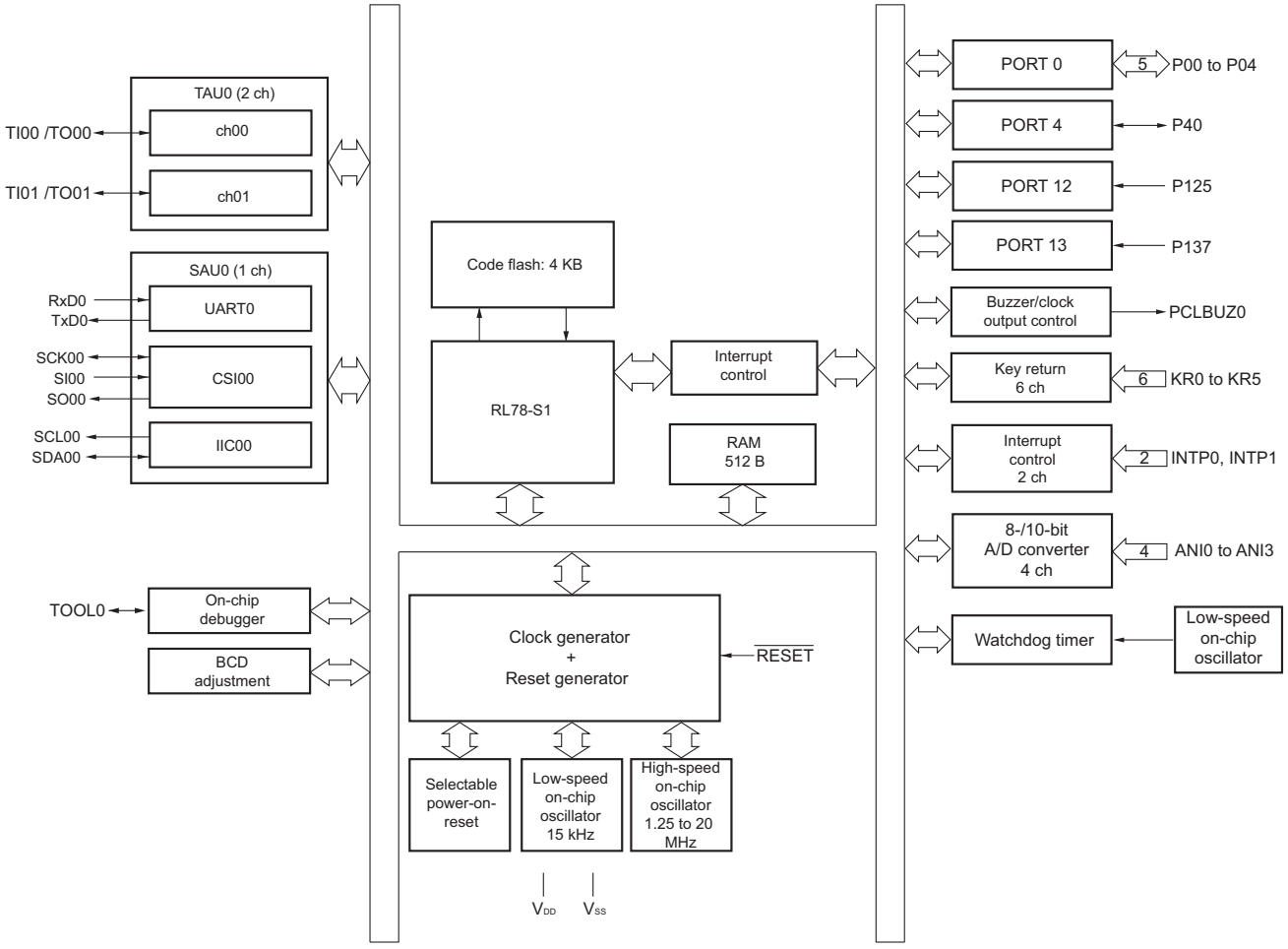
(**Notes** and **Caution** are listed on the next page.)

1.4 Pin Identification

ANI0 to ANI6	: Analog Input
INTP0 to INTP3	: Interrupt Request From Peripheral
KR0 to KR5	: Key Return
P00 to P07	: Port 0
P40, P41	: Port 4
P121, P122, P125	: Port 12
P137	: Port 13
PCLBUZ0	: Programmable Clock Output/ Buzzer Output
EXCLK	: External Clock Input
X1, X2	: Crystal Oscillator (Main System Clock)
IVCMP0	: Comparator Input
VCOUT0	: Comparator Output
IVREF0	: Comparator Reference Input
$\overline{\text{RESET}}$	: Reset
RxD0	: Receive Data
SCK00, SCK01	: Serial Clock Input/Output
SCL00, SCLA0	: Serial Clock Output
SDA00, SDAA0	: Serial Data Input/Output
SI00, SI01	: Serial Data Input
SO00, SO01	: Serial Data Output
TI00 to TI03	: Timer Input
TO00 to TO03	: Timer Output
TOOL0	: Data Input/Output for Tool
TxD0	: Transmit Data
V_{DD}	: Power Supply
V_{SS}	: Ground

1.5 Block Diagram

1.5.1 10-pin products



2.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to +6.5	V
Input Voltage	V_{I1}			−0.3 to V_{DD} + 0.3 Note	V
Output Voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins	P40, P41	−70	mA
			P00 to P07	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins	P40, P41	70	mA
			P00 to P07	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS}.

2.2 Oscillator Characteristics

2.2.1 X1 oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1		20	MHz
		2.0 V ≤ V_{DD} < 2.7 V	1		5	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G10 User's Manual.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency Notes 1, 2	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		T_A = -20 to +85°C	-2.0		+2.0	%
		T_A = -40 to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(1/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				-10.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-4.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-3.0	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-60.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			-9.0	mA
		Total of all pins (When duty ≤ 70% Note 3)				-80.0	mA
Output current, low Note 4	I_{OL1}	Per pin for 10-pin products: P00 to P04, P40 16-pin products: P00 to P07, P40, P41				20.0 Note 2	mA
		Total of 10-pin products: P40 16-pin products: P40, P41 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			6.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			1.2	mA
		Total of 10-pin products: P00 to P04 16-pin products: P00 to P07 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
			2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins (When duty ≤ 70% Note 3)				120.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. This is the output current value under conditions where the duty factor ≤ 70%.
The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OH} = - 10.0 mA
  Total output current of pins = (- 10.0 × 0.7)/(80 × 0.01) ≅ - 8.7 mA
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

Caution P00, P01, P06, and P07 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

(1) Flash ROM: 1 and 2 KB of 10-pin products

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		350	820	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		290	600	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.56	2.00	µA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the watchdog timer.

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

(2) Flash ROM: 4 KB of 10-pin products, and 16-pin products

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		0.92		mA
			Normal operation	f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		1.59	2.14	
				f_{IH} = 5 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		0.87	1.20	
				f_{MX} = 20 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		1.43	1.93	
					Resonator connection		1.54	2.13	
				f_{MX} = 5 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		0.67	1.02	
					Resonator connection		0.72	1.12	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		360	900	μA
				f_{IH} = 5 MHz Note 4	V_{DD} = 3.0 V, 5.0 V		310	660	
				f_{MX} = 20 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		200	700	
					Resonator connection		300	900	
				f_{MX} = 5 MHz Notes 5, 6 V_{DD} = 3.0 V, 5.0 V	Square wave input		100	440	
					Resonator connection		150	540	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.61	2.25	μA

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator (16-pin products only), I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. Not including the current flowing into the 12-bit interval timer and watchdog timer.

4. When the high-speed system clock is stopped.

5. When the high-speed on-chip oscillator is stopped.

6. 16-pin products only

Remarks 1. f_{IH}: High-speed on-chip oscillator clock frequency

2. f_{MX}: High-speed system clock frequency (X1 clock oscillator frequency or external main system clock frequency)

3. Temperature condition of the typical value is T_A = 25°C

(3) Peripheral Functions (Common to all products)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.30		μA
12-bit interval timer operating current	I_{TMKA} Notes 1, 2, 3				0.01		μA
Watchdog timer operating current	I_{WDT} Notes 1, 4				0.01		μA
A/D converter operating current	I_{ADC} Notes 1, 5	When conversion at maximum speed	V_{DD} = 5.0 V		1.30	1.90	mA
			V_{DD} = 3.0 V		0.50		mA
Comparator operating current	I_{CMP} Notes 1, 6	In high-speed mode	V_{DD} = 5.0 V		6.50		μA
		In low-speed mode	V_{DD} = 5.0 V		1.70		μA
Internal reference voltage operating current	I_{VREG} Note 1				10		μA

Notes 1. Current flowing to V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{TMKA}, when the 12-bit interval timer is in operation.

4. Current flowing only to the watchdog timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{FIL} and I_{WDT} when the watchdog timer is in operation.

5. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

6. Current flowing only to the comparator. The supply current of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{CMP} when the comparator is in operation.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. Temperature condition of the typical value is T_A = 25°C

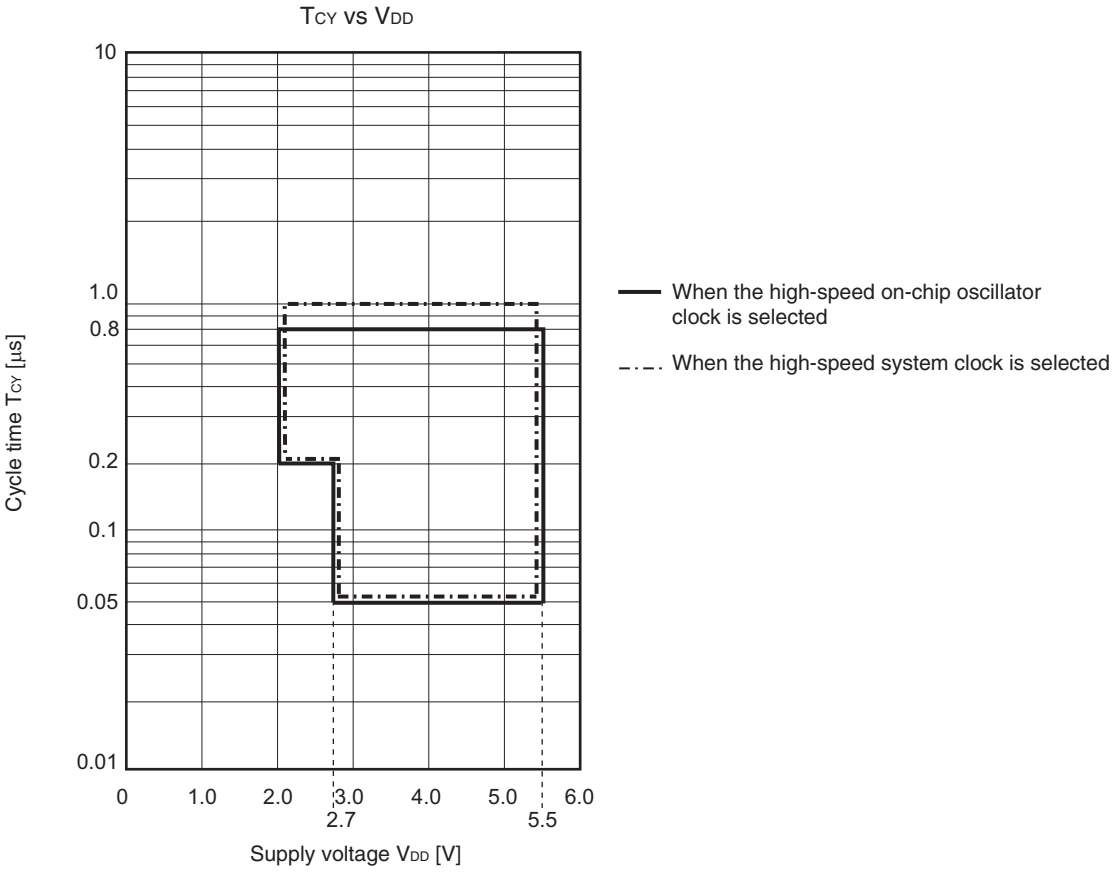
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

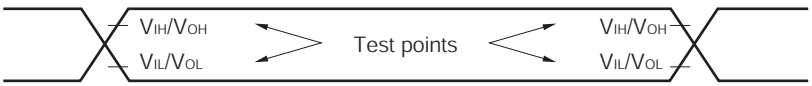
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	When high-speed on-chip oscillator clock (f_{IH}) is selected	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.2		0.8	μs
		When high-speed system clock (f_{MX}) is selected	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		1.0	μs
			2.0 V ≤ V_{DD} < 2.7 V	0.2		1.0	μs
External system clock frequency	T_{EX}		2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20	MHz
			2.0 V ≤ V_{DD} < 2.7 V	1.0		5	MHz
External system clock input high-level width, low-level width	T_{EXH}, T_{EXL}		2.7 V ≤ V_{DD} ≤ 5.5 V	24			ns
			2.0 V ≤ V_{DD} < 2.7 V	95			ns
TI00 to TI03 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK} + 10			ns
TO00 to TO03 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the timer clock select register 0 (TPS0) and the CKS0n1 bit of timer mode register 0nH (TMR0nH). n: Channel number (n = 0 to 3))

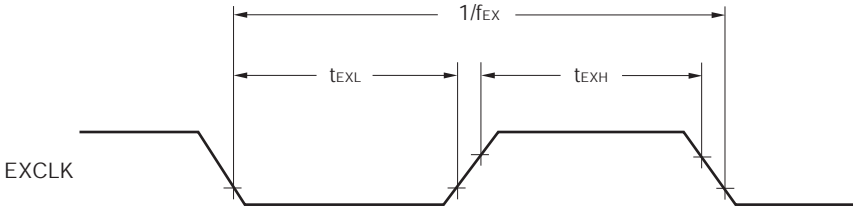
Minimum Instruction Execution Time during Main System Clock Operation



AC Timing Test Points

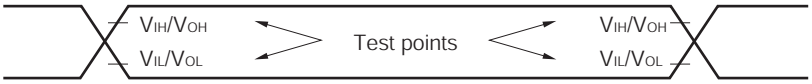


External System Clock Timing



2.5 Serial Interface Characteristics

AC Timing Test Points



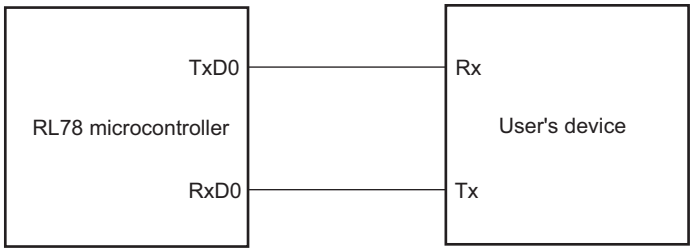
2.5.1 Serial array unit

(1) UART mode

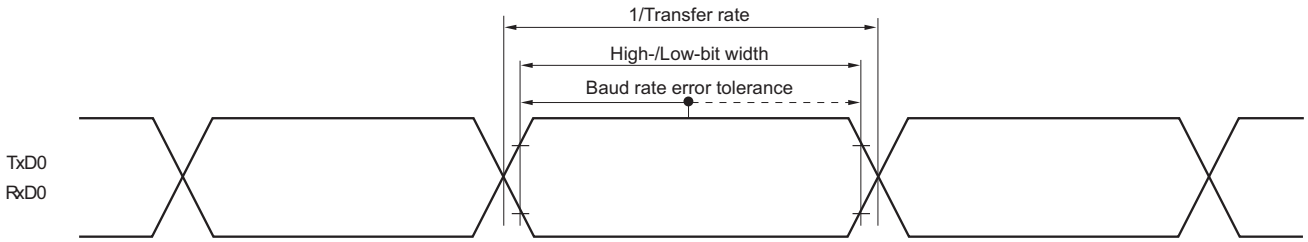
(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

(2) CSI mode (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 - 50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO1}	C = 30 pF Note 3				25	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SCKp and SOp output lines.

(3) CSI mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} > 16 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2 - 18			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 2	t_{KSO2}	C = 30 pF Note 3	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 110	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to SCKp↓" and the SIp hold time becomes "from SCKp↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from SCKp↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. C is the load capacitance of the SOp output lines.

Remarks 1. p: CSI number (p = 00, 01), n: Channel number (n = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the serial clock select register 0 (SPS0) and the CKS0n bit of the serial mode register 0nH (SMR0nH). n: Channel number (n = 0, 1))

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target pin: ANI0 to ANI6, internal reference voltage)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2, 3	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1	LSB
			V_{DD} = 3 V		±2.3	±4.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI6	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V Note 5	4.6		18.4	μs
		10-bit resolution Target pin: internal reference voltage Note 6	2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	μs
Zero-scale error Notes 1, 2, 3, 4	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19	%FSR
			V_{DD} = 3 V			±0.39	%FSR
Full-scale error Notes 1, 2, 3, 4	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29	%FSR
			V_{DD} = 3 V			±0.42	%FSR
Integral linearity error Notes 1, 2, 3	ILE	10-bit resolution	V_{DD} = 5 V			±1.8	LSB
			V_{DD} = 3 V			±1.7	LSB
Differential linearity error Notes 1, 2, 3	DLE	10-bit resolution	V_{DD} = 5 V			±1.4	LSB
			V_{DD} = 3 V			±1.5	LSB
Analog input voltage	V_{AIN}	Target pin: ANI0 to ANI6		0		V_{DD}	V
		Target pin: internal reference voltage Note 6		V_{REG} Note 7			V

Notes 1. TYP. Value is the average value at T_A = 25°C. MAX. value is the average value ±3σ at normal distribution.

2. These values are the results of characteristic evaluation and are not checked for shipment.

3. Excludes quantization error (±1/2 LSB).

4. This value is indicated as a ratio (%FSR) to the full-scale value.

5. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when conversion is done in the operating voltage range of 2.4 V ≤ V_{DD} < 2.7 V.

6. Set the LV0 bit in the A/D converter mode register 0 (ADM0) to 0 when the internal reference voltage is selected as the target for conversion.

7. Refer to **2.6.3 Internal reference voltage characteristics**.

Cautions 1. Arrange wiring and insert the capacitor so that no noise appears on the power supply/ground line.

2. Do not allow any pulses that rapidly change such as digital signals to be input/output to/from the pins adjacent to the conversion pin during A/D conversion.

3. Note that the internal reference voltage cannot be used as the reference voltage of the comparator when the internal reference voltage is selected as the target for A/D conversion.

2.6.2 Comparator characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage range	I_{VREF}	IVREF0 pin input (when C0VFR bit = 0)		0		V_{DD} - 1.4	V
		Internal reference voltage (when C0VRF bit = 1) Note 1		V_{REG} Note 2			V
	I_{VCMP}	IVCMP0 pin input		-0.3		V_{DD} + 0.3	V
Output delay	t_d	V_{DD} = 3.0 V, input slew rate > 50 mV/µs	High-speed mode			0.5	µs
			Low-speed mode		2.0		µs
Operation stabilization wait time	t_{CMP}			100			µs

Notes 1. When the internal reference voltage is selected as the reference voltage of the comparator, the internal reference voltage cannot be used as the target for A/D conversion.

2. Refer to **2.6.3 Internal reference voltage characteristics**.

2.6.3 Internal reference voltage characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal reference voltage	V_{REG}		0.74	0.815	0.89	V
Operation stabilization wait time	t_{AMP}	When A/D converter is used (ADS register = 07H)	5			µs

Note The internal reference voltage cannot be simultaneously used by the A/D converter and the comparator; only one of them must be selected.

2.6.4 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Power supply voltage level	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
			Power supply fall time	4.00	4.20	4.37	V
		V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
			Power supply fall time	2.70	2.84	2.96	V
		V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
			Power supply fall time	2.40	2.52	2.62	V
		V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
			Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width Note		T_{LSPW}		300			μs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPOR}.

Caution Set the detection voltage (V_{SPOR}) in the operating voltage range. The operating voltage range depends on the setting of the user option byte (000C2H). The operating voltage range is as follows:
When the CPU operating frequency is from 1 MHz to 20 MHz: V_{DD} = 2.7 to 5.5 V
When the CPU operating frequency is from 1 MHz to 5 MHz: V_{DD} = 2.0 to 5.5 V

2.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

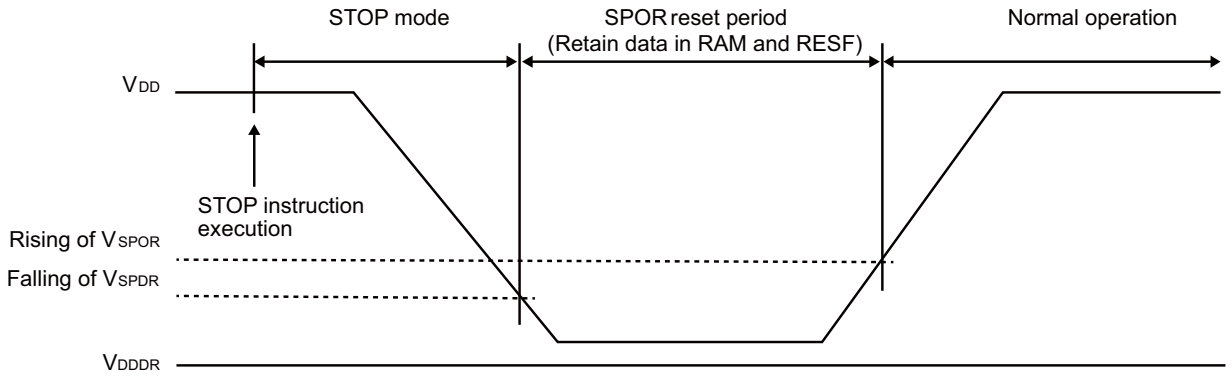
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.7 RAM Data Retention Characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.9		5.5	V

Caution Data in RAM is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}). Note that data in the RESF register might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage (V_{DDDR}).



2.8 Flash Memory Programming Characteristics

(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years.	T_A = +85°C	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

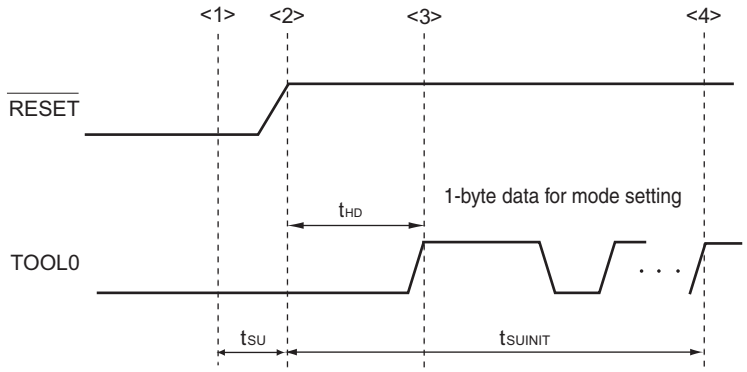
(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

2.10 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	SPOR reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	SPOR reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released	t_{HD}	SPOR reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (SPOR reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of entry to the flash memory programming mode by UART reception is completed.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released

Revision History	RL78/G10 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued
2.00	Jan 10, 2014	1, 2	Modification of descriptions in 1.1 Features
		3	Modification of description in 1.2 List of Part Numbers
		4	Modification of remark 2 in 1.3.1 10-pin products and 1.3.2 16-pin products
		8, 9	Addition of description of R5F10Y17ASP in 1.6 Outline of Functions
		11	Modification of description in 2.1 Absolute Maximum Ratings
		12	Modification of description in 2.2 Oscillator Characteristics
		13, 14	Modification of description, notes 1 to 4, and caution in 2.3.1 Pin characteristics
		16	Addition of description, notes 1 to 6, and remarks 1 and 2 in (2) Flash ROM: 4 KB of 10-pin products, and 16-pin products
		17	Addition of description, notes 1 to 6, and remarks 1 to 3 in (3) Peripheral Functions (Common to all products)
		18	Modification of description in 2.4 AC Characteristics
		19	Addition of figure of Minimum Instruction Execution Time during Main System Clock Operation
		19	Addition of figure of External System Clock Timing
		20	Modification of TI/TO Timing
		25	Addition of description in 2.5.2 Serial interface IICA
		26	Modification of description and notes 1 to 6 in 2.6.1 A/D converter characteristics
		27	Addition of description, notes 1 and 2 in 2.6.2 Comparator characteristics
		27	Addition of description and note in 2.6.3 Internal reference voltage characteristics
		28	Addition of caution in 2.6.4 SPOR Circuit characteristics
		28	Addition of figure in 2.6.6 Data retention power supply voltage characteristics
		31	Addition of R5F10Y17ASP in 3.1 10-pin products
		32	Modification of package drawing in 3.2 16-pin products
3.00	Nov 19, 2014	3	Addition of industrial applications in Figure 1-1 Part Number, Memory Size, and Package of RL78/G10
		3	Addition of industrial applications in Table 1-1 List of Ordering Part Numbers
		4	Addition of description to pin configuration in 1.3.1 10-pin products and 1.3.2 16-pin products
		22	Correction of error in 2.5.1 Serial array unit, (3) CSI mode (slave mode, SCKp... external clock input)
		28	Renamed to 2.7 RAM Data Retention Characteristics and modification of figure
		31	Addition of industrial application in 3.1 10-pin products
		32	Addition of industrial application in 3.2 16-pin products and modification of package drawing
3.10	Aug 12, 2016	1	Addition of description to Rich Analog in 1.1 Features
		3	Corrected Table 1-1. List of Ordering Part Numbers
		4	Modification of 1.3 Pin Configuration (Top View)
		31, 32	Deletion of under development