E·XFL



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe003hz010sg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

PIN DESCRIPTION

				-
PB1 C PB2 C PB3 C PB4 C PB5 C PA7 C PA6 C PA5 C	1	18-Pin DIP/SOIC	18	□ PB0 □ XTAL1 □ XTAL2 □ V _{SS} □ V _{CC} □ PA0 □ PA1 □ PA2
PA6 □ PA5 □				口 PA1 口 PA2
PA4 C	9		10	= PA3

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7-PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3-PA0	Port A, Pins 3,2,1,0	Input/Output
14	V _{CC}	Power Supply	
15	V _{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

Table 1. Standard Programming Mode





Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Pin #	Symbol	Function	Direction	
1	PGM	Program Mode	Input	
2–4	GND	Ground	•	
5	ADCLR/V _{PP}	Clear Clock/Program Voltage	Input	
6	NC	No Connection		
7–10	D7–D4	Data 7,6,5,4	Input/Output	
11–14	D3-D0	Data 3,2,1,0	Input/Output	
15	NC	No Connection		
16	V _{DD}	Power Supply		
17	GND	Ground		
18	NC	No Connection		
19	XTAL1	1-MHz Clock	Input	
20	ADCLK	Address Clock	Input	

Table 4. EPROM Programming Mode

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).



Figure 7. Test Load Diagram

CAPACITANCE

 T_{A} = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

DC ELECTRICAL CHARACTERISTICS

			T _A = 0°C Standard Te	to +70°C emperatures				
Svm	Parameter	V _{CC} ¹	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	3.0V	0.7V _{CC}	V _{CC} +0.3	1.3	V	Driven by External Clock Generator	
	-	5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} -0.3	$0.2V_{CC}$	0.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	$0.2V_{CC}$	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.0V	0.7V _{CC}	V _{CC} +0.3	1.3	V		
		5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	3.0V	V _{SS} -0.3	0.2V _{CC}	0.7	V		
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.5	V		
V _{OH}	Output High Voltage	3.0V	V _{CC} -0.4		3.1	V	I _{OH} = -2.0 mA	
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	
V _{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I _{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
V _{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I _{OL} = +6 mA	
		5.5V		1.2	0.5	V	I _{OL} = +12 mA	
VOFFSET	Comparator Input	3.0V		25.0	10.0	mV		
	Offset Voltage	5.5V		25.0	10.0	mV		
I _{IL}	Input Leakage	3.0V	-1.0	2.0	0.064	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1.0	2.0	0.064	μA	$V_{IN} = 0V, V_{CC}$	
I _{OL}	Output Leakage	3.0V	-1.0	2.0	0.114	μA	$V_{IN} = 0V, V_{CC}$	
		5.5V	-1.0	2.0	0.114	μA	$V_{IN} = 0V, V_{CC}$	
V _{ICR}	Comparator Input	3.0V	V _{SS} –0.3	V _{CC} -1.0		V		3
	Common Mode Voltage Range	5.5V	V _{SS} –0.3	V _{CC} -1.0		V		3
R _{PB5}	PB5 Pull-up Resistor	3.0V	100		200	kOhm		4
		5.5V	100		200			
V _{LV}	V _{CC} Low-Voltage Protection		2.45	2.85	2.60	V		

Table 5. DC Electrical Characteristics

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V. 2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.

3. For the analog comparator input when the analog comparator is enabled.

4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.

5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.

6. CL1 = CL2 = 22 pF.

7. Same as note 5, except inputs are at $V_{\mbox{\scriptsize CC}}.$

The device is based on the ZiLOG Z8Plus Core Architecture. This core is capable of addressing up to 64KB of program memory and 4 KB of RAM. Register RAM is accessed as either 8- or 16-bit registers using a combination of 4-, 8-, and 12-bit addressing modes. The architecture supports up to 15 vectored interrupts from external and internal sources. The processor decodes 44 CISC instructions using 6 addressing modes. See the <u>Z8Plus User's Manual</u> for more information.

RESET

This section describes the Z8Plus reset conditions, reset timing, and register initialization procedures. Reset is generated by the Voltage Brown-Out/Power-On Reset (VBO/POR), Watch-Dog Timer (WDT), and Stop-Mode Recovery (SMR).

A system reset overrides all other operating conditions and puts the Z8Plus device into a known state. To initialize the chip's internal logic, the POR device counts 64 internal clock cycles after the oscillator stabilizes. The control registers and ports are not reset to their default conditions after wakeup from a STOP mode or WDT time-out.

During **RESET**, the value of the program counter is 0020H. The I/O ports and control registers are configured to their default reset state. Resetting the device does not affect the contents of the general-purpose registers.

The **RESET** circuit initializes the control and peripheral registers, as shown in Table 8. Specific reset values are indicated by a 1 or a 0, while bits whose states are unchanged or unknown from Power-Up are indicated by the letter U.

Program execution starts 10 External Crystal (XTAL) clock cycles after the POR delay. The initial instruction fetch is from location 0020H. Figure 9 indicates reset timing.

After a reset, the first routine executed must be one that initializes the TCTLHI control register to the required system configuration This activity is followed by initialization of the remaining control registers.

					B	its				
Deviator (HEV)	Dogiotor Norro	7	c	F	4		2	1	•	Commente
Register (REA)	Register Name	/	O	5	4	3	2		U	
FF	Stack Pointer	0	0	U	U	U	U	U	U	Stack pointer is not affected by RESET.
FE	Reserved									
FD	Register Pointer	U	U	U	U	0	0	0	0	Register pointer is not affected by RESET.
FC	Flags	U	U	U	U	U	U	*	*	Only WDT & SMR flags are affected by RESET.
FB	Interrupt Mask	0	0	0	0	0	0	0	0	All interrupts masked by RESET.
FA	Interrupt Request	0	0	0	0	0	0	0	0	All interrupt requests cleared by RESET.
F9–F0	Reserved									
EF–E0	Virtual Copy									Virtual copy of the current working register set.
DF–D8	Reserved									
D7	Port B Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET.
D6	Port B Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortB after RESET.
D5	Port B Output	U	U	U	U	U	U	U	U	Output register not affected by RESET.
Note: *The SMR	and WDT flags are se	t to in	ndica	te the	sou	rce of	the I	RESE	Ŧ.	

Table 8. Control and Peripheral Registers*

Z8PE003 Z8Plus OTP Microcontroller

RESET (Continued)

Table 8. Control and Periphera	I Registers* (Continued)
--------------------------------	--------------------------

Bits										
Register (HEX)	Register Name	7	6	5	4	3	2	1	0	Comments
D4	Port B Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET.
D3	Port A Special Function	0	0	0	0	0	0	0	0	Deactivates all port special functions after RESET.
D2	Port A Directional Control	0	0	0	0	0	0	0	0	Defines all bits as inputs in PortA after RESET.
D1	Port A Output	U	U	U	U	U	U	U	U	Output register not affected by RESET
D0	Port A Input	U	U	U	U	U	U	U	U	Current sample of the input pin following RESET.
CF	Reserved									
CE	Reserved									
CD	T1VAL	U	U	U	U	U	U	U	U	
CC	T0VAL	U	U	U	U	U	U	U	U	
СВ	T3VAL	U	U	U	U	U	U	U	U	
СА	T2VAL	U	U	U	U	U	U	U	U	
C9	T3AR	U	U	U	U	U	U	U	U	
C8	T2AR	U	U	U	U	U	U	U	U	
C7	T1ARHI	U	U	U	U	U	U	U	U	
C6	T0ARHI	U	U	U	U	U	U	U	U	
C5	T1ARLO	U	U	U	U	U	U	U	U	
C4	T0ARLO	U	U	U	U	U	U	U	U	
С3	WDTHI	1	1	1	1	1	1	1	1	
C2	WDTLO	1	1	1	1	1	1	1	1	
C1	TCTLHI	1	1	1	1	1	0	0	0	WDT enabled in HALT mode, WDT time-out at maximum value, STOP mode disabled.
C0	TCTLLO	0	0	0	0	0	0	0	0	All standard timers are disabled.
Note: *The SMR	and WDT flags are se	et to ii	ndica	te the	e sou	rce of	the F	RESE	Ŧ.	

Table 9. Flag Register Bit D1, D0

D1	D0	Reset Source
0	0	V _{BO} /POR
0	1	SMR Recovery
1	0	WDT Reset
1	1	Reserved

IREQ SOFTWARE INTERRUPT GENERATION

IREQ can be used to generate software interrupts by specifying IREQ as the destination of any instruction referencing the Z8Plus Standard Register File. These software interrupts (SWI) are controlled in the same manner as hardware generated requests. In other words, the IMASK controls the enabling of each SWI.

To generate a SWI, the request bit in IREQ is set by the following statement:

OR IREQ, #NUMBER

The immediate data variable, NUMBER, has a 1 in the bit position corresponding to the required level of SWI. For example, an SWI must be issued when an IREQ5 occurs. Bit 5 of NUMBER must have a value of 1.

OR IREQ, #0010000B

If the interrupt system is globally enabled, IREQ5 is enabled, and there are no higher priority requests pending, control is transferred to the service routine pointed to by the IREQ5 vector.

Note: Software may modify the IREQ register at any time. Care should be taken when using any instruction that modifies the IREQ register while interrupt sources are active. The software writeback always takes precedence over the hardware. If a software writeback takes place on the same cycle as an interrupt source tries to set an IREQ bit, the new interrupt is lost.

Nesting of Vectored Interrupts

Nesting vectored interrupts allows higher priority requests to interrupt a lower priority request. To initiate vectored interrupt nesting, perform the following steps during the interrupt service routine:

- PUSH the old IMASK on the stack
- Load IMASK with a new mask to disable lower priority interrupts
- Execute an El instruction
- Proceed with interrupt processing
- Execute a DI instruction after processing is complete
- Restore the IMASK to its original value by POPing the previous mask from the stack
- Execute IRET

Depending on the application, some simplification of the above procedure may be possible.

RESET Conditions

The IMASK and IREQ registers initialize to 00h on RESET.

PROGRAMMABLE OPTIONS

EPROM Protect. When selecting the DISABLE EPROM PROTECT/ENABLE TESTMODE option, the user can read the software code in the program memory. ZiLOG's internal factory test mode, or any of the standard test mode methods, are useful for reading or verifying the code in the microcontroller when using an EPROM programmer. If the user should select the ENABLE EPROM PROTECT/DIS-ABLE TESTMODE option, it is not possible to read the code using a tester, programmer, or any other standard method. As a result, ZiLOG is unable to test the EPROM memory at any time after customer delivery. This option bit only affects the user's ability to read the code and has no effect on the operation of the part in an application. ZiLOG tests the EPROM memory before customer delivery whether or not the ENABLE EPROM PRO-TECT/DISABLE TESTMODE option is selected; ZiLOG provides a standard warranty for the part.

System Clock Source. When selecting the RC OSCILLA-TOR ENABLE option, the oscillator circuit on the microcontroller is configured to work with an external RC circuit. When selecting the Crystal/Other Clock Source option, the oscillator circuit is configured to work with an external crystal, ceramic resonator, or LC oscillator.

WATCH-DOG TIMER

The Watch-Dog Timer (WDT) is a retriggerable one-shot 16-bit timer that resets the device if it reaches its terminal count. The WDT is driven by the XTAL2 clock pin. To provide the longer time-out periods required in applications, the watch-dog timer is only updated every 64th clock cycle. When operating in the RUN or HALT modes, a WDT timeout reset is functionally equivalent to an interrupt vectoring the PC to 0020H, and setting the WDT flag to 1. Coming out of **RESET**, the WDT is fully enabled with its time-out value set at minimum, unless otherwise programmed during the first instruction. Subsequent executions of the WDT instruction reinitialize the watch-dog timer registers (C2h and C3h) to their initial values as defined by bits D6, D5, and D4 of the TCTLHI register. The WDT cannot be disabled except on the first cycle after **RESET** and when the device enters STOP mode.

The WDT instruction should be executed often enough to provide some margin of time to allow the WDT registers to approach 0. Because the WDT time-out periods are relatively long, a WDT $\overrightarrow{\text{RESET}}$ occurs in the unlikely event that the WDT times out on exactly the same cycle that the WDT instruction is executed.

RESET clears both the WDT and SMR flags. A WDT timeout sets the WDT flag, and the STOP instruction sets the SMR flag. This function enables software to determine whether a WDT time-out or a return from STOP mode occurred. Reading the WDT and SMR flags does not reset the flag to 0; therefore, the user must clear the flag via software.

Note: Failure to clear the SMR flag can result in unexpected behavior.



Figure 11. TCTLHI Register for Control of WDT

The STOP mode provides the lowest possible device standby current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP mode, the Z8Plus only requires a STOP instruction. It is *not* necessary to execute a NOP instruction immediately before the STOP instruction.

6F STOP ;enter STOP mode

The STOP mode is exited by any one of the following resets: POR or a Stop-Mode Recovery source. At reset generation, the processor always restarts the application program at address 0020H, and the STOP mode flag is set. Reading the STOP mode flag does not clear it. The user must clear the STOP mode flag with software.

Note: Failure to clear the STOP mode flag can result in undefined behavior.

The Z8Plus provides a dedicated Stop-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin

(SMR) circuit. In this case, a low-level applied to input pin PB0 (I/O Port B, bit 0) triggers an SMR. To use this mode, pin PB0 must be configured as an input and the special function selected before the STOP mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM} . Program execution starts at address 20h, after the POR delay.

Notes: 1. The PB0 input, when used for Stop-Mode Recovery, does not initialize the control registers.

The STOP mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the device's operating range
- Output current sourcing is minimized
- All inputs (digital and analog) are at the Low or High rail voltages
- 2. For detailed information about flag settings, see the <u>Z8Plus User's Manual</u>.



Figure 20. 8-Bit Standard Timers



Figure 21. 16-Bit Standard PWM Timer



T1 (MSB) and T0 (LSB). T23 is a standard 16-bit timer formed by cascading 8-bit timers T3 (MSB) and T2 (LSB).



A pair of READ/WRITE registers is utilized for each 8-bit timer. One register is defined to contain the auto-initialization value for the timer. The second register contains the current value for the timer. When a timer is enabled, the timer decrements the value in its count register and continues decrementing until it reaches 0. An interrupt is generated, and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer stops counting when the value reaches 0. Control logic clears the appropriate control register bit to disable the timer. This operation is referred to as a *single-shot*. If auto-initialization is enabled, the timer counts from the initialization value. Software must not attempt to use timer registers for any other function.

User software is allowed to write to any WRITE register at any time; however, care should be taken if timer registers are updated while the timer is enabled. If software changes the count value while the timer is in operation, the timer continues counting from the updated value. **Note:** Unpredictable behavior can occur if the value updates at the same time that the timer reaches 0.

Similarly, if user software changes the initialization value register while the timer is active, the next time that the timer reaches 0, the timer initializes to the changed value.

Note: Unpredictable behavior can occur if the initialization value register is changed while the timer is in the process of being initialized.

The initialization value is determined by the exact timing of the WRITE operation. In all cases, the Z8Plus assigns a higher priority to the software WRITE than to a decrementer write-back. However, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software WRITE. A READ of either register can be conducted at any time, with no effect on the functionality of the timer.











Figure 25. Timer T0 Output Through T_{OUT}

RESET CONDITIONS

After a $\overline{\text{RESET}}$, the timers are disabled. See Table 8 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8Plus dedicates 14 lines to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide either standard input/output, or the following special functions: T0 output, comparator input, SMR input, and external interrupt inputs. All pins except PB5 include push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation. The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers (Figure 26).



Directional Control and Special Function Registers

Each port on the Z8Plus features a dedicated directional control register that determines (on a bit-wise basis) if a given port bit operates as input or output.

Each port on the Z8Plus features a special function register (SFR) that, in conjunction with the directional control register, implements (on a bit-by-bit basis) any special functionality that can be defined for each particular port bit.

Table 14. I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port features an Output Value Register and an input value register. For port bits configured as an input by means of the directional control register, the input value register

PORT A REGISTER DIAGRAMS















Figure 31. Port A Special Function Register

PORT B

Port B Description

Port B is a 6-bit (bidirectional), CMOS-compatible I/O port. These six I/O lines can be configured under software control to be an input or output. Each bit is configured independently from the other bits. That is, one bit may be set to INPUT while another bit is set to OUTPUT.

In addition to standard input/output capability, five pins of Port B provide special functionality as indicated in Table 15.

Special functionality is invoked via the Port B special function register. Port B, bit 5, is an open-drain-only pin when in output mode. There is no high-side driver on the output stage, nor is there any high-side protection device, because PB5 acts as the V_{PP} pin for EPROM programming mode. The user should always place an external protection diode on this pin. See Figure 32.

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	T0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

Table '	15.	Port	B	Special	Functions
---------	-----	------	---	---------	-----------





PORT B—PIN 1 CONFIGURATION





PORT B—PIN 2 CONFIGURATION



Figure 36. Port B Pin 2 Diagram

COMPARATOR OPERATION (Continued)

age Protection trip point $(\mathsf{V}_{\mathsf{LV}})$ is reached. The actual Low-Voltage Protection trip point is a function of process parameters.

Low-Voltage Protection is active in RUN and HALT modes only, but is disabled in STOP mode (Figure 42).



Figure 42. Typical Low Voltage Protection vs. Temperature

PACKAGE INFORMATION



MILLIMETER INCH SYMBOL MIN MAX MIN MAX 0.51 0.81 .020 .032 3.25 3.43 .128 .135 0.38 0.53 .015 .021 1.14 1.65 .045 .065 0.23 0.38 .009 .015 22.35 23.37 .880 .920 7.62 8.13 .300 .320 6.22 6.48 .245 .255 2.54 TYP .100 TYP 7.87 8.89 .310 .350 3.18 3.81 .125 .150 1.52 1.65 .060 .065 1.65 .035 .065

CONTROLLING DIMENSIONS : INCH





CYLLDOI	MILLIMETER		INCH		
21MBOL	MIN	МАХ	MIN	МАХ	
A	2.40	2.65	0.094	0.104	
A1	0.10	0.30	0.004	0.012	
A2	2.24	2.44	0.088	0.096	
В	0.36	0.46	0.014	0.018	
С	0.23	0.30	0.009	0.012	
D	11.40	11.75	0.449	0.463	
Ε	7.40	7.60	0.291	0.299	
(e)	1.27	1.27 TYP		0.050 TYP	
н	10.00	10.65	0.394	0.419	
h	0.30	0.50	0.012	0.020	
L	0.60	1.00	0.024	0.039	
Q1	0.97	1.07	0.038	0.042	

CONTROLLING DIMENSIONS : MM LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 46. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
8	0.25	0.30	0.38	0.010	0.012	0.015
С	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			1	0.0256 TY	P
н	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram