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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	18-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe003pz010ec

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low; and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

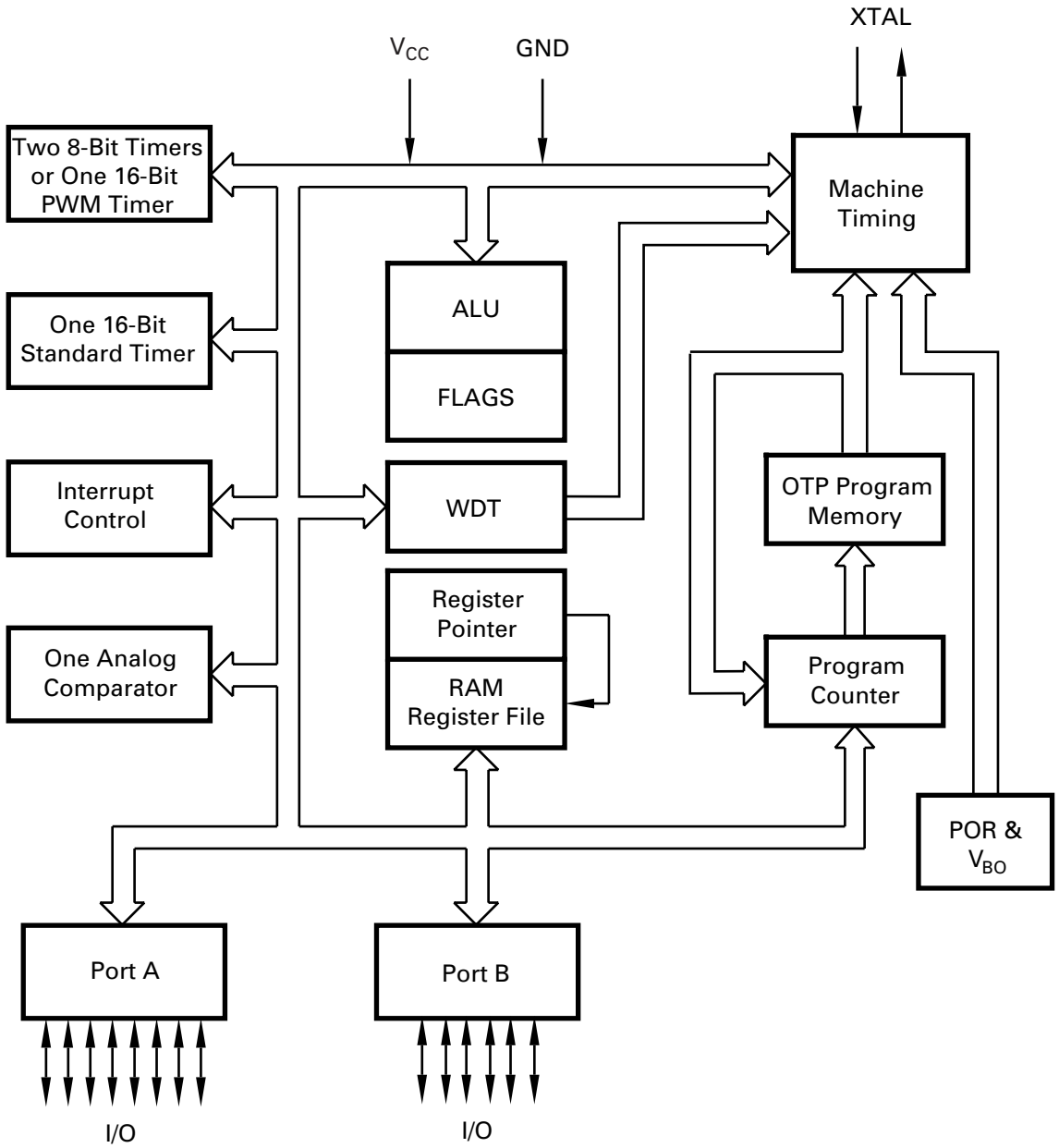


Figure 1. Functional Block Diagram

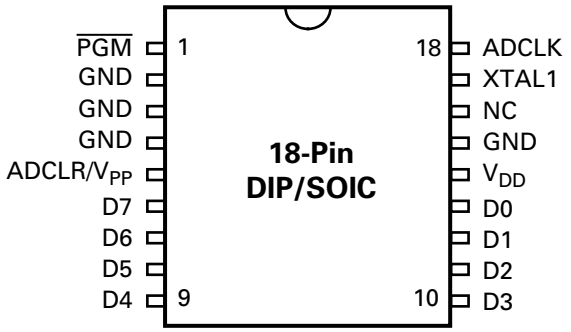


Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1-MHz Clock	Input
18	ADCLK	Address Clock	Input

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to Ground. Positive current flows into the referenced pin (Figure 7).

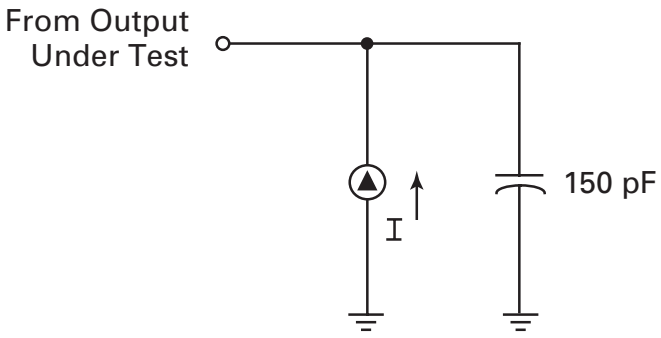


Figure 7. Test Load Diagram

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, unmeasured pins returned to GND.

Parameter	Min	Max
Input capacitance	0	12 pF
Output capacitance	0	12 pF
I/O capacitance	0	12 pF

Table 5. DC Electrical Characteristics (Continued)

			T_A = 0ºC to +70ºC Standard Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	5,6
		5.5V		6.0	3.5	mA	@ 10 MHz	5,6
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current			500	150	nA	STOP mode V_{IN} = 0V, V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 6. DC Electrical Characteristics (Continued)

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7
		5.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

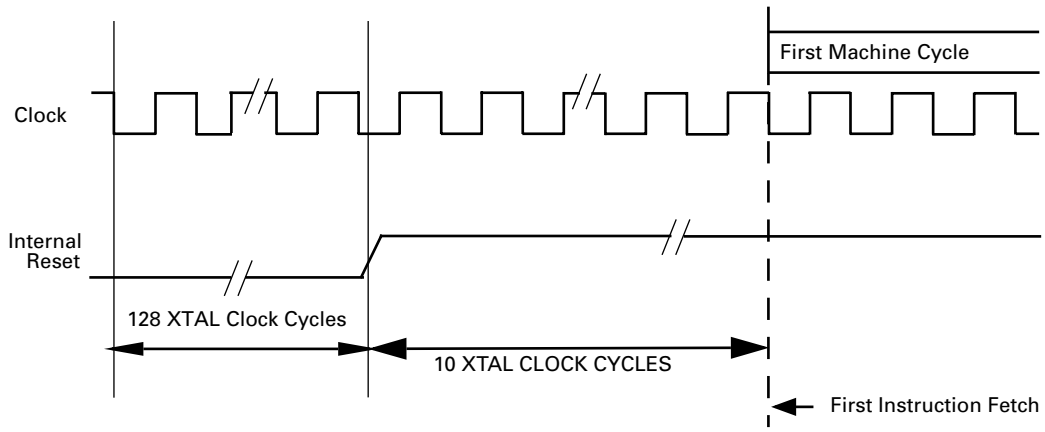


Figure 9. Reset Timing

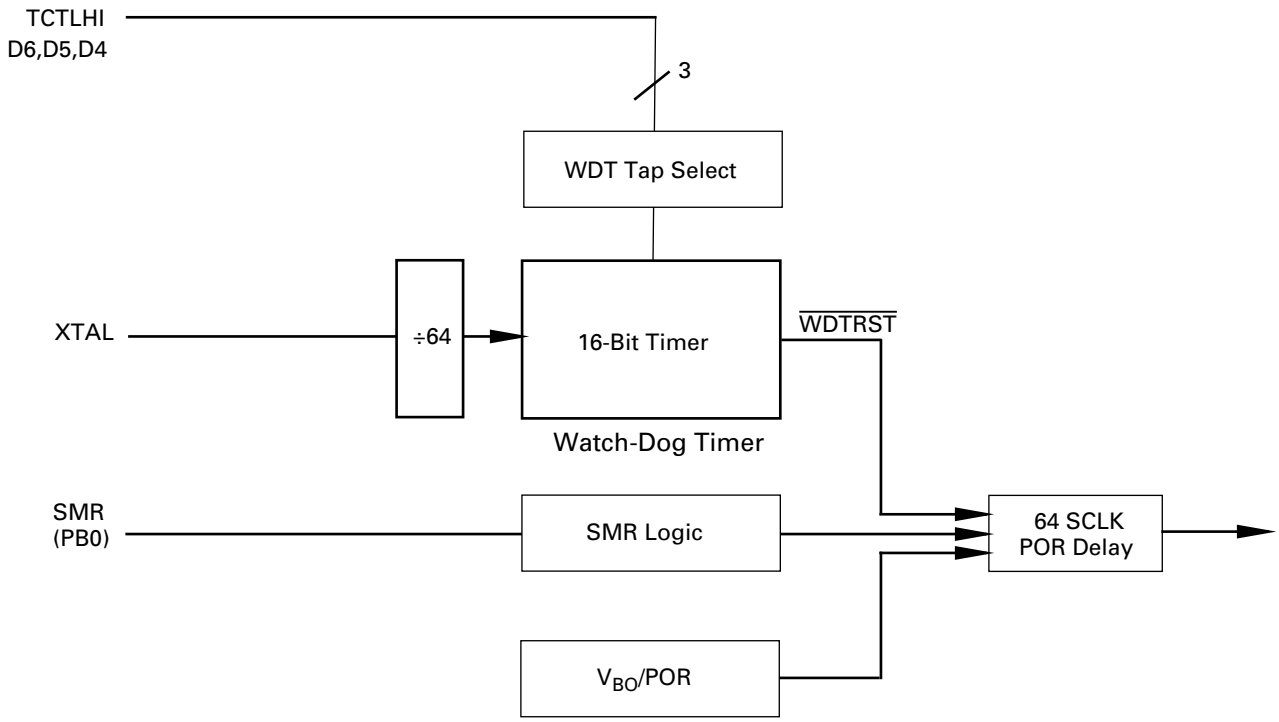


Figure 10. Reset Circuitry with POR, WDT, V_{BO}, and SMR

Table 11. Interrupt Mask Register—IMASK (FBh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate U = Undefined/ Undetermined								

Bit Position	R/W	Value	Description
7		0 1	Disables Interrupts Enables Interrupts
6		0	Reserved, must be 0
5		0 1	Disables IRQ5 Enables IRQ5
4		0 1	Disables IRQ4 Enables IRQ4
3		0 1	Disables IRQ3 Enables IRQ3
2		0 1	Disables IRQ2 Enables IRQ2
1		0 1	Disables IRQ1 Enables IRQ1
0		0 1	Disables IRQ0 Enables IRQ0

Interrupt Request (IREQ) Register Initialization

IREQ (Table 12) is a register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt is issued, the corresponding bit position in the register is set to 1. Bits 0 to 5 are assigned to interrupt requests IREQ0 to IREQ5, respectively.

Whenever RESET is executed, the IREQ resistor is set to 00h.

Table 12. Interrupt Request Register–IREQ (FAh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate U = Undefined/ Undetermined								

Bit Position	R/W	Value	Description
7	R/W	0	Reserved, must be 0
6	R/W	0	Reserved, must be 0
5	R/W	0 1	IRQ5 reset IRQ5 set
4	R/W	0 1	IRQ4 reset IRQ4 set
3	R/W	0 1	IRQ3 reset IRQ3 set
2	R/W	0 1	IRQ2 reset IRQ2 set
1	R/W	0 1	IRQ1 reset IRQ1 set
0	R/W	0 1	IRQ0 reset IRQ0 set

STOP MODE OPERATION

The STOP mode provides the lowest possible device stand-by current. This instruction turns off the on-chip oscillator and internal system clock.

To enter the STOP mode, the Z8Plus only requires a STOP instruction. It is *not* necessary to execute a NOP instruction immediately before the STOP instruction.

```
6F   STOP   ;enter STOP mode
```

The STOP mode is exited by any one of the following resets: POR or a Stop-Mode Recovery source. At reset generation, the processor always restarts the application program at address 0020H, and the STOP mode flag is set. Reading the STOP mode flag does not clear it. The user must clear the STOP mode flag with software.

Note: Failure to clear the STOP mode flag can result in undefined behavior.

The Z8Plus provides a dedicated Stop-Mode Recovery (SMR) circuit. In this case, a low-level applied to input pin PB0 (I/O Port B, bit 0) triggers an SMR. To use this mode, pin PB0 must be configured as an input and the special function selected before the STOP mode is entered. The Low level on PB0 must be held for a minimum pulse width T_{WSM}. Program execution starts at address 20h, after the POR delay.

Notes: 1. The PB0 input, when used for Stop-Mode Recovery, does not initialize the control registers.

The STOP mode current (I_{CC2}) is minimized when:

- V_{CC} is at the low end of the device's operating range
- Output current sourcing is minimized
- All inputs (digital and analog) are at the Low or High rail voltages

2. For detailed information about flag settings, see the Z8Plus User's Manual.

OSCILLATOR OPERATION

The Z8Plus MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

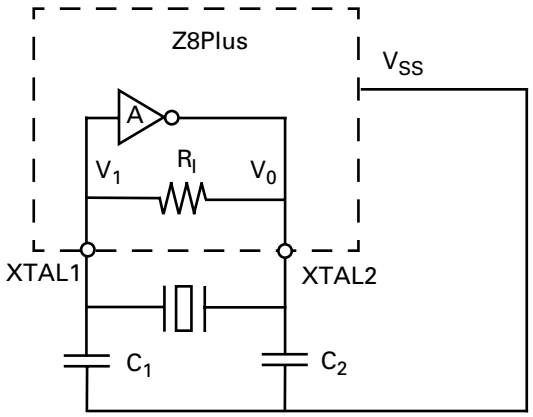


Figure 14. Pierce Oscillator with Internal Feedback Circuit

One drawback to the Pierce oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements. A x B = 1; where A = VO/VI is the gain of the amplifier, and B = VI/VO is the gain of the feedback element. The total phase shift around the loop is forced to 0 (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

Start-up time may be affected if C_1 and C_2 are increased dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it ceases to operate.

For fast and reliable oscillator start-up over the manufacturing process range, the load capacitors should be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8Plus oscillator pins should be as short and wide as possible to reduce parasitic inductance and resistance. The components (caps, the crystal, and resistors) should be placed as close as possible to the oscillator pins of the Z8Plus.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, and system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8Plus device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8Plus device V_{SS} (GND) pin. It should not be shared with any other system-ground trace or components except at the Z8Plus device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-Up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the C_1 and C_2 capacitors require reduction. The amplifier gain is either not adequate at frequency, or the crystal R's are too large.

Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

OSCILLATOR OPERATION (Continued)

Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8Plus as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 meg-Ohms.

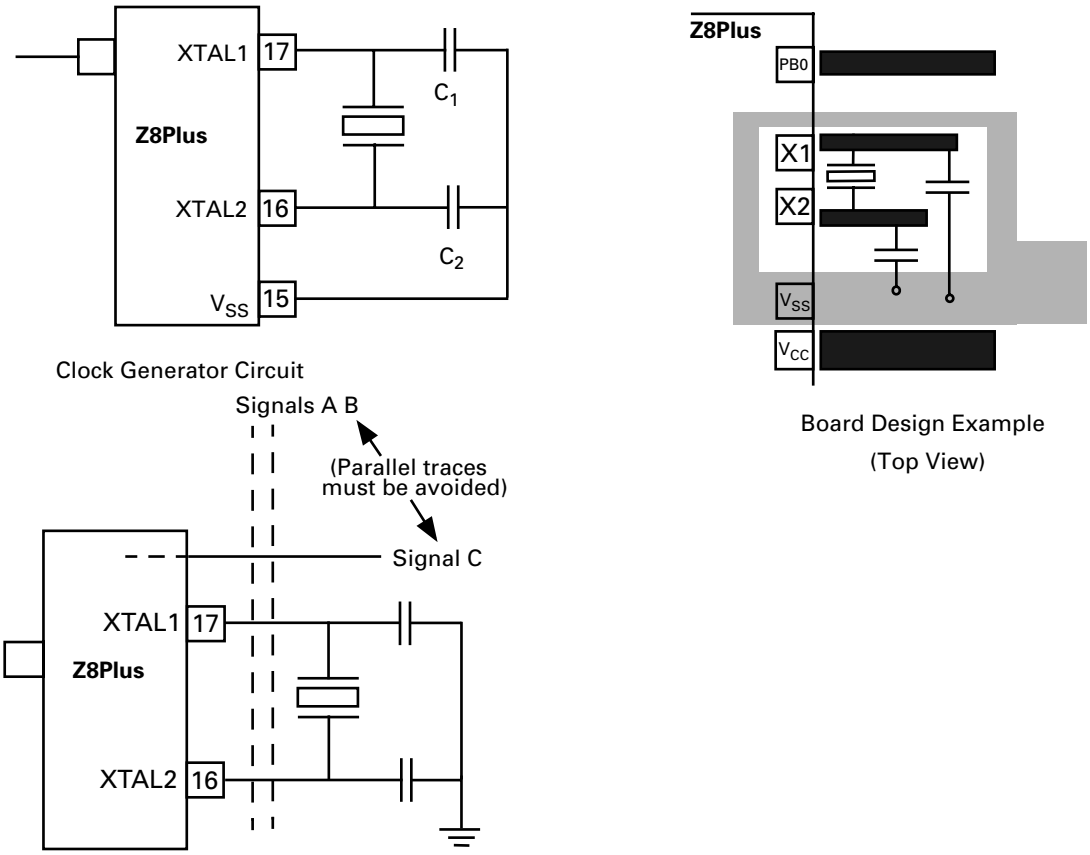


Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should exhibit the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, fundamental mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF,
	15 typical
Resistance	100 Ohms maximum

Depending on the operation frequency, the oscillator may require additional capacitors, C_1 and C_2, as illustrated in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturer's crystal specifications.

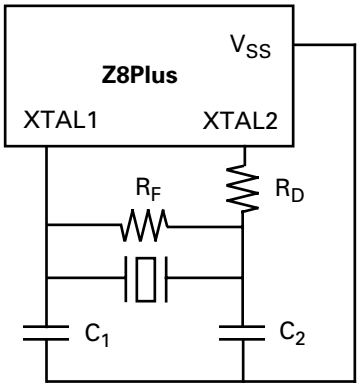


Figure 16. Crystal/Ceramic Resonator Oscillator

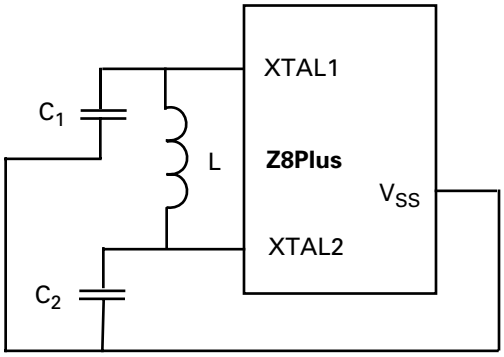


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

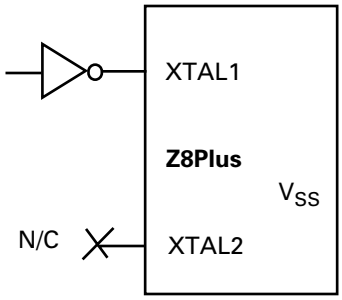


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8Plus oscillator can use an inductor capacitor oscillator (LC) network to generate an XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$1/C_T = 1/C_1 + 1/C_2$$
$$\text{If } C_1 = C_2$$
$$1/C_T = 2/C_1$$
$$C_1 = 2C_T$$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 µH is displayed as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi [27\ (10^{-6})\ C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pF}$$

Thus, C_1 = 55.2 pF and C_2 = 55.2 pF.

TIMERS

Two 8-bit timers, timer 0 (T0) and timer 1 (T1) are available to function as a pair of independent 8-bit standard timers. They may also be cascaded to function as a 16-bit Pulse-Width Modulator (PWM) timer. Two additional 8-bit timers (T2 and T3) are provided, but they can only operate as one 16-bit standard timer.

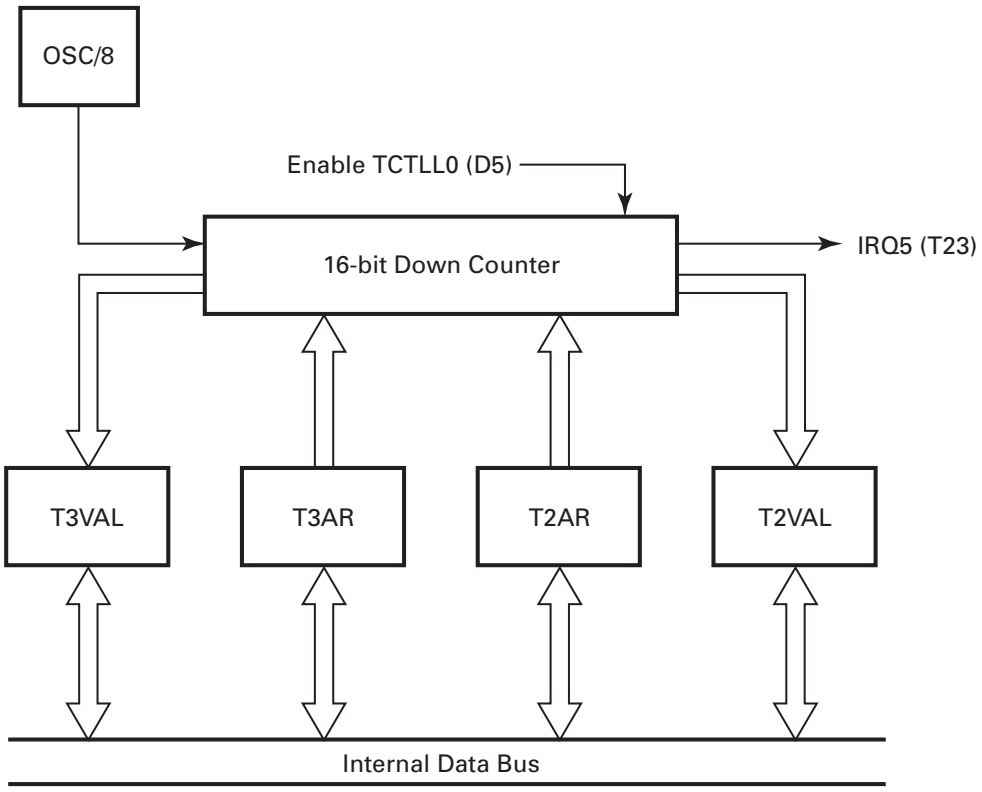


Figure 19. 16-Bit Standard Timer

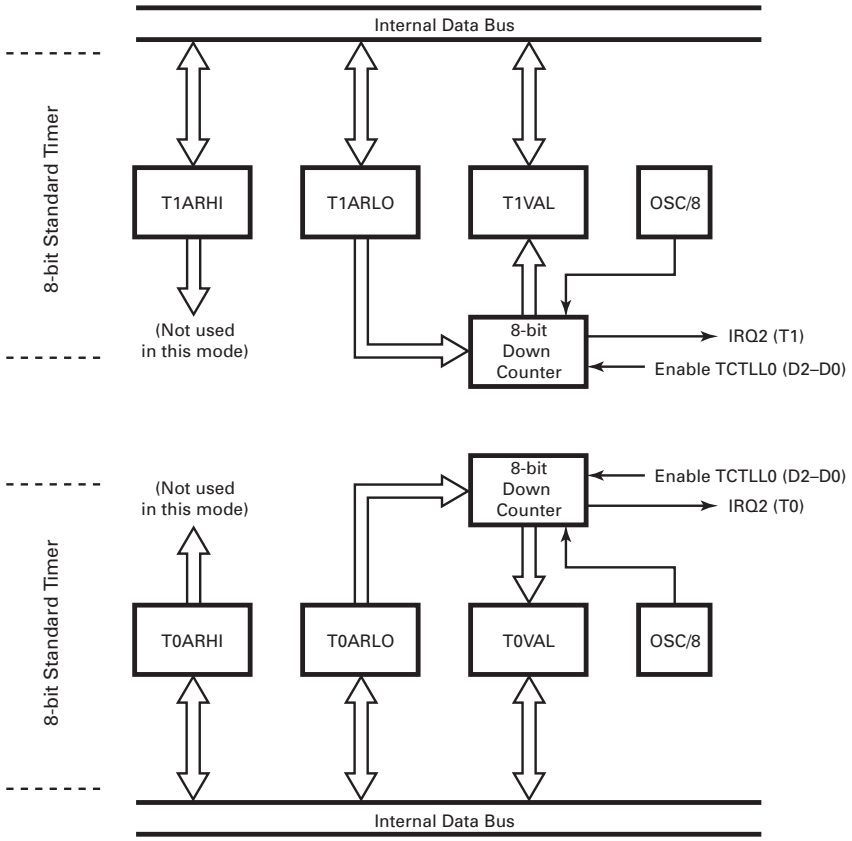


Figure 20. 8-Bit Standard Timers

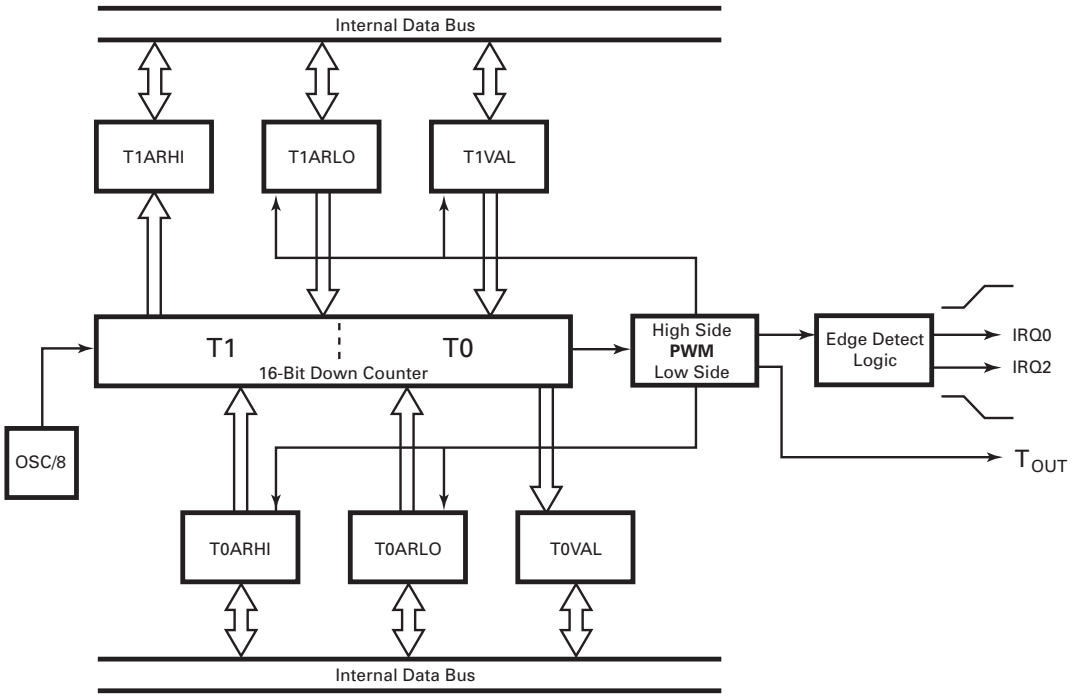
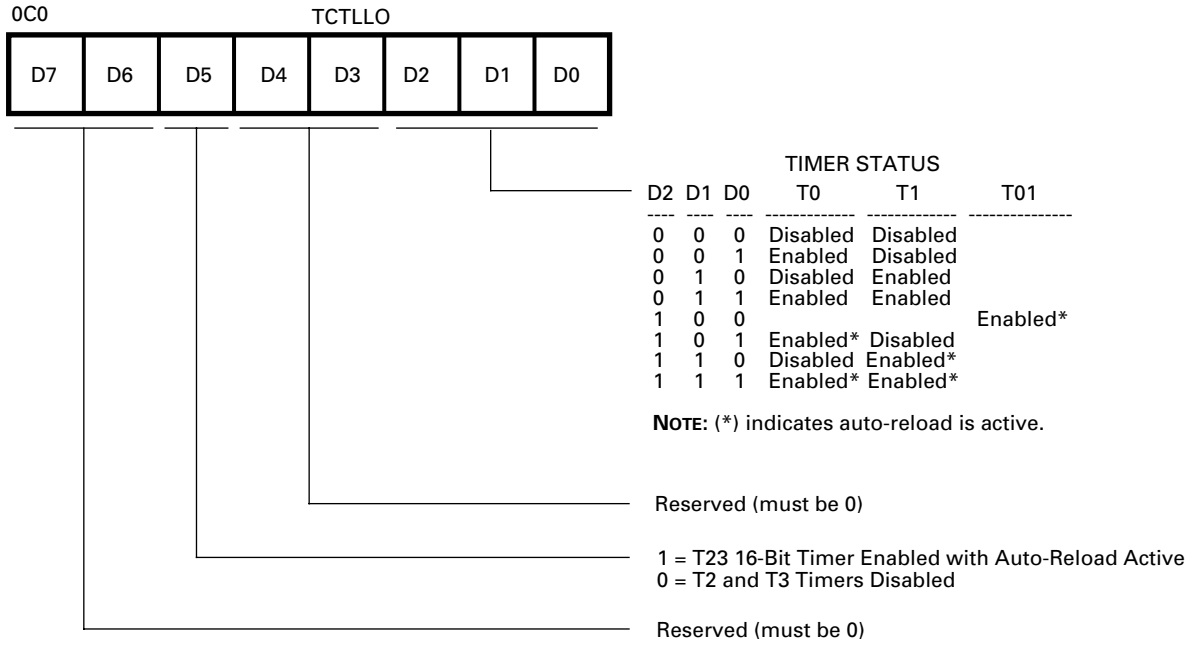


Figure 21. 16-Bit Standard PWM Timer

TIMERS (Continued)



Note: Timer T01 is a 16-bit PWM Timer formed by cascading 8-bit timers T1 (MSB) and T0 (LSB). T23 is a standard 16-bit timer formed by cascading 8-bit timers T3 (MSB) and T2 (LSB).

Figure 22. TCTLLO Register

A pair of READ/WRITE registers is utilized for each 8-bit timer. One register is defined to contain the auto-initialization value for the timer. The second register contains the current value for the timer. When a timer is enabled, the timer decrements the value in its count register and continues decrementing until it reaches 0. An interrupt is generated, and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer stops counting when the value reaches 0. Control logic clears the appropriate control register bit to disable the timer. This operation is referred to as a *single-shot*. If auto-initialization is enabled, the timer counts from the initialization value. Software must not attempt to use timer registers for any other function.

User software is allowed to write to any WRITE register at any time; however, care should be taken if timer registers are updated while the timer is enabled. If software changes the count value while the timer is in operation, the timer continues counting from the updated value.

Note: Unpredictable behavior can occur if the value updates at the same time that the timer reaches 0.

Similarly, if user software changes the initialization value register while the timer is active, the next time that the timer reaches 0, the timer initializes to the changed value.

Note: Unpredictable behavior can occur if the initialization value register is changed while the timer is in the process of being initialized.

The initialization value is determined by the exact timing of the WRITE operation. In all cases, the Z8Plus assigns a higher priority to the software WRITE than to a decrementer write-back. However, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software WRITE. A READ of either register can be conducted at any time, with no effect on the functionality of the timer.

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port's directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

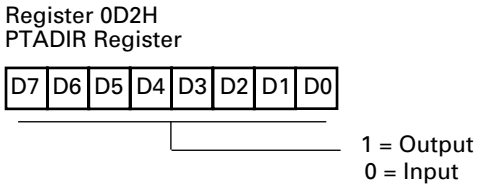


Figure 27. Port A Directional Control Register

PORT B—PIN 0 CONFIGURATION

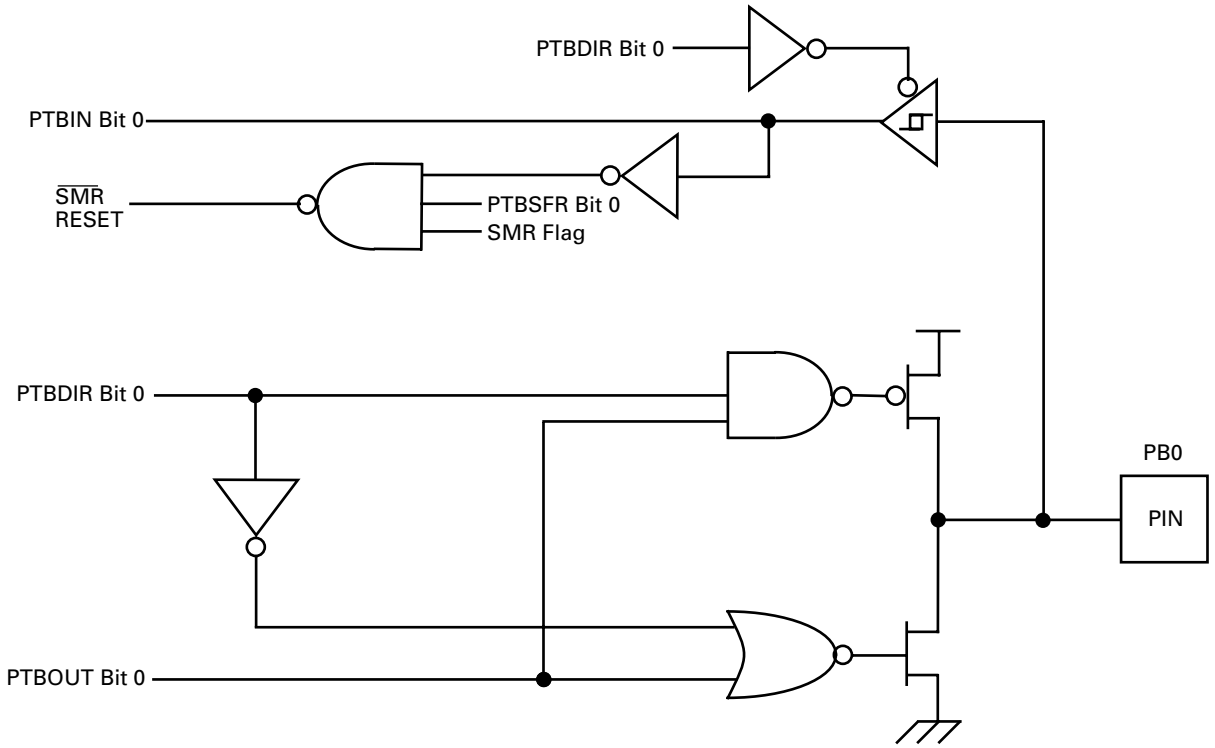
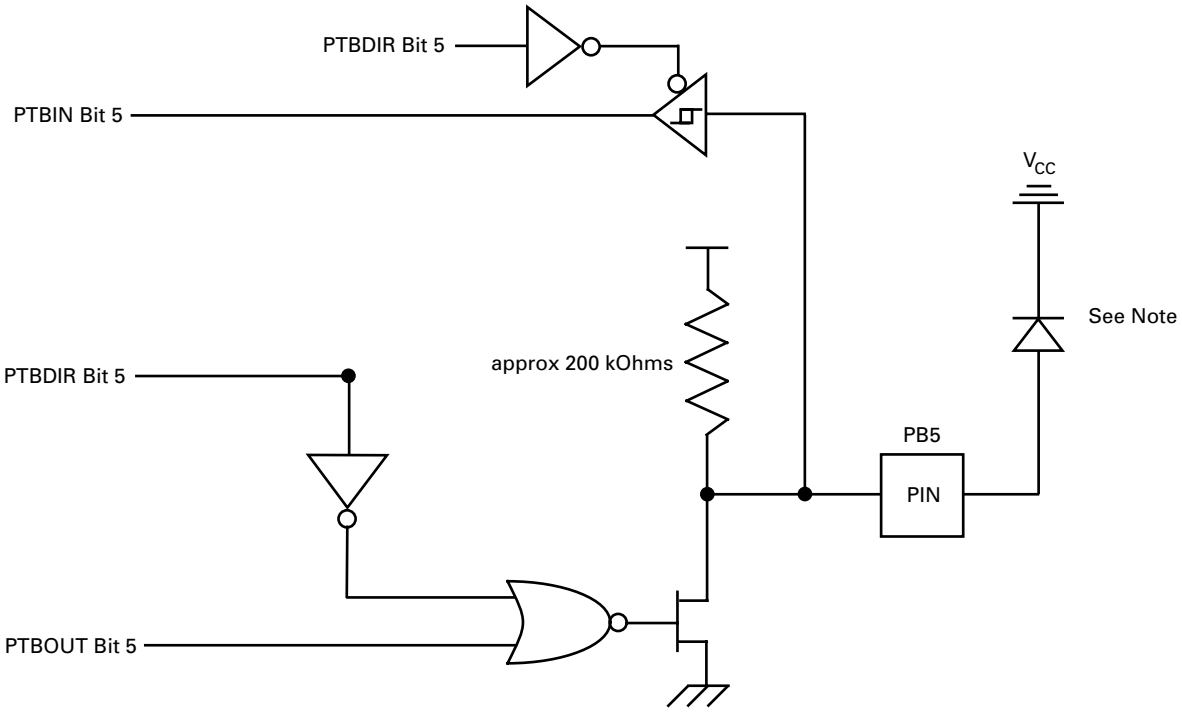


Figure 33. Port B Pin 0 Diagram



Note: There is no high-side protection device. The user should always place an external protection diode as shown.

Figure 34. Port B Pin 5 Diagram

PORT B—PIN 1 CONFIGURATION

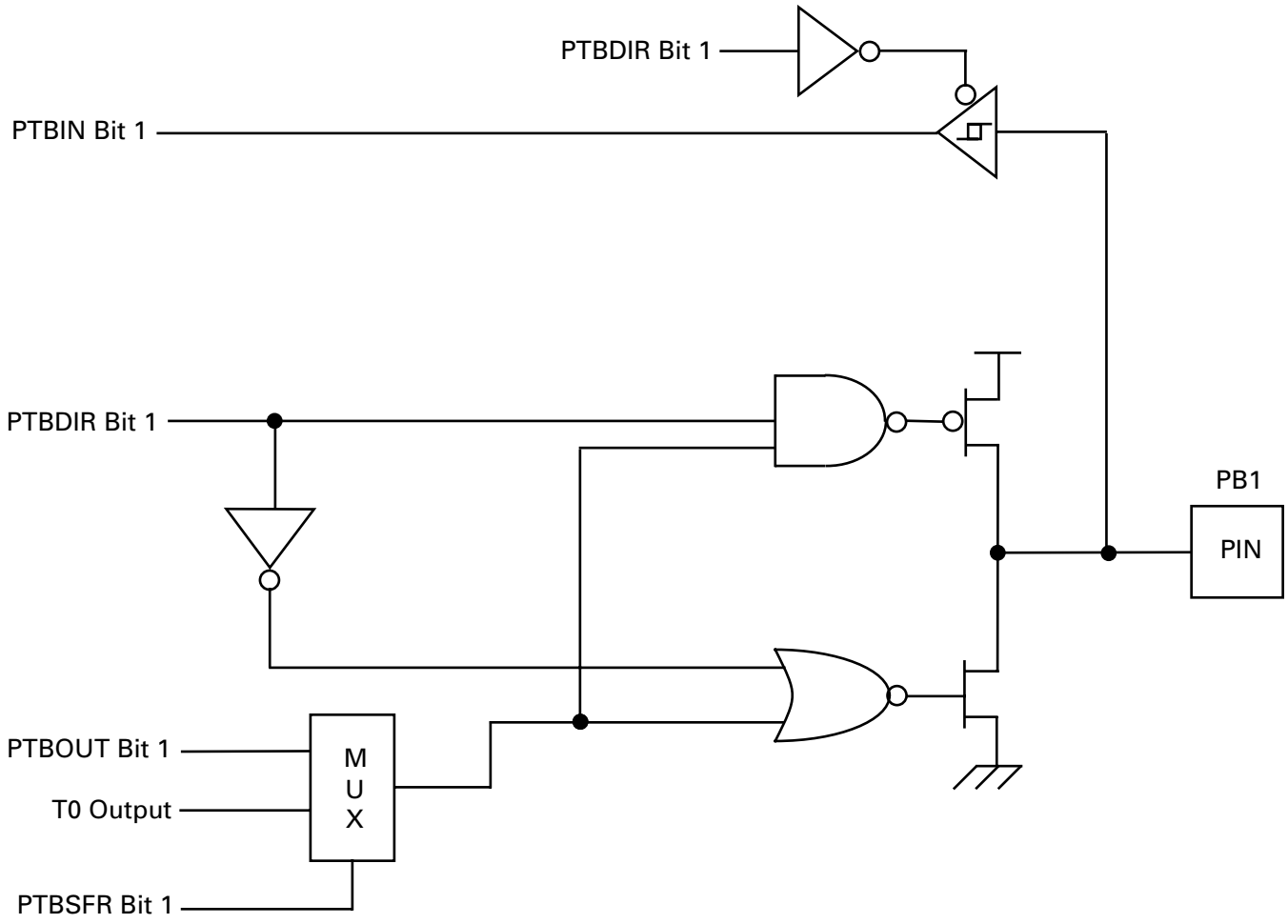


Figure 35. Port B Pin 1 Diagram

PORT B—PINS 3 AND 4 CONFIGURATION

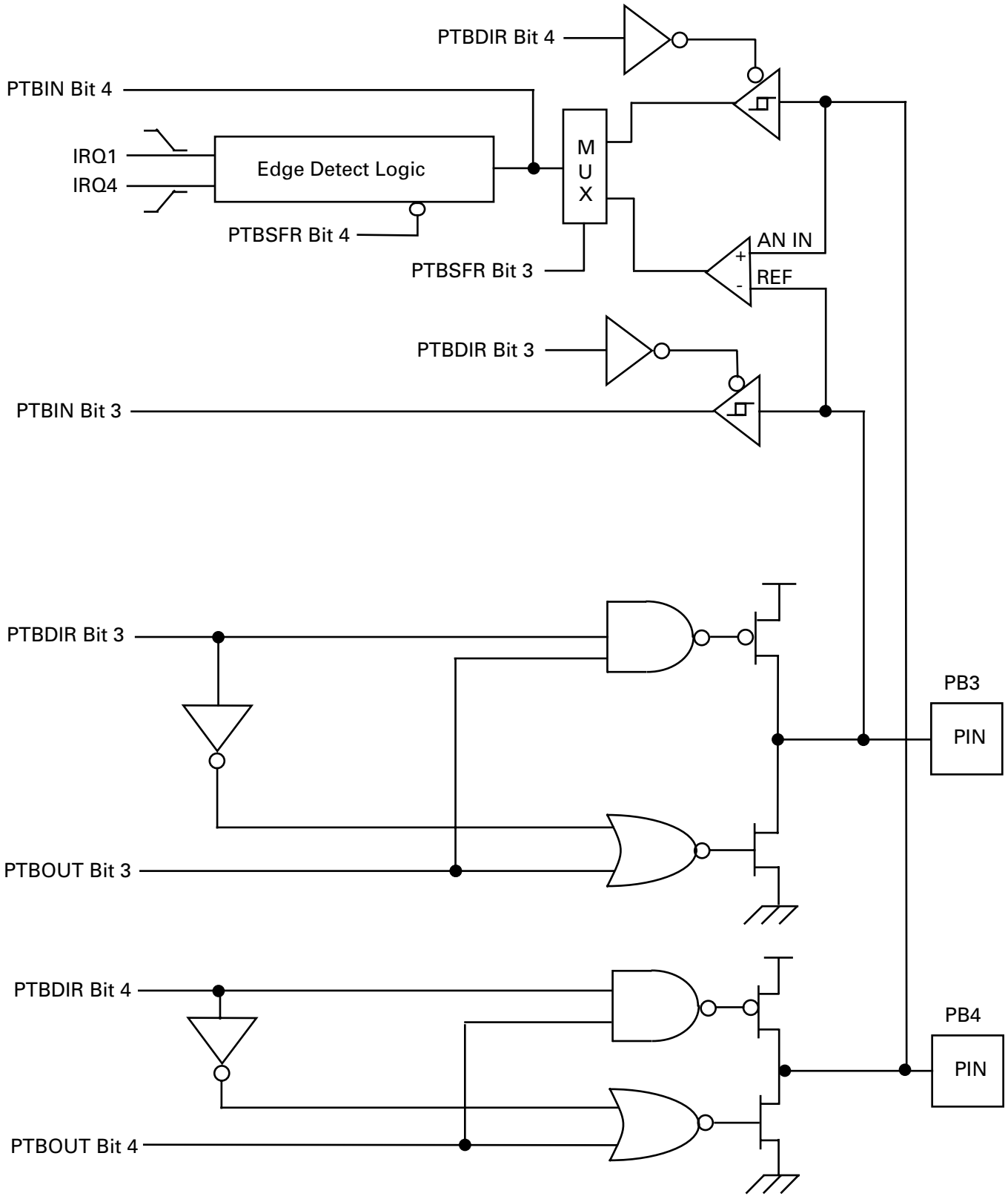


Figure 37. Port B Pins 3 and 4 Diagram

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

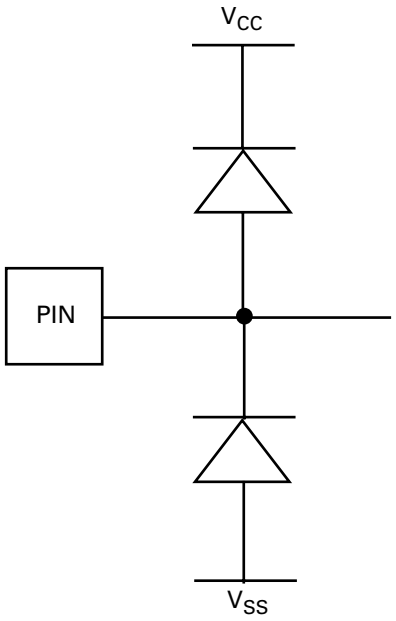


Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

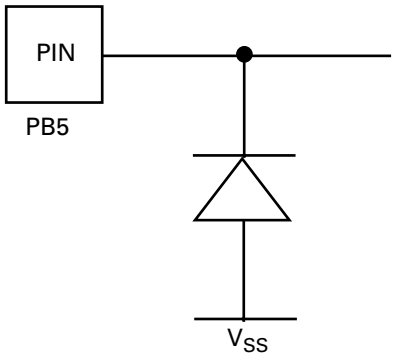
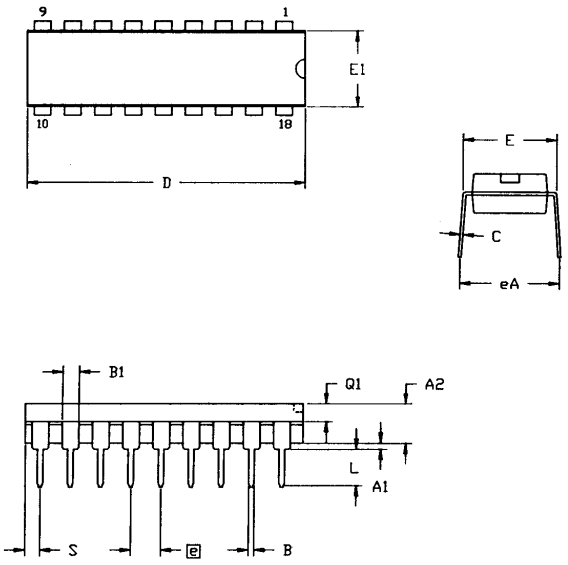


Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

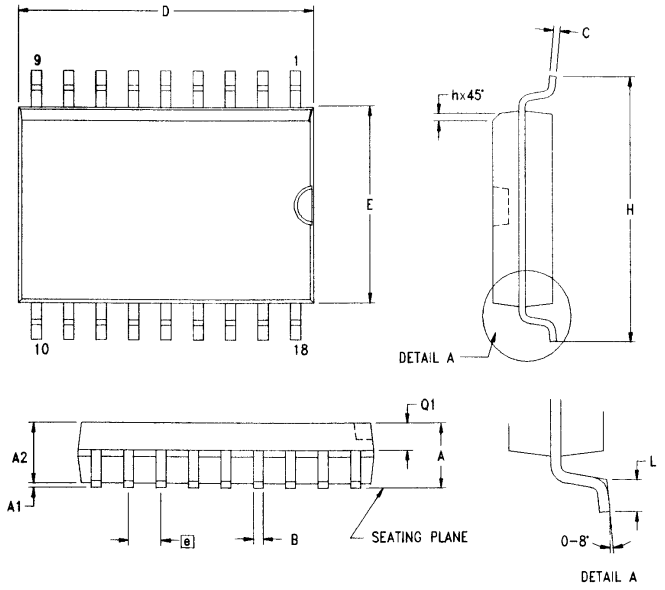
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

Figure 45. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 46. 18-Pin SOIC Package Diagram