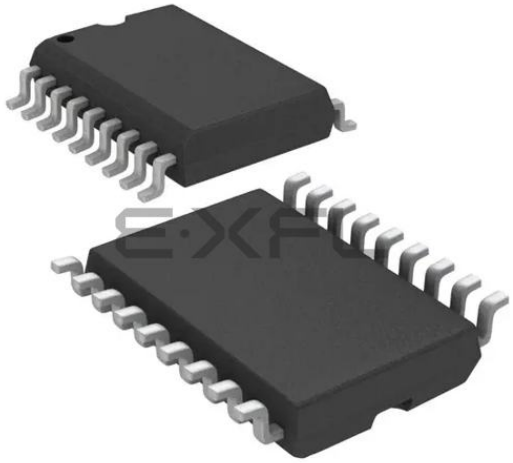

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe003sz010ec

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low; and $\overline{B}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

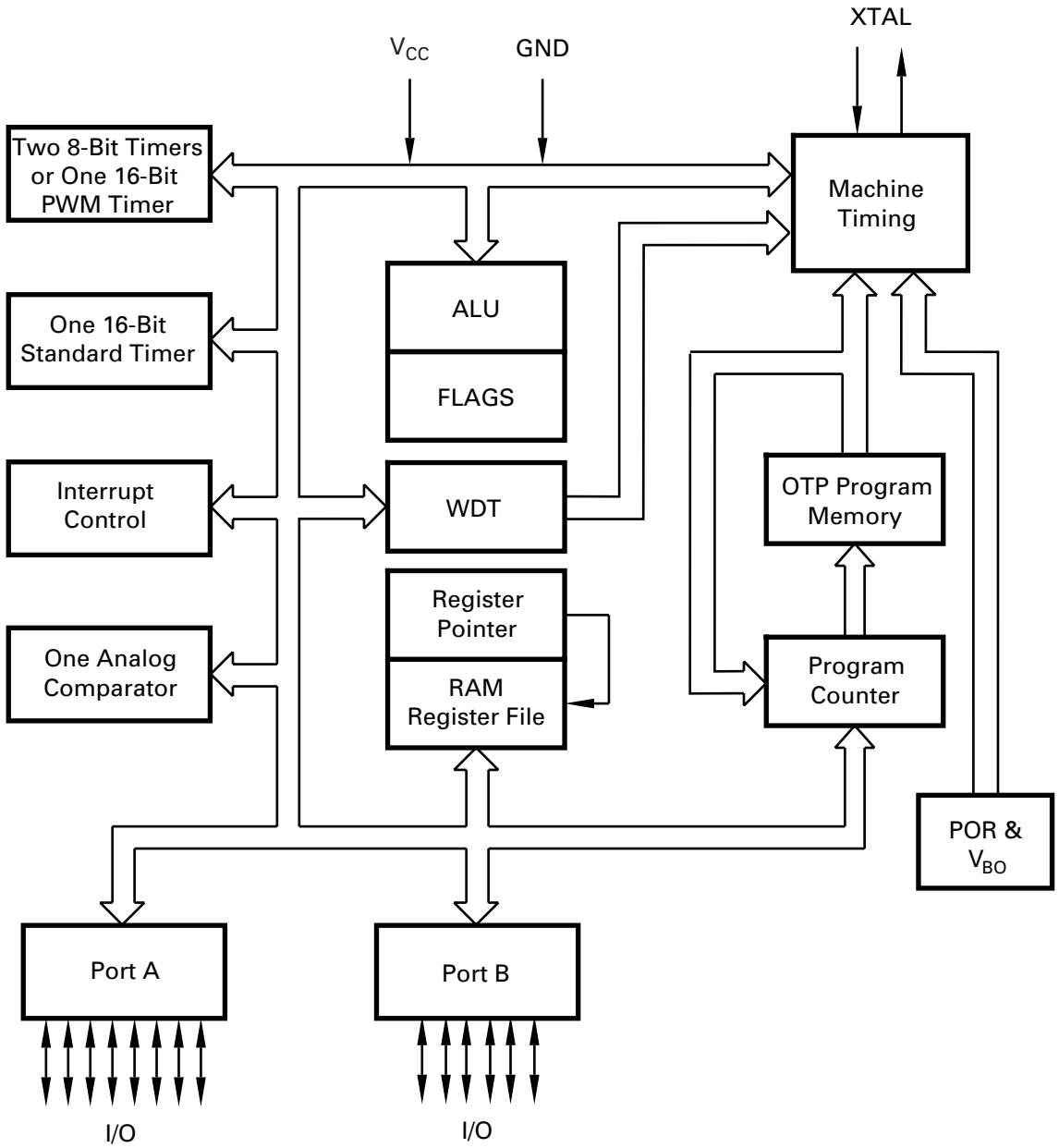


Figure 1. Functional Block Diagram

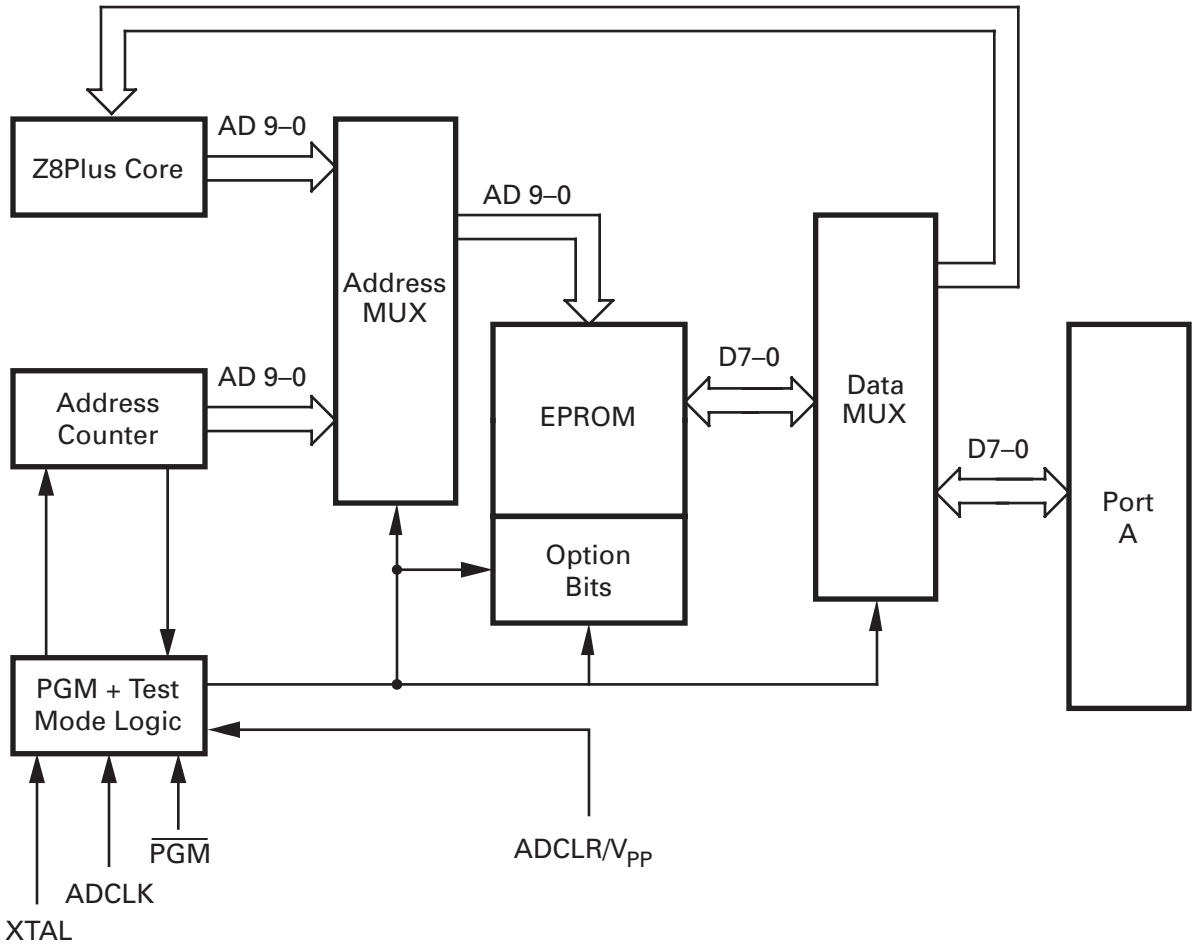


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

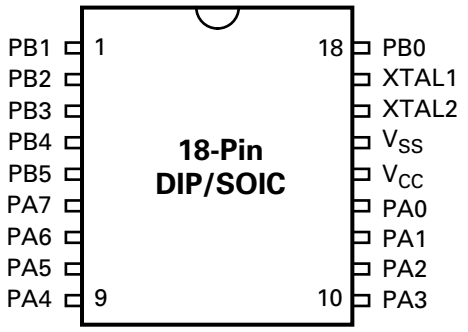


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V_{CC}	Power Supply	
15	V_{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

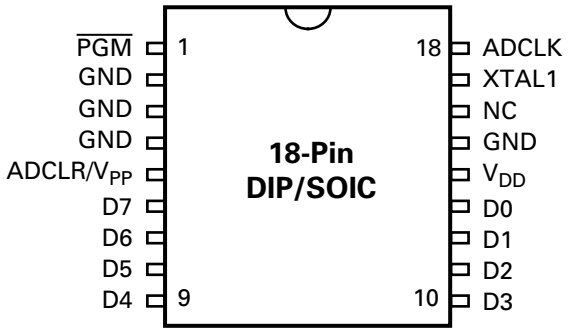


Figure 4. 18-Pin DIP/SOIC Pin Identification

Table 2. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6–9	D7–D4	Data 7,6,5,4	Input/Output
10–13	D3–D0	Data 3,2,1,0	Input/Output
14	V_{DD}	Power Supply	
15	GND	Ground	
16	NC	No Connection	
17	XTAL1	1-MHz Clock	Input
18	ADCLK	Address Clock	Input

PIN DESCRIPTION (Continued)

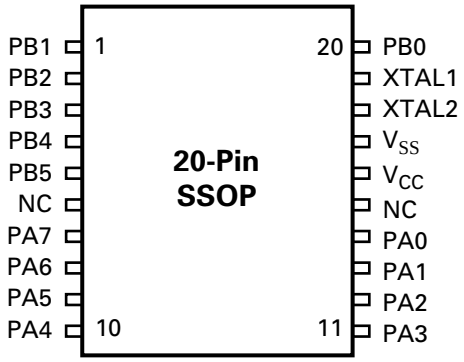


Figure 5. 20-Pin SSOP Pin Identification

Table 3. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	Input/Output

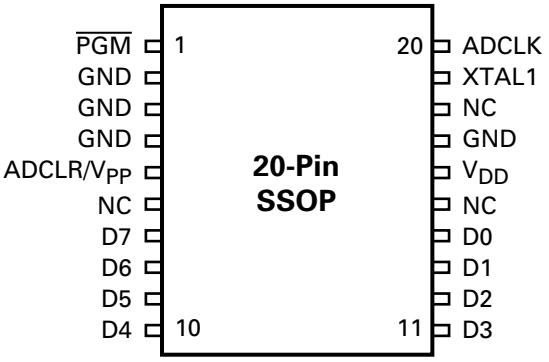


Figure 6. 20-Pin SSOP Pin Identification/EPROM Programming Mode

Table 4. EPROM Programming Mode

Pin #	Symbol	Function	Direction
1	$\overline{PGM}$	Program Mode	Input
2–4	GND	Ground	
5	ADCLR/V_{PP}	Clear Clock/Program Voltage	Input
6	NC	No Connection	
7–10	D7–D4	Data 7,6,5,4	Input/Output
11–14	D3–D0	Data 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{DD}	Power Supply	
17	GND	Ground	
18	NC	No Connection	
19	XTAL1	1-MHz Clock	Input
20	ADCLK	Address Clock	Input

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on PB5 Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		40	mA	3
Maximum Allowable Current into V_{DD}		40	mA	3
Maximum Allowable Current into an Input Pin	–600	+600	µA	4
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	5
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	3
Maximum Allowable Output Current Sourced by Port A		40	mA	3
Maximum Allowable Output Current Sunk by Port B		40	mA	3
Maximum Allowable Output Current Sourced by Port B		40	mA	3

Notes:
1. Applies to all pins except the PB5 pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Peak Current. Do not exceed 25mA average current in either direction.
4. Excludes XTAL pins.
5. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 6. DC Electrical Characteristics

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	V_{CC} –1.5V		V		3
		5.5V	0	V_{CC} –1.5V		V		3
R_{PB5}	PB5 Pull-up Resistor	4.5V	100		200	kOhm		4
		5.5V	100		200			
V_{LV}	V_{CC} Low-Voltage Protection		2.45	2.85	2.60	V		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	5,6
		5.5V		7.0	4.0	mA	@ 10 MHz	5,6

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Table 6. DC Electrical Characteristics (Continued)

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7
		5.5V		700	250	nA	STOP mode V_{IN} = 0V,V_{CC}	7

Notes:
1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

AC ELECTRICAL CHARACTERISTICS

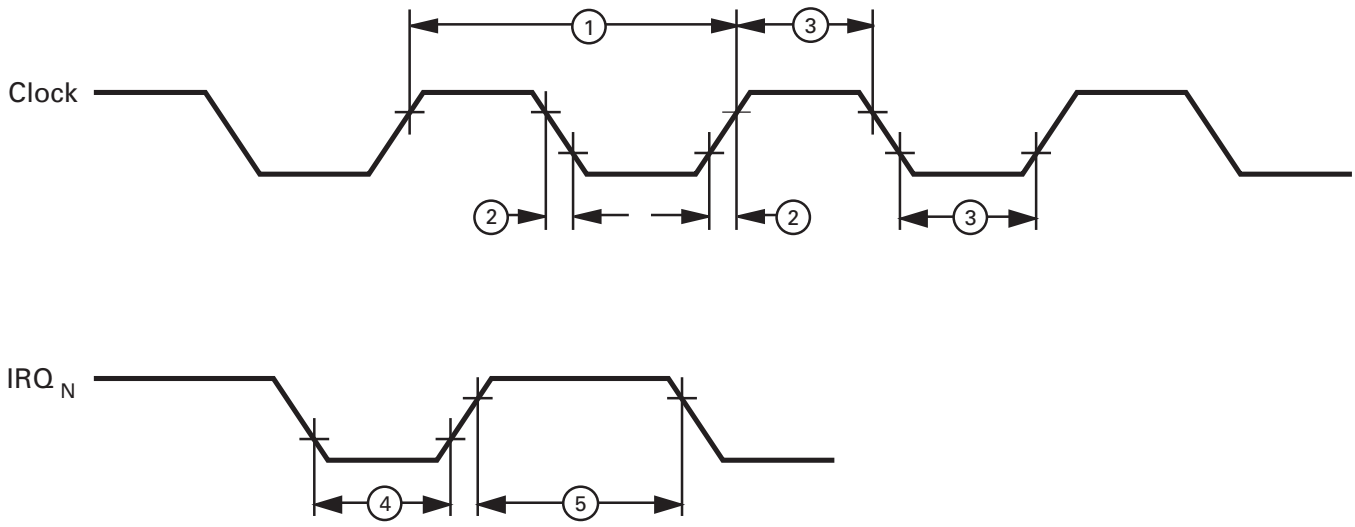


Figure 8. AC Electrical Timing Diagram

Table 7. Additional Timing

				T_A = 0°C to +70°C T_A = –40°C to +105°C @ 10 MHz			
No	**Symbol**	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Units**	**Notes**
1	T_PC	Input Clock Period	3.0V	100	DC	ns	2
			5.5V	100	DC	ns	2
2	T_RC,T_FC	Clock Input Rise and Fall Times	3.0V		15	ns	2
			5.5V		15	ns	2
3	T_WC	Input Clock Width	3.0V	50		ns	2
			5.5V	50		ns	2
4	T_WIL	Int. Request Input Low Time	3.0V	70		ns	2
			5.5V	70		ns	2
5	T_WIH	Int. Request Input High Time	3.0V	5TpC			2
			5.5V	5TpC			2
6	T_{WSM}	STOP mode Recovery Width Spec.	3.0V	25		ns	
			5.5V	25		ns	
7	T_{OST}	Oscillator Start-Up Time	3.0V		5TpC		
			5.5V		5TpC		
8	T_{POR}	Power-On Reset Time	3.0V	128 T_PC + T_{OST}			
			5.5V				

Notes:
1. The V_{DD} voltage specification of 3.0V guarantees 3.0V. The V_{DD} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Timing Reference uses 0.7 V_{CC} for a logical 1 and 0.2 V_{CC} for a logical 0.

CLOCK

The Z8Plus MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, and a divide-by-two shaping circuit. Figure 12 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

By selecting the RC OSCILLATOR option in the graphical user interface (GUI), the circuit may instead be driven by an external Resistor and Capacitor (RC) oscillator. Figure 13 illustrates this configuration. This design is limited to no more than 4 MHz to restrict EMI noise.

Note: The reduced drive strength of this configuration also allows the clock circuit to use a micropower-type crystal (also known as a tuning fork) without reduction resistors.

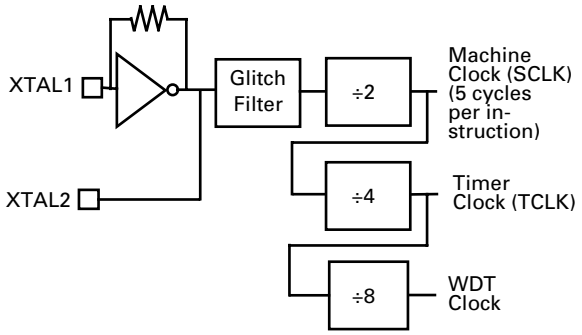


Figure 12. Clock Circuit

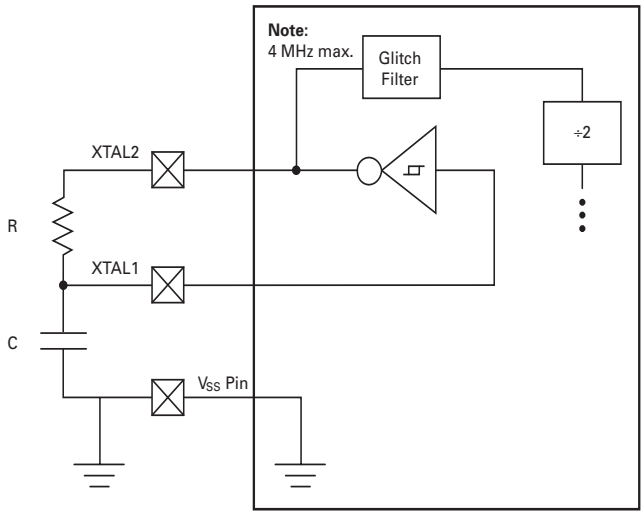


Figure 13. Z8Plus in RC Oscillator Mode

LC OSCILLATOR

The Z8Plus oscillator can use an inductor capacitor oscillator (LC) network to generate an XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$1/C_T = 1/C_1 + 1/C_2$$
$$\text{If } C_1 = C_2$$
$$1/C_T = 2/C_1$$
$$C_1 = 2C_T$$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 µH is displayed as follows:

$$5.83\ (10\text{^}6) = \frac{1}{2\pi [27\ (10^{-6})\ C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pF}$$

Thus, C_1 = 55.2 pF and C_2 = 55.2 pF.

TIMERS

Two 8-bit timers, timer 0 (T0) and timer 1 (T1) are available to function as a pair of independent 8-bit standard timers. They may also be cascaded to function as a 16-bit Pulse-Width Modulator (PWM) timer. Two additional 8-bit timers (T2 and T3) are provided, but they can only operate as one 16-bit standard timer.

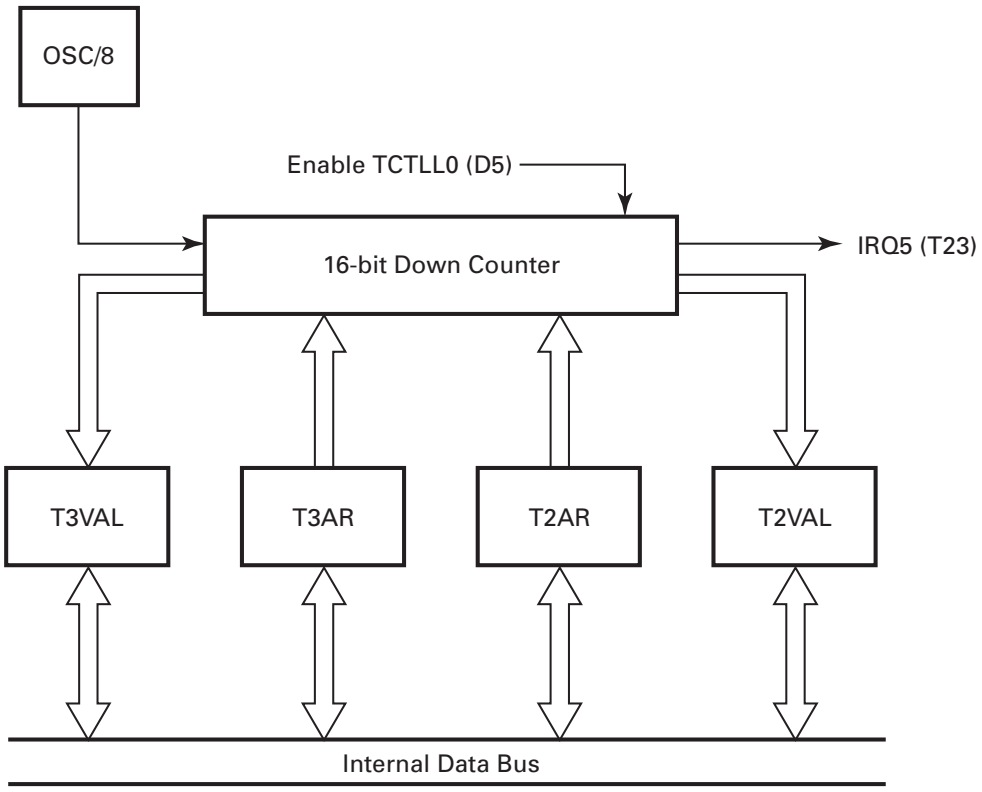
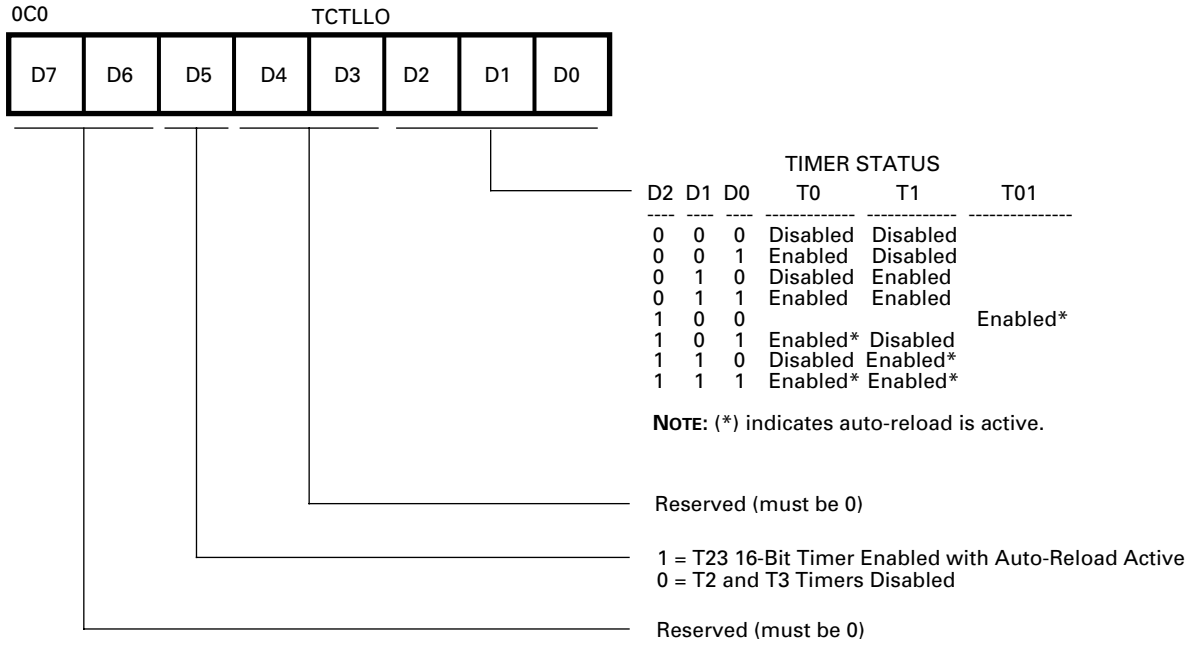


Figure 19. 16-Bit Standard Timer

TIMERS (Continued)



Note: Timer T01 is a 16-bit PWM Timer formed by cascading 8-bit timers T1 (MSB) and T0 (LSB). T23 is a standard 16-bit timer formed by cascading 8-bit timers T3 (MSB) and T2 (LSB).

Figure 22. TCTLLO Register

A pair of READ/WRITE registers is utilized for each 8-bit timer. One register is defined to contain the auto-initialization value for the timer. The second register contains the current value for the timer. When a timer is enabled, the timer decrements the value in its count register and continues decrementing until it reaches 0. An interrupt is generated, and the contents of the auto-initialization register are optionally copied into the count value register. If auto-initialization is not enabled, the timer stops counting when the value reaches 0. Control logic clears the appropriate control register bit to disable the timer. This operation is referred to as a *single-shot*. If auto-initialization is enabled, the timer counts from the initialization value. Software must not attempt to use timer registers for any other function.

User software is allowed to write to any WRITE register at any time; however, care should be taken if timer registers are updated while the timer is enabled. If software changes the count value while the timer is in operation, the timer continues counting from the updated value.

Note: Unpredictable behavior can occur if the value updates at the same time that the timer reaches 0.

Similarly, if user software changes the initialization value register while the timer is active, the next time that the timer reaches 0, the timer initializes to the changed value.

Note: Unpredictable behavior can occur if the initialization value register is changed while the timer is in the process of being initialized.

The initialization value is determined by the exact timing of the WRITE operation. In all cases, the Z8Plus assigns a higher priority to the software WRITE than to a decrementer write-back. However, when hardware clears a control register bit for a timer that is configured for single-shot operation, the clearing of the control bit overrides a software WRITE. A READ of either register can be conducted at any time, with no effect on the functionality of the timer.

PORT B—PIN 0 CONFIGURATION

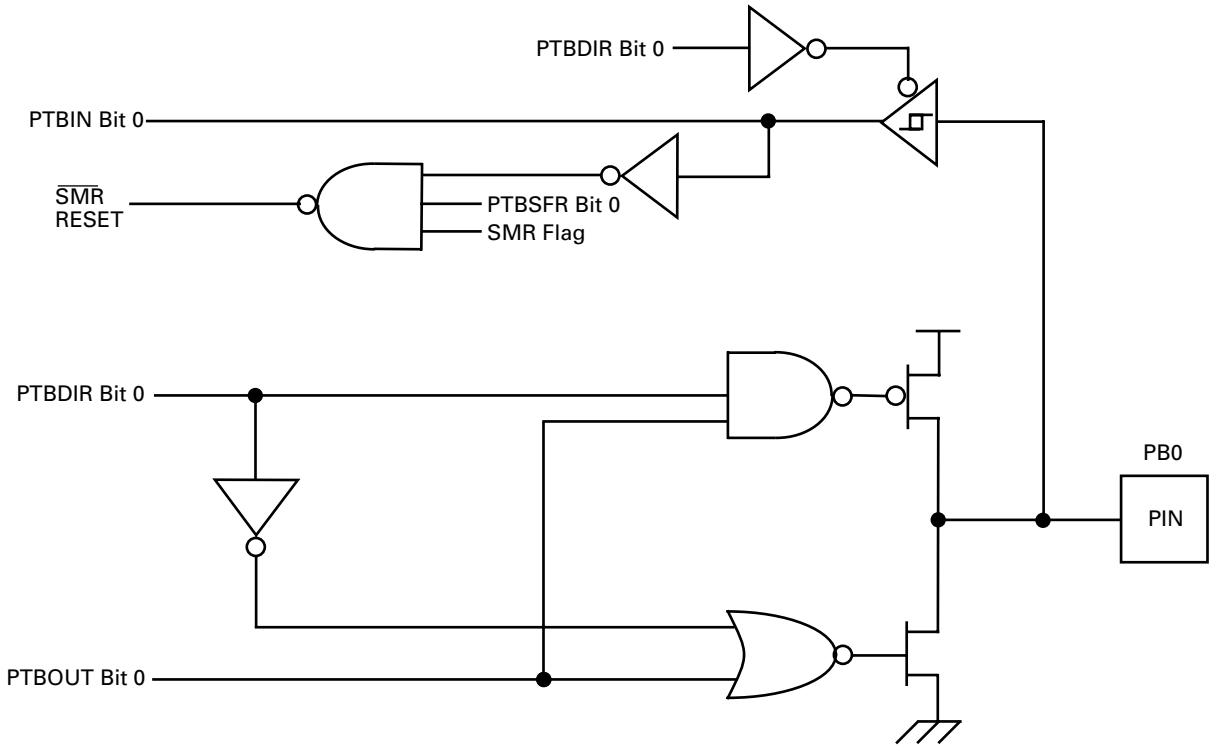
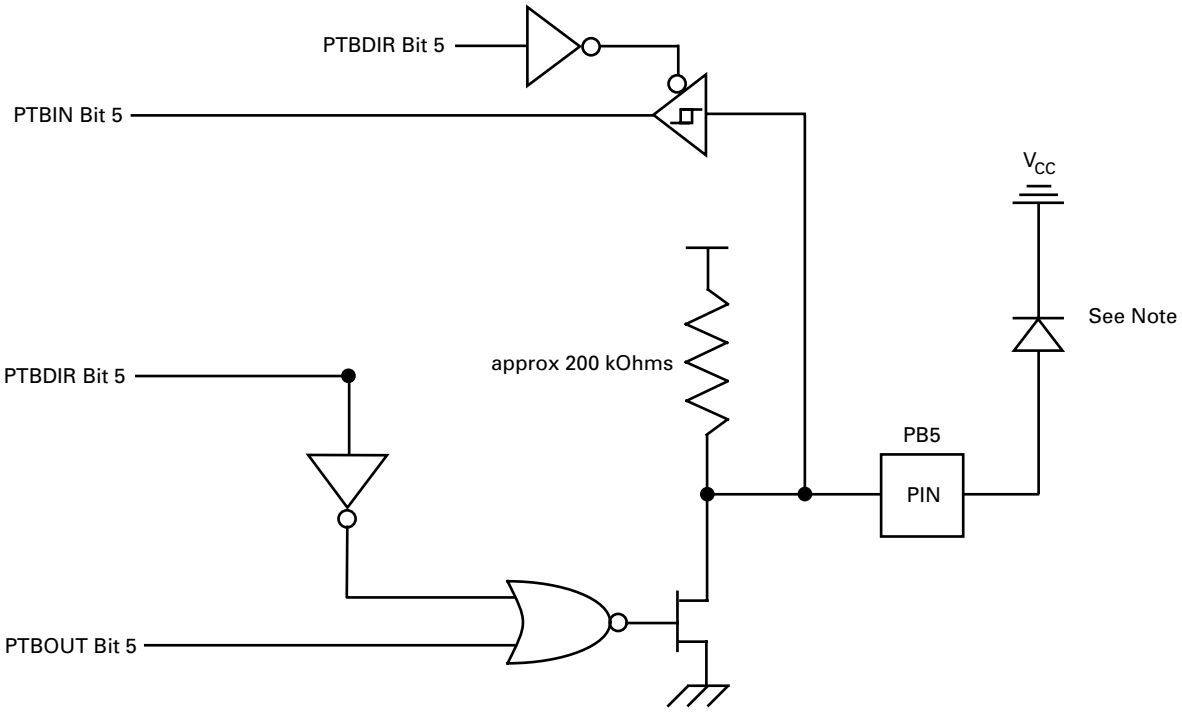


Figure 33. Port B Pin 0 Diagram



Note: There is no high-side protection device. The user should always place an external protection diode as shown.

Figure 34. Port B Pin 5 Diagram

PORT B—PIN 1 CONFIGURATION

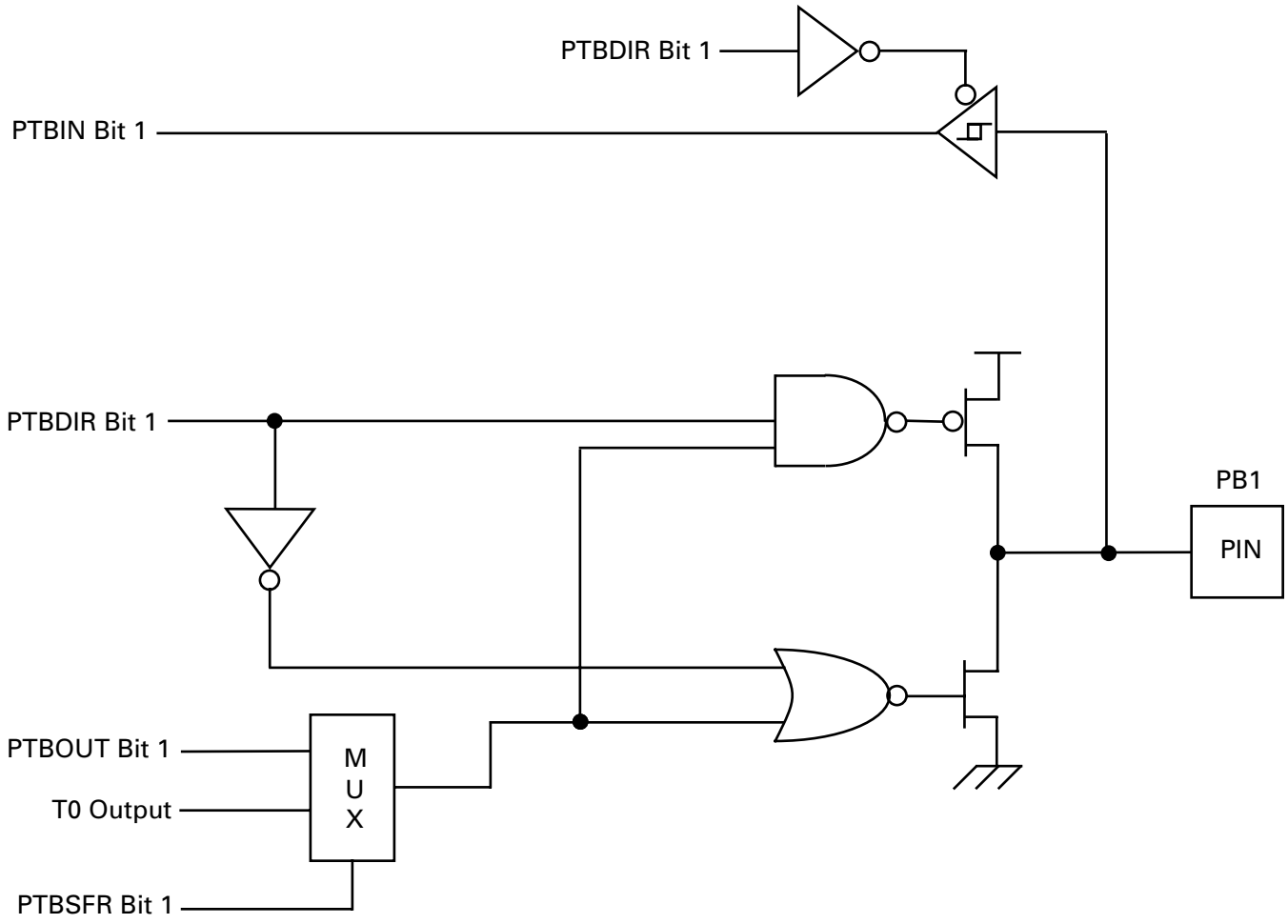


Figure 35. Port B Pin 1 Diagram

PORT B CONTROL REGISTERS

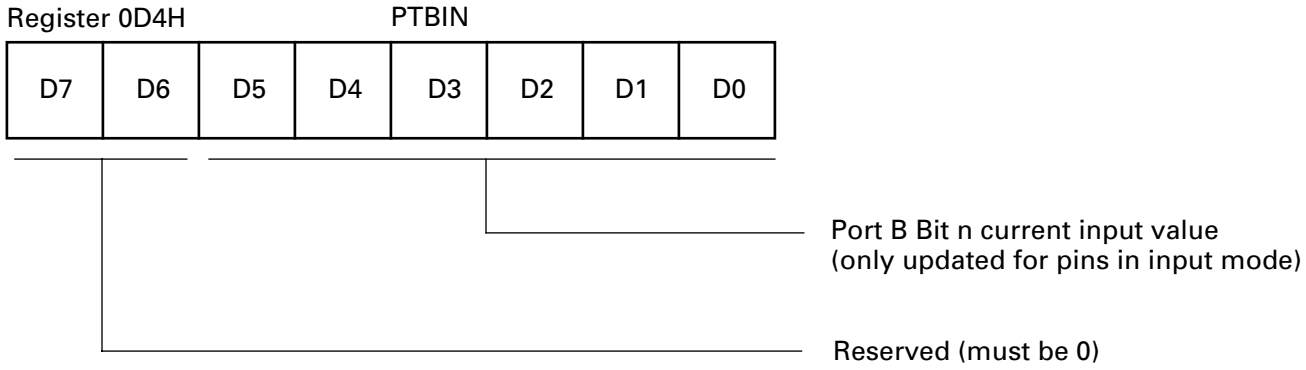


Figure 38. Port B Input Value Register

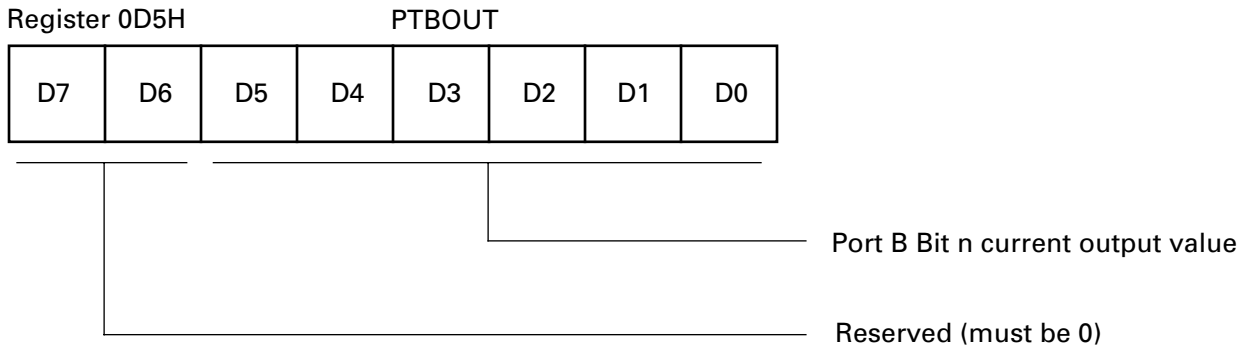


Figure 39. Port B Output Value Register

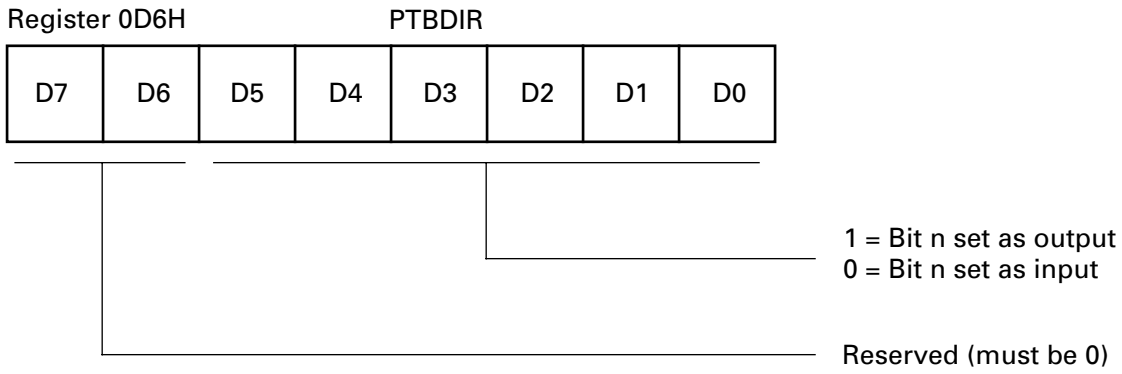


Figure 40. Port B Directional Control Register

I/O PORT RESET CONDITIONS

Full Reset

Port A and Port B output value registers are not affected by $\overline{\text{RESET}}$.

On $\overline{\text{RESET}}$, the Port A and Port B directional control registers are cleared to all zeros, which defines all pins in both ports as inputs.

On $\overline{\text{RESET}}$, the directional control registers redefine all pins as inputs, and the Port A and Port B input value registers overwrites the previously held data with the current sample of the input pins.

On $\overline{\text{RESET}}$, the Port A and Port B special function registers are cleared to 00h, which deactivates all port special functions.

Note: The SMR and WDT time-out events are *not* full device resets. The port control registers are not affected by either of these events.

ANALOG COMPARATOR

The device includes one on-chip analog comparator. Pin PB4 features a comparator front end. The comparator reference voltage is on pin PB3.

Comparator Description

The on-chip comparator can process an analog signal on PB4 with reference to the voltage on PB3. The analog function is enabled by programming the Port B special function register bits 3 and 4.

When the analog comparator function is enabled, bit 4 of the input register is defined as holding the synchronized output of the comparator, while bit 3 retains a synchronized sample of the reference input.

If the interrupts for PB4 are enabled when the comparator special function is selected, the output of the comparator generates interrupts.

COMPARATOR OPERATION

The comparator output reflects the relationship between the analog input to the reference input. If the voltage on the analog input is higher than the voltage on the reference input, then the comparator output is at a High state. If the voltage on the analog input is lower than the voltage on the reference input, then the analog output is at a Low state.

Comparator Definitions

V_{ICR}

The usable voltage range for the positive input and reference input is called the Comparator Input Common Mode Voltage Range (V_{ICR}).

Note: The comparator is not guaranteed to work if the input is outside of the V_{ICR} range.

V_{OFFSET}

The absolute value of the voltage between the positive input and the reference input required to make the comparator output voltage switch is the Comparator Input Offset Voltage (V_{OFFSET}).

I_{IO}

For the CMOS voltage comparator input, the input offset current (I_{IO}) is the leakage current of the CMOS input gate.

HALT Mode

The analog comparator is functional during HALT mode. If the interrupts are enabled, an interrupt generated by the comparator causes a return from HALT mode.

STOP Mode

The analog comparator is disabled during STOP mode. The comparator is powered down to prevent it from drawing any current.

Low Voltage Protection. An on-board Voltage Comparator checks that the V_{CC} is at the required level to ensure correct operation of the device. A reset is globally driven if V_{CC} is below the specified voltage (Low Voltage Protection).

The device functions normally at or above 3.0V under all conditions, and is guaranteed to function normally at supply voltages above the Low Voltage Protection trip point. Below 3.0V, the device functions normally until the Low Volt-

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

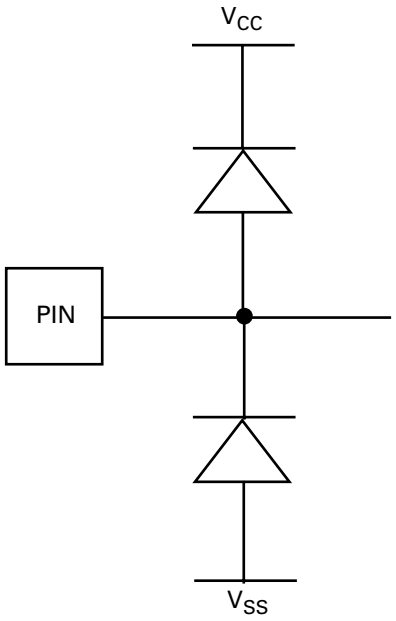


Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

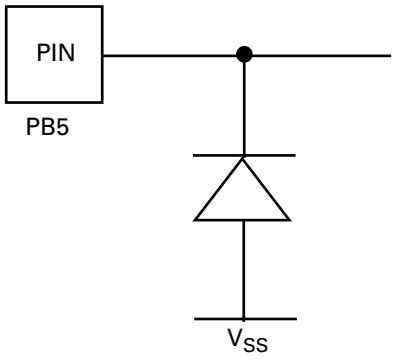
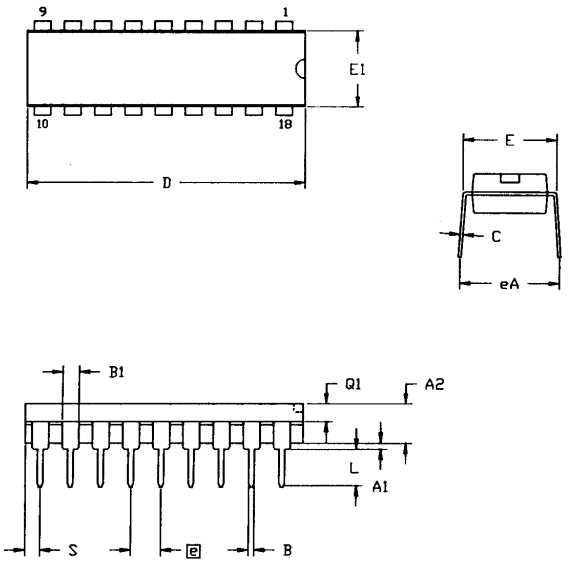


Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

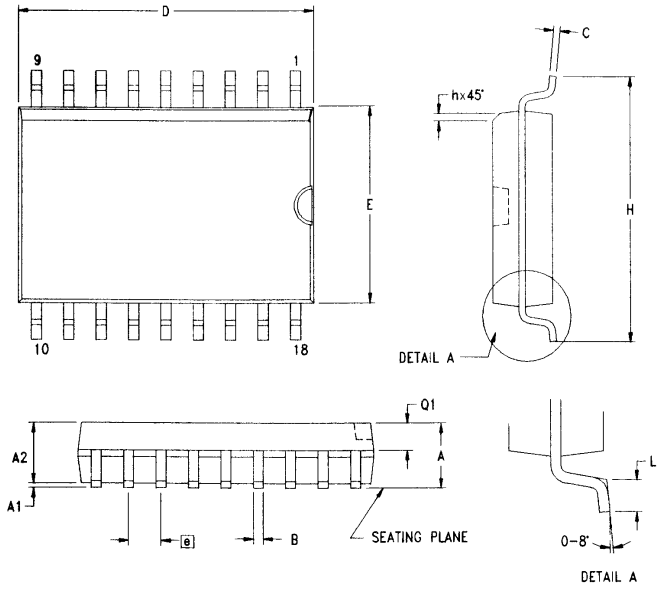
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

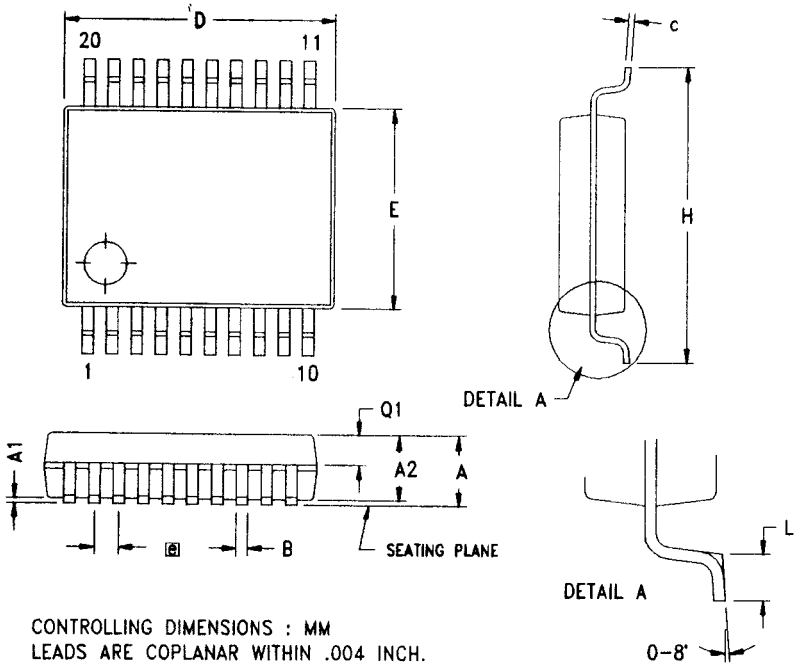
Figure 45. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 46. 18-Pin SOIC Package Diagram



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram