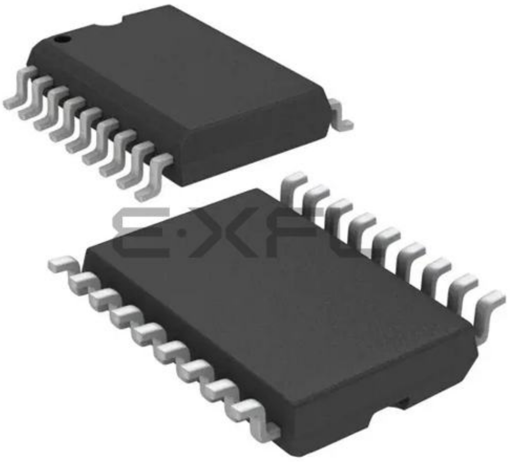


Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe003sz010sc00tr

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an $\overline{\text{overline}}$ are active Low. For example, B/$\overline{\text{W}}$, in which WORD is active Low; and $\overline{\text{B}}$/W, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

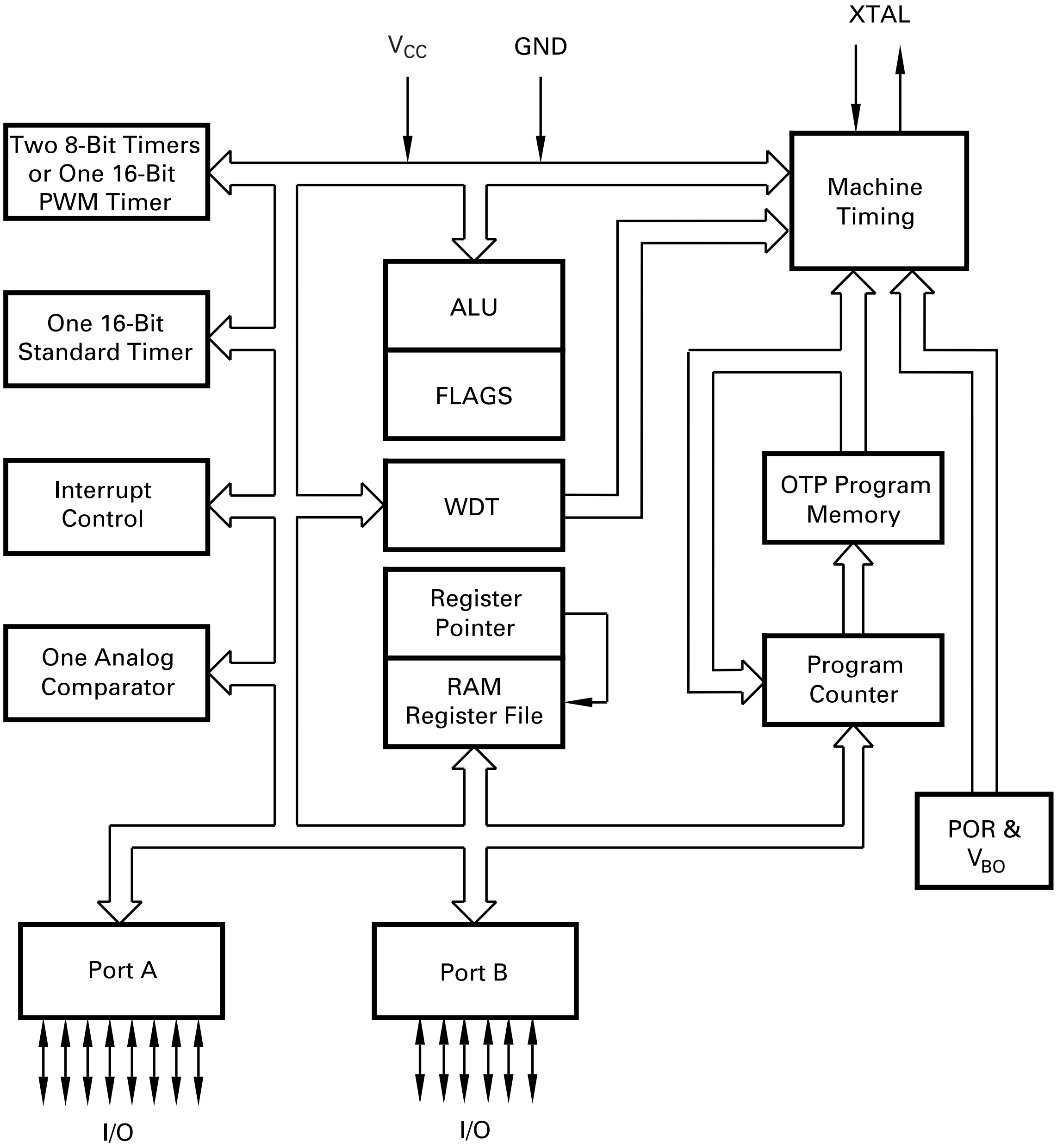


Figure 1. Functional Block Diagram

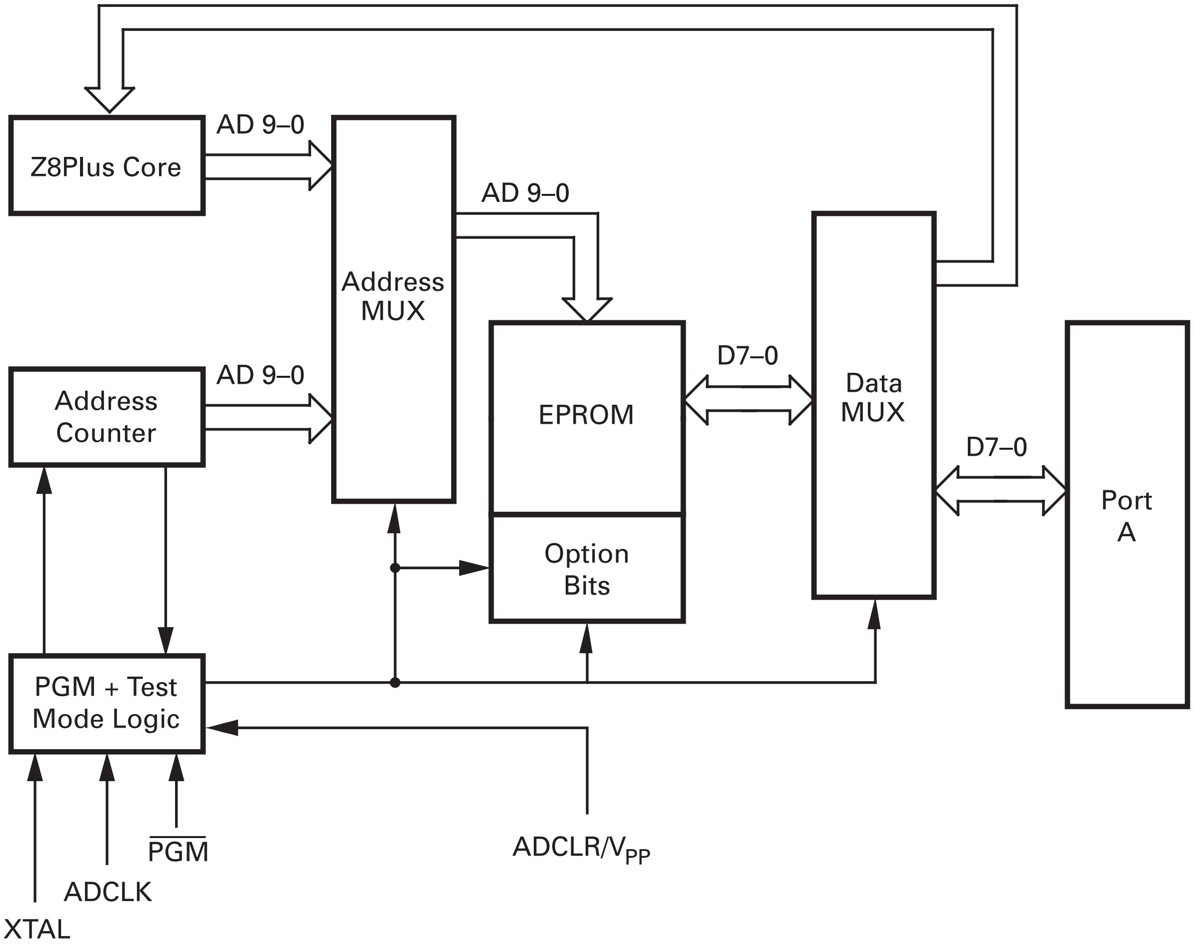


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION (Continued)

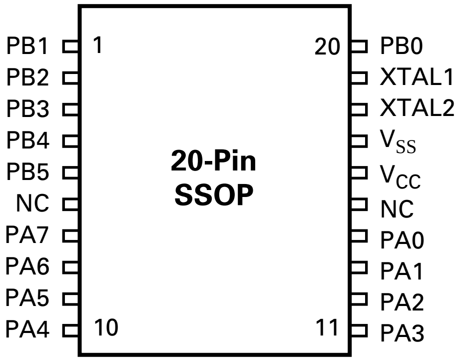


Figure 5. 20-Pin SSOP Pin Identification

Table 3. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6	NC	No Connection	
7–10	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
11–14	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
15	NC	No Connection	
16	V_{CC}	Power Supply	
17	V_{SS}	Ground	
18	XTAL2	Crystal Oscillator Clock	Output
19	XTAL1	Crystal Oscillator Clock	Input
20	PB0	Port B, Pin 0	Input/Output

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units	Note
Ambient Temperature under Bias	–40	+105	C	
Storage Temperature	–65	+150	C	
Voltage on any Pin with Respect to V_{SS}	–0.6	+7	V	1
Voltage on V_{DD} Pin with Respect to V_{SS}	–0.3	+7	V	
Voltage on PB5 Pin with Respect to V_{SS}	–0.6	V_{DD}+1	V	2
Total Power Dissipation		880	mW	
Maximum Allowable Current out of V_{SS}		40	mA	3
Maximum Allowable Current into V_{DD}		40	mA	3
Maximum Allowable Current into an Input Pin	–600	+600	µA	4
Maximum Allowable Current into an Open-Drain Pin	–600	+600	µA	5
Maximum Allowable Output Current Sunk by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sourced by Any I/O Pin		25	mA	
Maximum Allowable Output Current Sunk by Port A		40	mA	3
Maximum Allowable Output Current Sourced by Port A		40	mA	3
Maximum Allowable Output Current Sunk by Port B		40	mA	3
Maximum Allowable Output Current Sourced by Port B		40	mA	3

Notes:

1. Applies to all pins except the PB5 pin and where otherwise noted.
2. There is no input protection diode from pin to V_{DD}.
3. Peak Current. Do not exceed 25mA average current in either direction.
4. Excludes XTAL pins.
5. Device pin is not at an output Low state.

Stresses greater than those listed under Absolute Maximum Ratings can cause permanent damage to the device. This rating is a stress rating only. Functional operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period can affect device reliability. Total power dissipation should not exceed 880 mW for the package. Power dissipation is calculated as follows:

$$\text{Total Power Dissipation} = V_{DD} \times [I_{DD} - (\text{sum of } I_{OH})] + \text{sum of } [(V_{DD} - V_{OH}) \times I_{OH}] + \text{sum of } (V_{OL} \times I_{OL})$$

Table 5. DC Electrical Characteristics (Continued)

			T_A = 0°C to +70°C Standard Temperatures					
Sym	**Parameter**	V_{CC}[1]	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
I_{CC}	Supply Current	3.0V		2.5	2.0	mA	@ 10 MHz	5,6
		5.5V		6.0	3.5	mA	@ 10 MHz	5,6
I_{CC1}	Standby Current	3.0V		2.0	1.0	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
		5.5V		4.0	2.5	mA	HALT mode V_{IN} = 0V, V_{CC} @ 10 MHz	5,6
I_{CC2}	Standby Current			500	150	nA	STOP mode V_{IN} = 0V, V_{CC}	7

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 6. DC Electrical Characteristics

			T_A = –40°C to +105°C Extended Temperatures					
Sym	**Parameter**	**V_{CC}[1]**	**Min**	**Max**	**Typical[2] @ 25°C**	**Units**	**Conditions**	**Notes**
V_{CH}	Clock Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
		5.5V	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} = –2.0 mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I_{OL} = +4.0 mA	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	I_{OL} = +12 mA	
		5.5V		1.2	0.5	V	I_{OL} = +12 mA	
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
		5.5V	–1.0	2.0	<1.0	µA	V_{IN} = 0V, V_{CC}	
V_{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	V_{CC} –1.5V		V		3
		5.5V	0	V_{CC} –1.5V		V		3
R_{PB5}	PB5 Pull-up Resistor	4.5V	100		200	kOhm		4
		5.5V	100		200			
V_{LV}	V_{CC} Low-Voltage Protection		2.45	2.85	2.60	V		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	5,6
		5.5V		7.0	4.0	mA	@ 10 MHz	5,6

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

Note: The WDT can only be disabled via software if the first instruction out of the $\overline{\text{RESET}}$ performs this function. Logic within the device detects that it is in the process of executing the first instruction after the processor leaves $\overline{\text{RESET}}$. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 13 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are `001`, which sets the WDT to its minimum time-out period when coming out of $\overline{\text{RESET}}$.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT mode. A 0 prevents the WDT from resetting the part while halted. Coming out of $\overline{\text{RESET}}$, the WDT is enabled during HALT mode.

STOP MODE (D3). Coming out of $\overline{\text{RESET}}$, the device STOP mode is disabled. If an application requires use of STOP mode, bit D3 must be cleared immediately at leaving $\overline{\text{RESET}}$. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters STOP mode.

Bits 2, 1 and 0. These bits are reserved and must be `0`.

Table 13. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10-MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	8,388,608 TpC	838.86 ms

Note: *TpC is an XTAL clock cycle. The default at reset is 001.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8Plus MCU supports two Power-Down modes to minimize device current consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter HALT mode, the device only requires a HALT instruction. It is *not* necessary to execute a NOP instruction immediately before the HALT instruction.

```
    7F   HALT       ; enter HALT mode
```

HALT mode can be exited by servicing an external or internal interrupt. The first instruction executed is the interrupt service routine. At completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT mode can also be exited via a $\overline{\text{RESET}}$ activation or a Watch-Dog Timer (WDT) time-out. In these cases, program execution restarts at `0020H`, the reset restart address.

OSCILLATOR OPERATION

The Z8Plus MCU uses a Pierce oscillator with an internal feedback resistor (Figure 14). The advantages of this circuit are low-cost, large output signal, low-power level in the crystal, stability with respect to V_{CC} and temperature, and low impedances (not disturbed by stray effects).

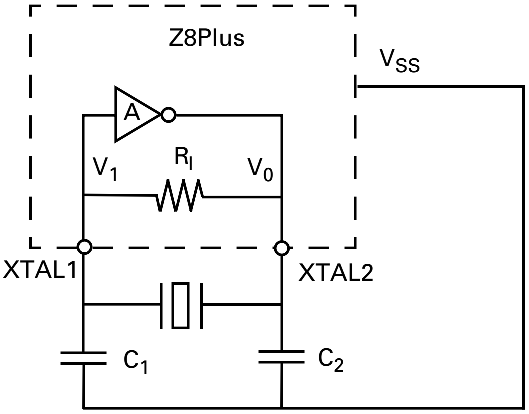


Figure 14. Pierce Oscillator with Internal Feedback Circuit

One drawback to the Pierce oscillator is the requirement for high gain in the amplifier to compensate for feedback path losses. The oscillator amplifies its own noise at start-up until it settles at the frequency that satisfies the gain/phase requirements. A x B = 1; where A = VO/VI is the gain of the amplifier, and B = VI/VO is the gain of the feedback element. The total phase shift around the loop is forced to 0 (360 degrees). V_{IN} must be in phase with itself; therefore, the amplifier/inverter provides a 180-degree phase shift, and the feedback element is forced to provide the other 180-degree phase shift.

R1 is a resistive component placed from output to input of the amplifier. The purpose of this feedback is to bias the amplifier in its linear region and provide the start-up transition.

Capacitor C2, combined with the amplifier output resistance, provides a small phase shift. It also provides some attenuation of overtones.

Capacitor C_1, combined with the crystal resistance, provides an additional phase shift.

Start-up time may be affected if C_1 and C_2 are increased dramatically in size. As C_1 and C_2 increase, the start-up time increases until the oscillator reaches a point where it ceases to operate.

For fast and reliable oscillator start-up over the manufacturing process range, the load capacitors should be sized as low as possible without resulting in overtone operation.

Layout

Traces connecting crystal, caps, and the Z8Plus oscillator pins should be as short and wide as possible to reduce parasitic inductance and resistance. The components (caps, the crystal, and resistors) should be placed as close as possible to the oscillator pins of the Z8Plus.

The traces from the oscillator pins of the integrated circuit (IC) and the ground side of the lead caps should be guarded from all other traces (clock, V_{CC}, address/data lines, and system ground) to reduce cross talk and noise injection. Guarding is usually accomplished by keeping other traces and system ground trace planes away from the oscillator circuit, and by placing a Z8Plus device V_{SS} ground ring around the traces/components. The ground side of the oscillator lead caps should be connected to a single trace to the Z8Plus device V_{SS} (GND) pin. It should not be shared with any other system-ground trace or components except at the Z8Plus device V_{SS} pin. The objective is to prevent differential system ground noise injection into the oscillator (Figure 15).

Indications of an Unreliable Design

There are two major indicators that are used in working designs to determine their reliability over full lot and temperature variations. They are:

Start-Up Time. If start-up time is excessive, or varies widely from unit to unit, there is probably a gain problem. To fix the problem, the C_1 and C_2 capacitors require reduction. The amplifier gain is either not adequate at frequency, or the crystal R's are too large.

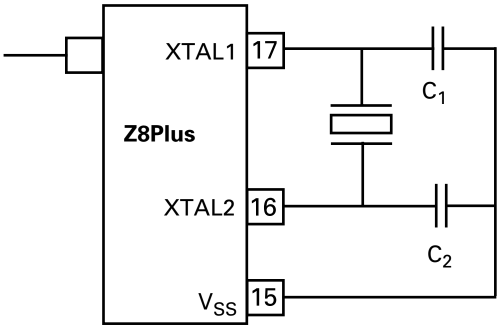
Output Level. The signal at the amplifier output should swing from ground to V_{CC} to indicate adequate gain in the amplifier. As the oscillator starts up, the signal amplitude grows until clipping occurs. At that point, the loop gain is effectively reduced to unity, and constant oscillation is achieved. A signal of less than 2.5 volts peak-to-peak is an indication that low gain can be a problem. Either C_1 or C_2 should be made smaller, or a low-resistance crystal should be used.

OSCILLATOR OPERATION (Continued)

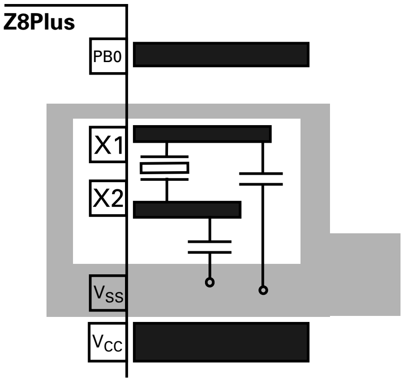
Circuit Board Design Rules

The following circuit board design rules are suggested:

- To prevent induced noise, the crystal and load capacitors should be physically located as close to the Z8Plus as possible.
- Signal lines should not run parallel to the clock oscillator inputs. In particular, the crystal input circuitry and the internal system clock output should be separated as much as possible.
- V_{CC} power lines should be separated from the clock oscillator input circuitry.
- Resistivity between XTAL1 or XTAL2 (and the other pins) should be greater than 10 meg-Ohms.



Clock Generator Circuit



Board Design Example
(Top View)

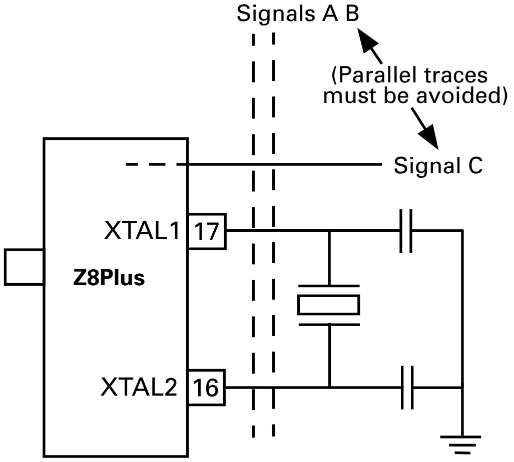


Figure 15. Circuit Board Design Rules

Crystals and Resonators

Crystals and ceramic resonators (Figure 16) should exhibit the following characteristics to ensure proper oscillation:

Crystal Cut	AT (crystal only)
Mode	Parallel, fundamental mode
Crystal Capacitance	<7pF
Load Capacitance	10pF < CL < 220 pF,
	15 typical
Resistance	100 Ohms maximum

Depending on the operation frequency, the oscillator may require additional capacitors, C_1 and C_2, as illustrated in Figure 16 and Figure 17. The capacitance values are dependent on the manufacturer's crystal specifications.

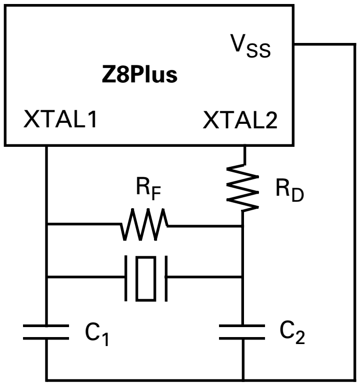


Figure 16. Crystal/Ceramic Resonator Oscillator

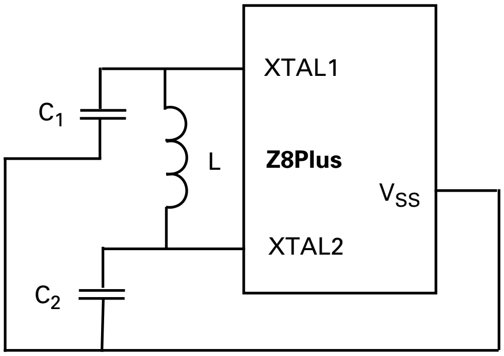


Figure 17. LC Clock

In most cases, the R_D is 0 Ohms and R_F is infinite. These specifications are determined and specified by the crystal/ceramic resonator manufacturer. The R_D can be increased to decrease the amount of drive from the oscillator output to the crystal. It can also be used as an adjustment to avoid clipping of the oscillator signal to reduce noise. The R_F can be used to improve the start-up of the crystal/ceramic resonator. The Z8Plus oscillator already locates an internal shunt resistor in parallel to the crystal/ceramic resonator.

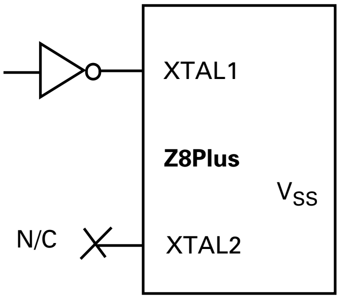


Figure 18. External Clock

Figure 16, Figure 17, and Figure 18 recommend that the load capacitor ground trace connect directly to the V_{SS} (GND) pin of the Z8Plus. This requirement assures that no system noise is injected into the Z8Plus clock. This trace should not be shared with any other components except at the V_{SS} pin of the Z8Plus.

Note: A parallel-resonant crystal or resonator manufacturer specifies a load capacitor value that is a series combination of C_1 and C_2, including all parasitics (PCB and holder).

LC OSCILLATOR

The Z8Plus oscillator can use an inductor capacitor oscillator (LC) network to generate an XTAL clock (Figure 17).

The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi\,(LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics.

Simple series capacitance is calculated using the equation at the top of the next column.

$$\begin{aligned} 1/C_T &= 1/C_1 + 1/C_2 \\ \text{If } C_1 &= C_2 \\ 1/C_T &= 2/C_1 \\ C_1 &= 2C_T \end{aligned}$$

A sample calculation of capacitance C_1 and C_2 for 5.83-MHz frequency and inductance value of 27 µH is displayed as follows:

$$5.83\,(10\text{^}6) = \frac{1}{2\pi\,[27\,(10^{-6})\,C_T]^{1/2}}$$

$$C_T = 27.6\text{ pF}$$

Thus, C_1 = 55.2 pF and C_2 = 55.2 pF.

TIMERS

Two 8-bit timers, timer 0 (T0) and timer 1 (T1) are available to function as a pair of independent 8-bit standard timers. They may also be cascaded to function as a 16-bit Pulse-Width Modulator (PWM) timer. Two additional 8-bit timers (T2 and T3) are provided, but they can only operate as one 16-bit standard timer.

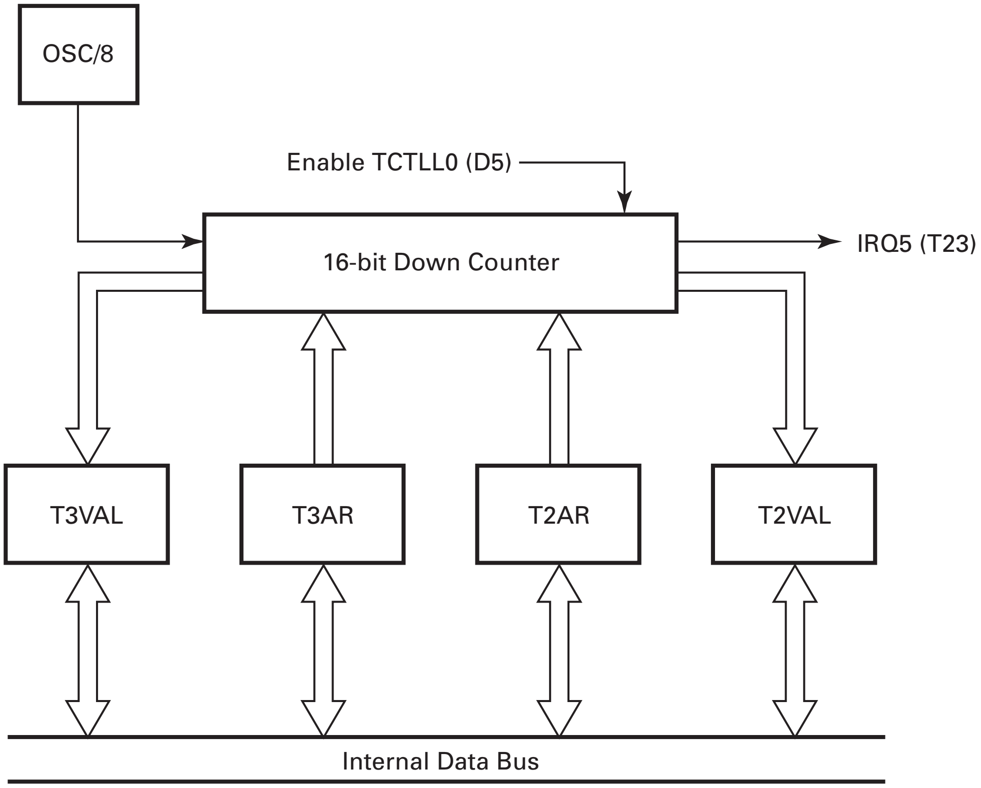


Figure 19. 16-Bit Standard Timer

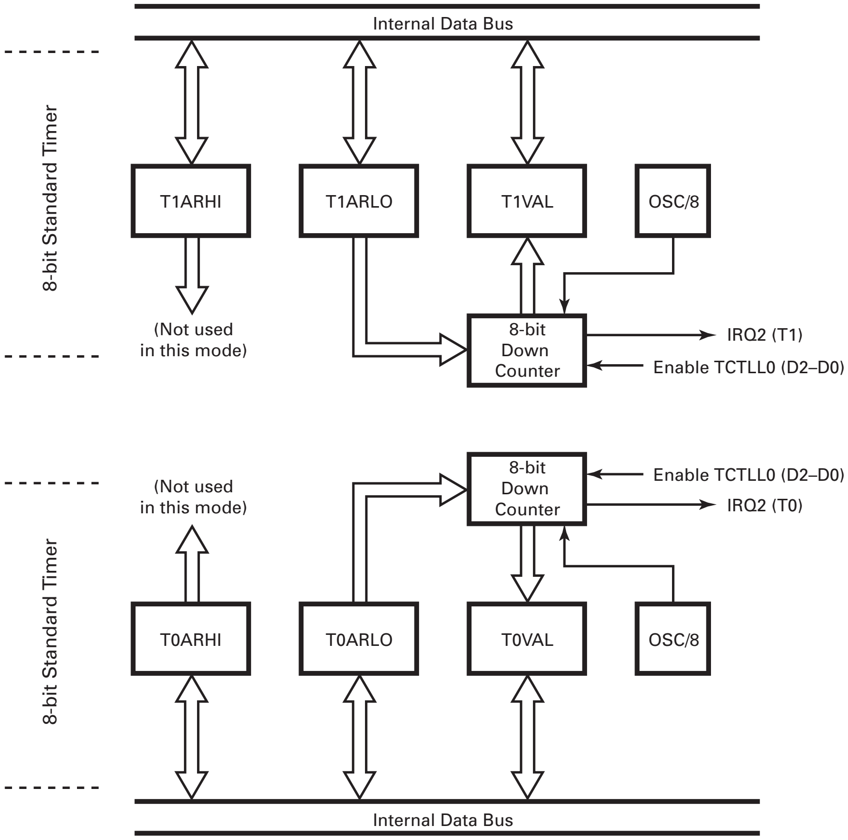


Figure 20. 8-Bit Standard Timers

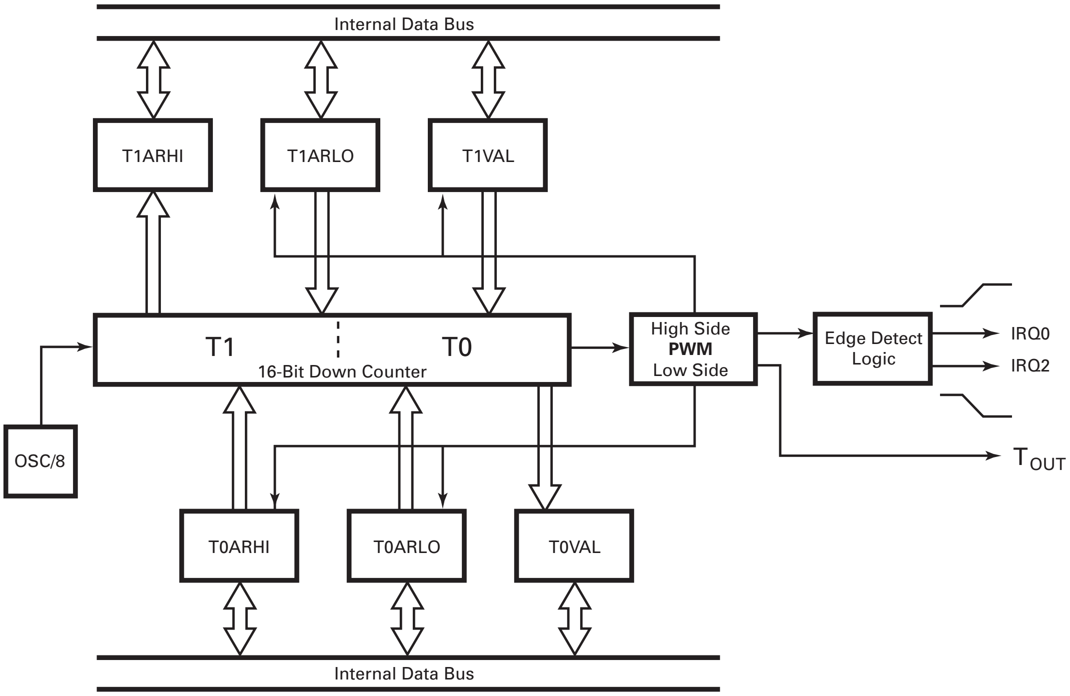


Figure 21. 16-Bit Standard PWM Timer

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16-bit timer. The interrupt for the combined timer is defined to be generated by timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function is performed automatically.

All 16-bit timers continue counting while their interrupt requests are active and operate independently of each other.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt is responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the WRITE begin counting from the value in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source input only. Each enabled timer is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initialization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it alternately initializes its count value using the Low auto-init pair, followed by the High auto-init pair. This functionality corresponds to a PWM. That is, the T1 interrupt defines the end of the High section of the waveform, and the T0 interrupt marks the end of the Low portion of the PWM waveform.

The PWM begins counting with whatever data is held in the count registers. After this value expires, the first reload depends on the state of the PB1 pin if T_{OUT} mode is selected. Otherwise, the Low value is applied first.

After the auto-initialization is completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt IRQ2 is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H; Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6; Figure 24) to configure PB1 for T_{OUT} operation for T0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 is capable of being a clock output for T0, toggling the PB1 output pin on each T0 timeout.

At end-of-count, the interrupt request line (IRQ0), clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when T0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, T0 is in Continuous Counting Mode, T_{OUT} exhibits a 50-percent duty cycle output. If the timer pair is selected (T01) as a PWM, the duty cycle depends on the High and Low reload values. At the end of each High time, PB1 toggles Low. At the end of each Low time, PB1 toggles HI.

RESET CONDITIONS

After a $\overline{\text{RESET}}$, the timers are disabled. See Table 8 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8Plus dedicates 14 lines to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide either standard input/output, or the following special functions: T0 output, comparator input, SMR input, and external interrupt inputs.

All pins except PB5 include push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation.The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers (Figure 26).

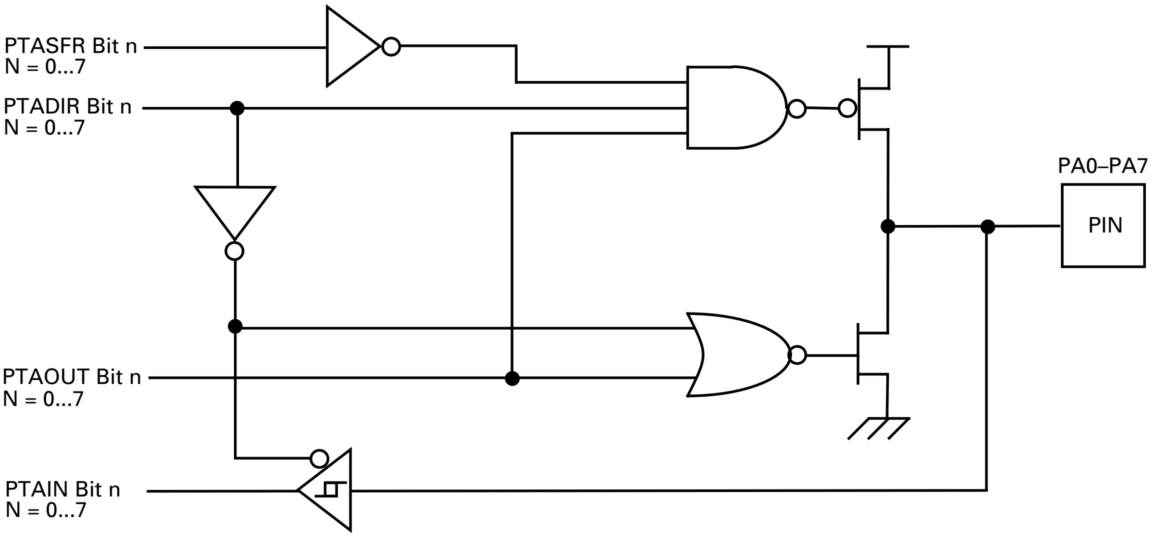


Figure 26. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

Directional Control and Special Function Registers

Each port on the Z8Plus features a dedicated directional control register that determines (on a bit-wise basis) if a given port bit operates as input or output.

Each port on the Z8Plus features a special function register (SFR) that, in conjunction with the directional control register, implements (on a bit-by-bit basis) any special functionality that can be defined for each particular port bit.

Table 14. I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port features an Output Value Register and an input value register. For port bits configured as an input by means of the directional control register, the input value register

PORT B

Port B Description

Port B is a 6-bit (bidirectional), CMOS-compatible I/O port. These six I/O lines can be configured under software control to be an input or output. Each bit is configured independently from the other bits. That is, one bit may be set to INPUT while another bit is set to OUTPUT.

In addition to standard input/output capability, five pins of Port B provide special functionality as indicated in Table 15.

Table 15. Port B Special Functions

Port Pin	Input Special Function	Output Special Function
PB0	Stop Mode Recovery Input	None
PB1	None	T0 Output
PB2	IRQ3	None
PB3	Comparator Reference Input	None
PB4	Comparator Signal Input/IRQ1/IRQ4	None

Special functionality is invoked via the Port B special function register. Port B, bit 5, is an open-drain-only pin when in output mode. There is no high-side driver on the output stage, nor is there any high-side protection device, because PB5 acts as the V_{PP} pin for EPROM programming mode. The user should always place an external protection diode on this pin. See Figure 32.

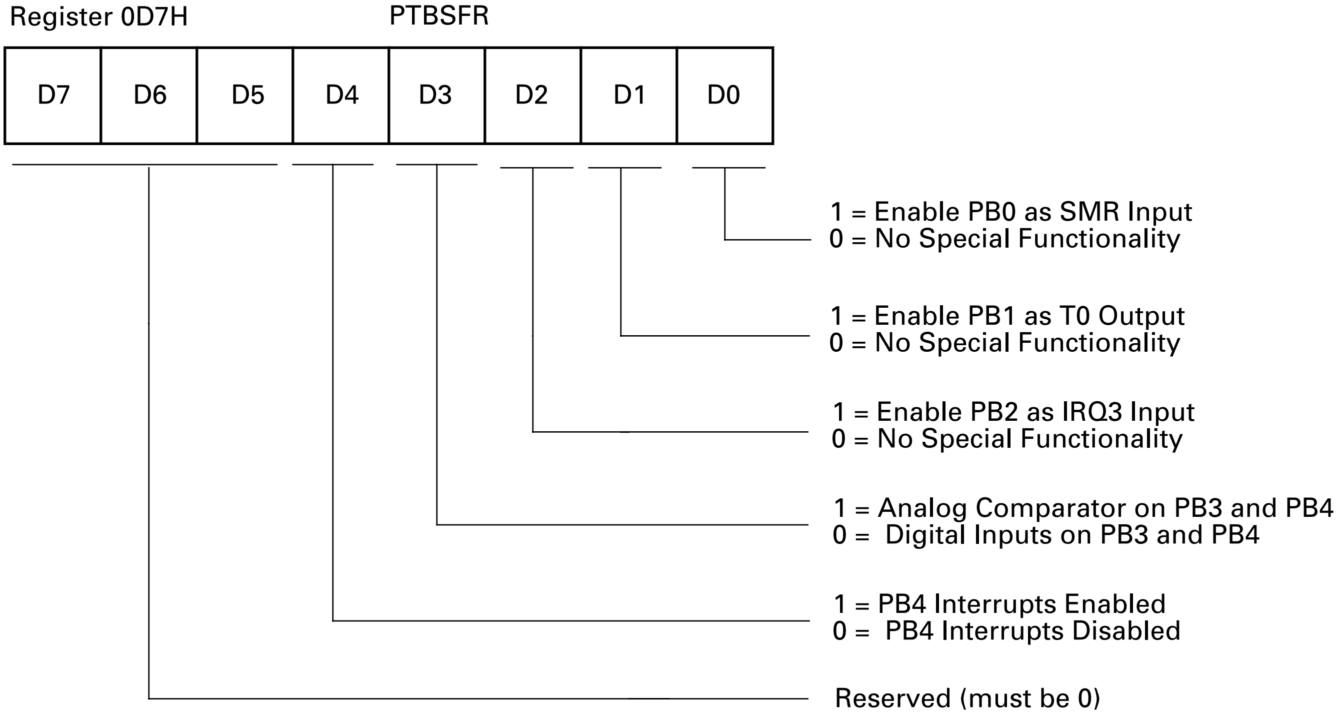


Figure 32. Port B Special Function Register

PORT B—PIN 0 CONFIGURATION

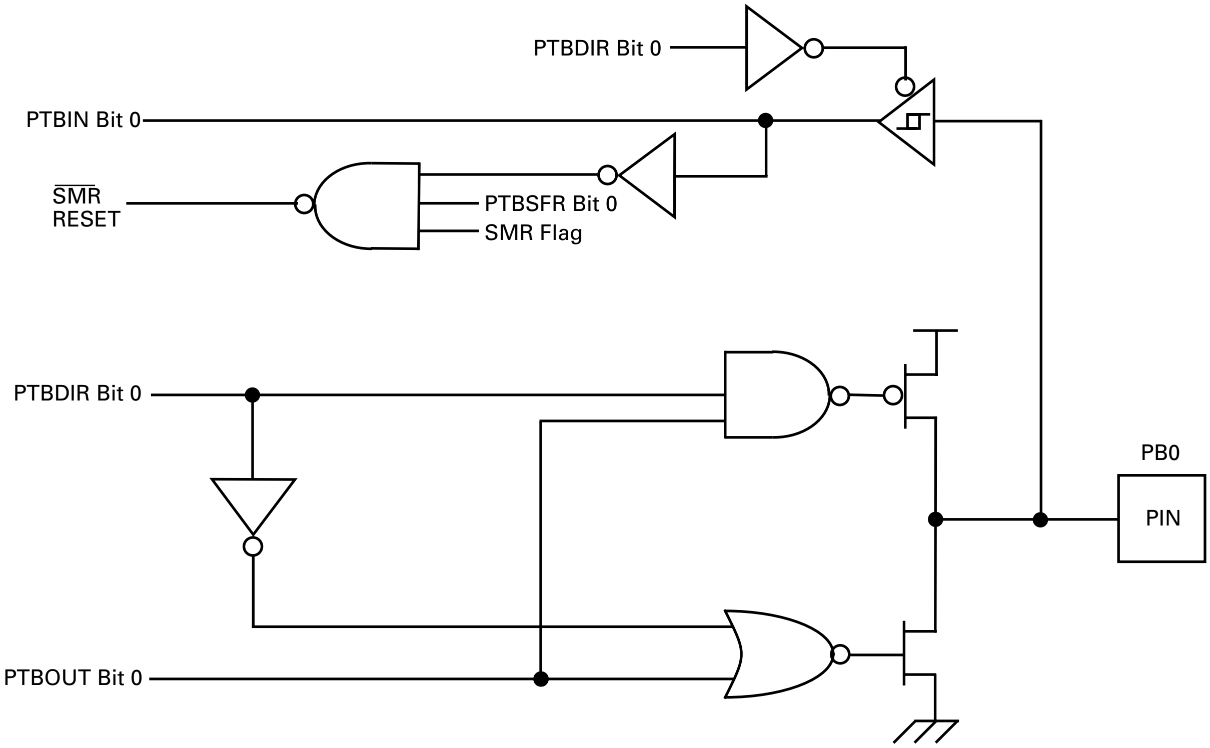
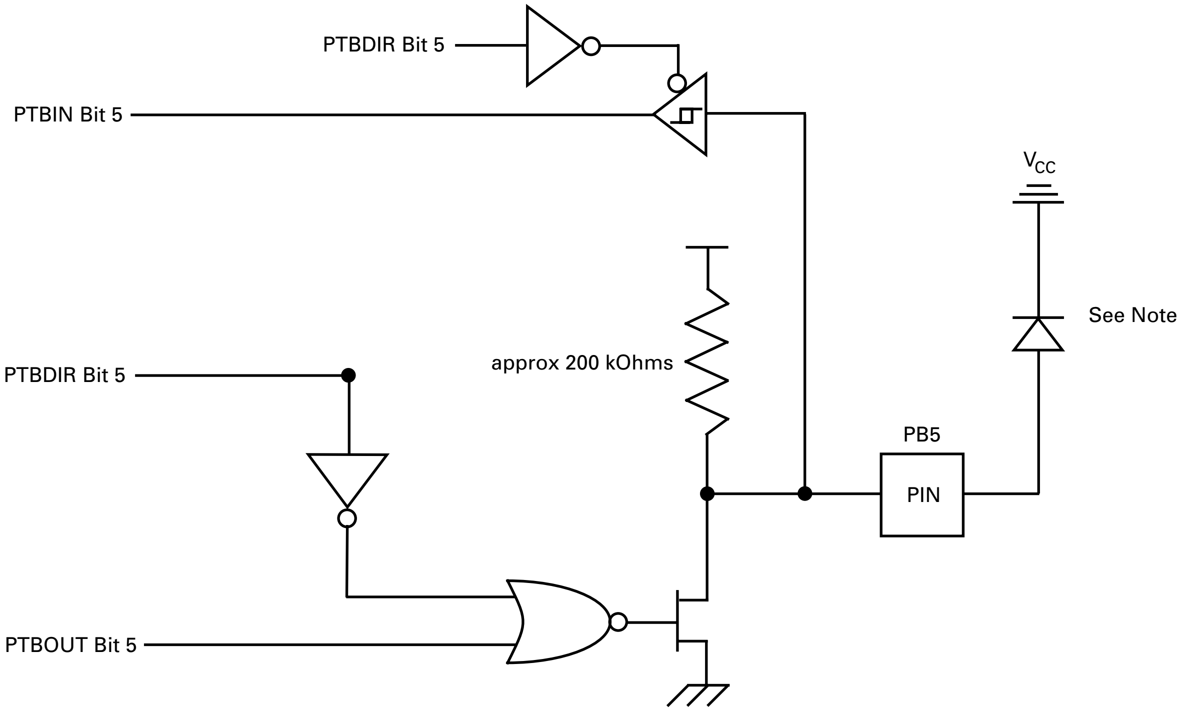


Figure 33. Port B Pin 0 Diagram



Note: There is no high-side protection device. The user should always place an external protection diode as shown.

Figure 34. Port B Pin 5 Diagram

COMPARATOR OPERATION (Continued)

age Protection trip point (V_{LV}) is reached. The actual Low-Voltage Protection trip point is a function of process parameters.

Low-Voltage Protection is active in RUN and HALT modes only, but is disabled in STOP mode (Figure 42).

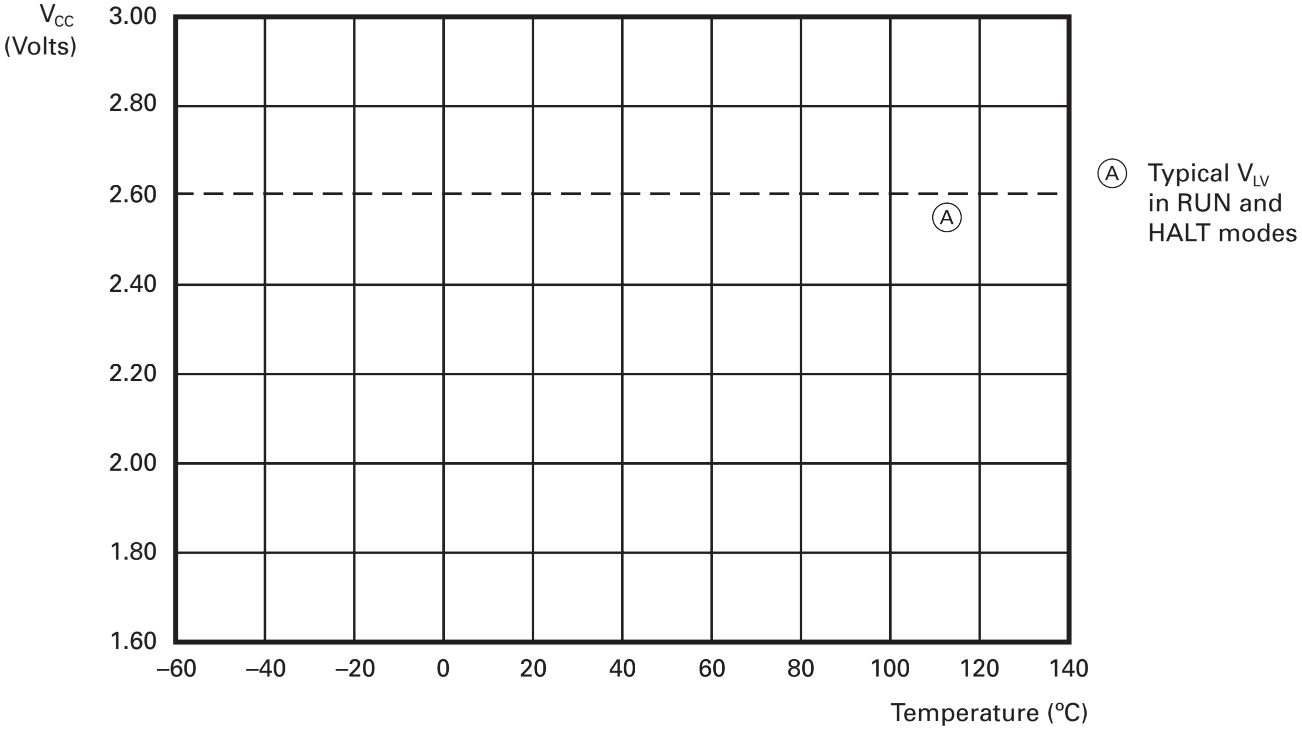


Figure 42. Typical Low Voltage Protection vs. Temperature

INPUT PROTECTION

All I/O pins feature diode input protection. There is a diode from the I/O pad to V_{CC} and V_{SS} (Figure 43).

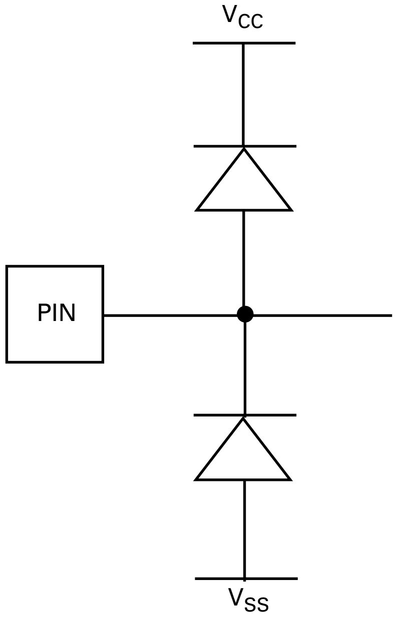


Figure 43. I/O Pin Diode Input Protection

However, the PB5 pin features only the input protection diode, from the pad to V_{SS} (Figure 44).

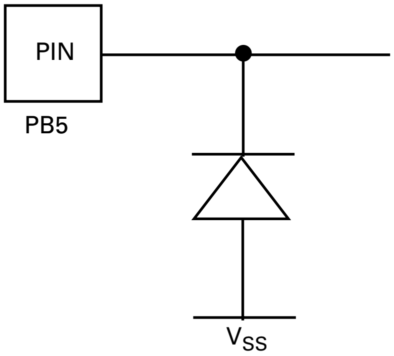
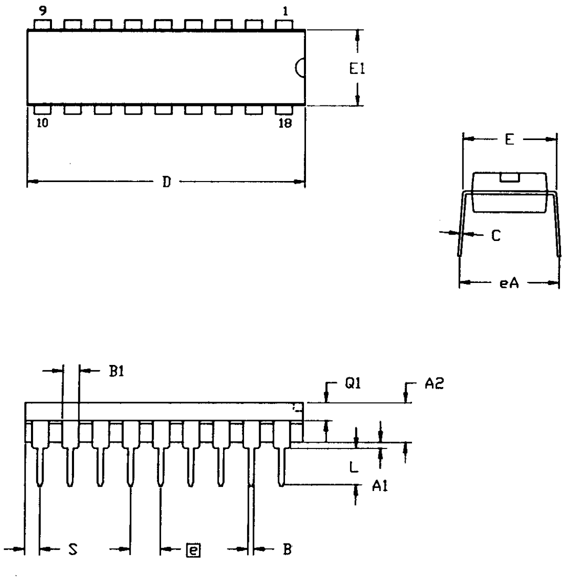


Figure 44. PB5 Pin Input Protection

The high-side input protection diode was removed on this pin to allow the application of high voltage during the OTP programming mode.

For better noise immunity in applications that are exposed to system EMI, a clamping diode to V_{SS} from this pin should be used to prevent entering the OTP programming mode or to prevent high voltage from damaging this pin.

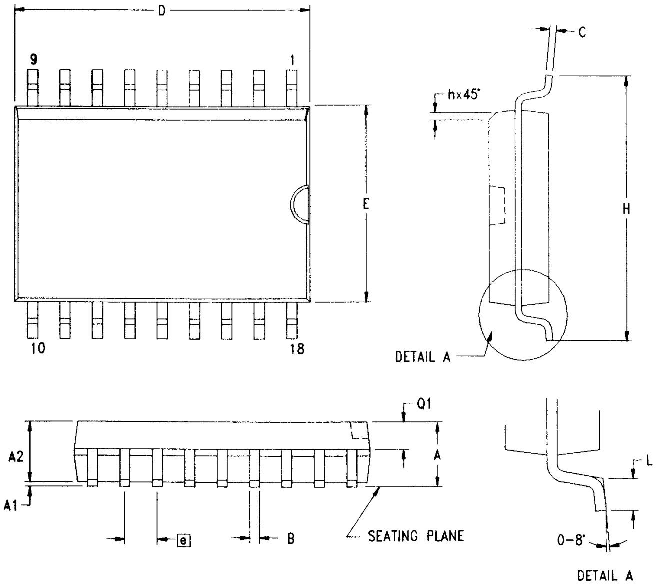
PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.14	1.65	.045	.065
C	0.23	0.38	.009	.015
D	22.35	23.37	.880	.920
E	7.62	8.13	.300	.320
E1	6.22	6.48	.245	.255
e	2.54 TYP		.100 TYP	
eA	7.87	8.89	.310	.350
L	3.18	3.81	.125	.150
Q1	1.52	1.65	.060	.065
S	0.89	1.65	.035	.065

CONTROLLING DIMENSIONS : INCH

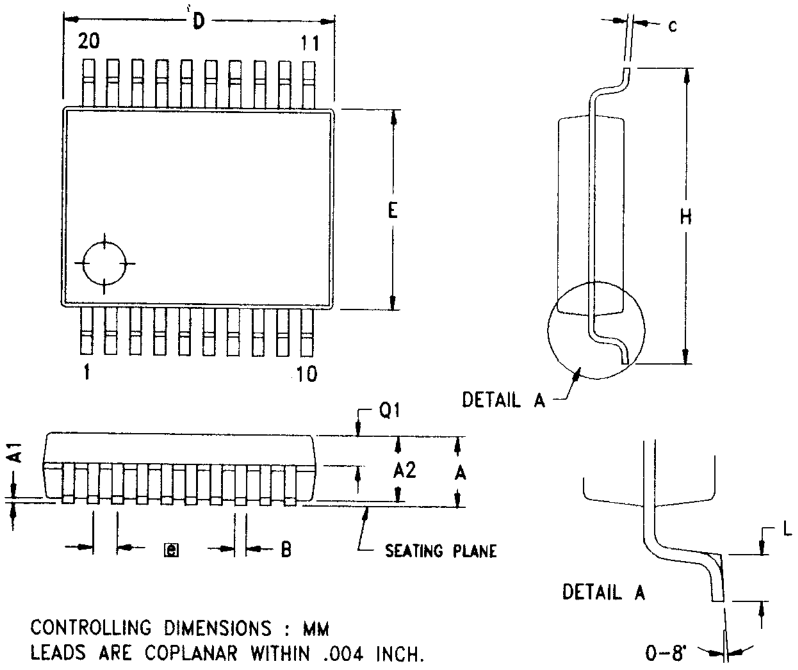
Figure 45. 18-Pin DIP Package Diagram



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.65	0.094	0.104
A1	0.10	0.30	0.004	0.012
A2	2.24	2.44	0.088	0.096
B	0.36	0.46	0.014	0.018
C	0.23	0.30	0.009	0.012
D	11.40	11.75	0.449	0.463
E	7.40	7.60	0.291	0.299
e	1.27 TYP		0.050 TYP	
H	10.00	10.65	0.394	0.419
h	0.30	0.50	0.012	0.020
L	0.60	1.00	0.024	0.039
Q1	0.97	1.07	0.038	0.042

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 46. 18-Pin SOIC Package Diagram



CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.73	1.85	1.98	0.068	0.073	0.078
A1	0.05	0.13	0.21	0.002	0.005	0.008
A2	1.68	1.73	1.83	0.066	0.068	0.072
B	0.25	0.30	0.38	0.010	0.012	0.015
C	0.13	0.15	0.22	0.005	0.006	0.009
D	7.07	7.20	7.33	0.278	0.283	0.289
E	5.20	5.30	5.38	0.205	0.209	0.212
e	0.65 TYP			0.0256 TYP		
H	7.65	7.80	7.90	0.301	0.307	0.311
L	0.56	0.75	0.94	0.022	0.030	0.037
Q1	0.74	0.78	0.82	0.029	0.031	0.032

Figure 47. 20-Pin SSOP Package Diagram