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Details

Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	10MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	14
Program Memory Size	1KB (1K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	18-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8pe003sz010sg

GENERAL DESCRIPTION (Continued)

Both the 8-bit and 16-bit on-chip timers, with several user-selectable modes, administer real-time tasks such as counting/timing and I/O data communications.

Note: All signals with an overline are active Low. For example, $\overline{B/W}$, in which WORD is active Low; and $\overline{B/W}$, in which BYTE is active Low.

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V _{CC}	V _{DD}
Ground	GND	V _{SS}

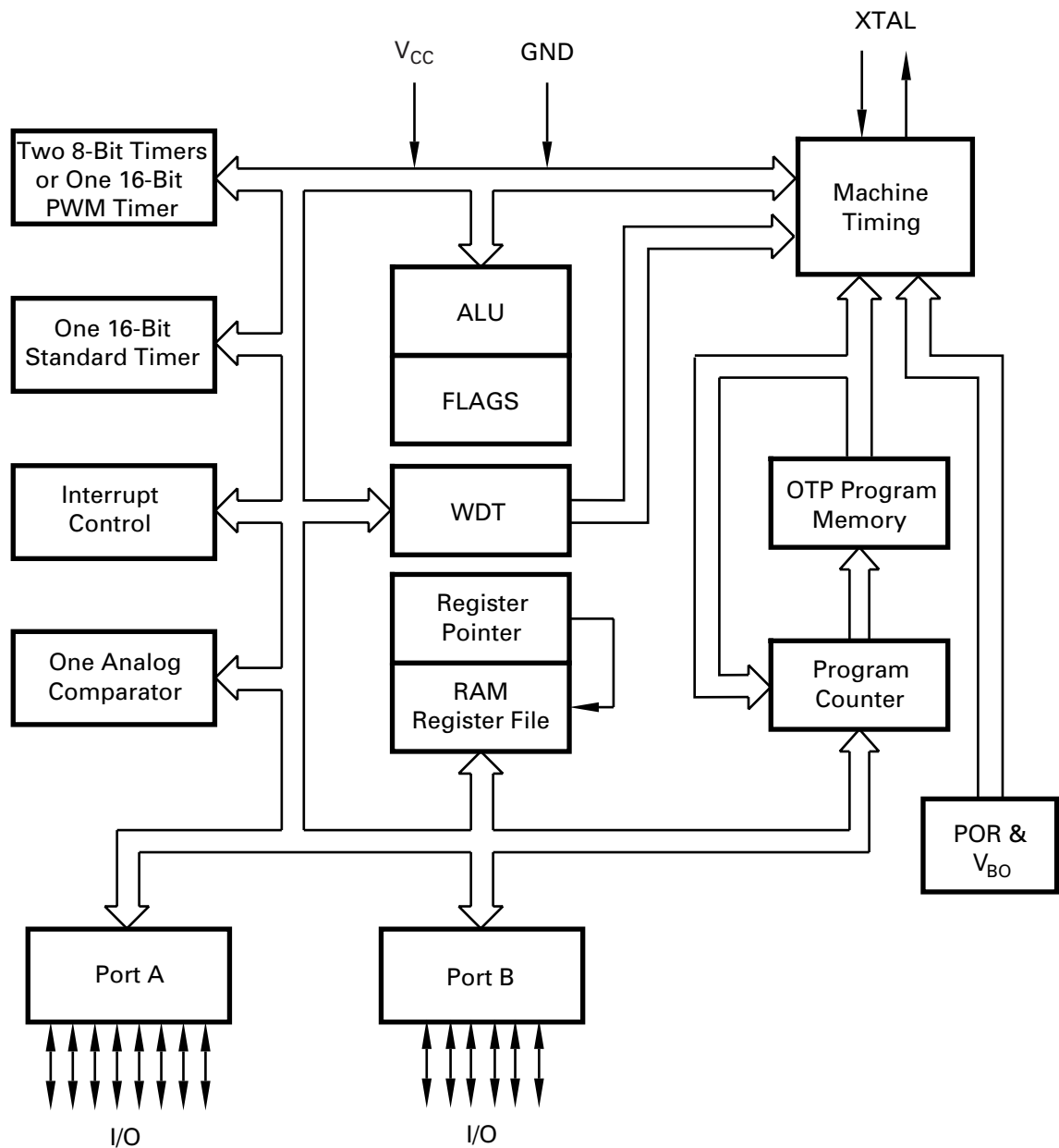


Figure 1. Functional Block Diagram

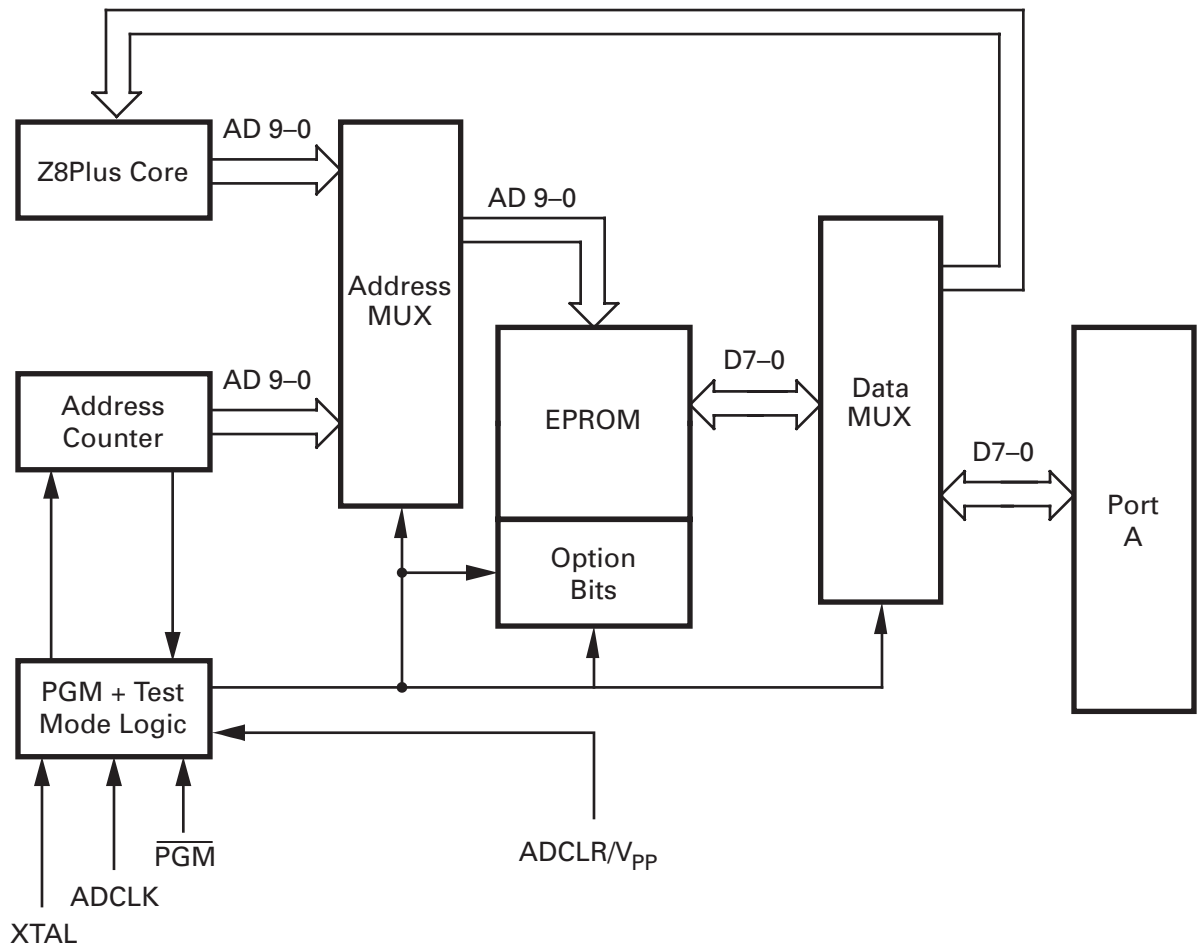


Figure 2. EPROM Programming Mode Block Diagram

PIN DESCRIPTION

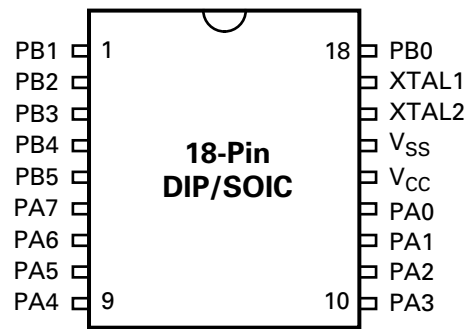


Figure 3. 18-Pin DIP/SOIC Pin Identification

Table 1. Standard Programming Mode

Pin #	Symbol	Function	Direction
1–5	PB1–PB5	Port B, Pins 1,2,3,4,5	Input/Output
6–9	PA7–PA4	Port A, Pins 7,6,5,4	Input/Output
10–13	PA3–PA0	Port A, Pins 3,2,1,0	Input/Output
14	V _{CC}	Power Supply	
15	V _{SS}	Ground	
16	XTAL2	Crystal Oscillator Clock	Output
17	XTAL1	Crystal Oscillator Clock	Input
18	PB0	Port B, Pin 0	Input/Output

DC ELECTRICAL CHARACTERISTICS

Table 5. DC Electrical Characteristics

T _A = 0°C to +70°C Standard Temperatures								
Sym	Parameter	V _{CC} ¹	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
V _{CH}	Clock Input High Voltage	3.0V	0.7V _{CC}	V _{CC} +0.3	1.3	V	Driven by External Clock Generator	
		5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V	Driven by External Clock Generator	
V _{CL}	Clock Input Low Voltage	3.0V	V _{SS} -0.3	0.2V _{CC}	0.7	V	Driven by External Clock Generator	
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.5	V	Driven by External Clock Generator	
V _{IH}	Input High Voltage	3.0V	0.7V _{CC}	V _{CC} +0.3	1.3	V		
		5.5V	0.7V _{CC}	V _{CC} +0.3	2.5	V		
V _{IL}	Input Low Voltage	3.0V	V _{SS} -0.3	0.2V _{CC}	0.7	V		
		5.5V	V _{SS} -0.3	0.2V _{CC}	1.5	V		
V _{OH}	Output High Voltage	3.0V	V _{CC} -0.4		3.1	V	I _{OH} = -2.0 mA	
		5.5V	V _{CC} -0.4		4.8	V	I _{OH} = -2.0 mA	
V _{OL1}	Output Low Voltage	3.0V		0.6	0.2	V	I _{OL} = +4.0 mA	
		5.5V		0.4	0.1	V	I _{OL} = +4.0 mA	
V _{OL2}	Output Low Voltage	3.0V		1.2	0.5	V	I _{OL} = +6 mA	
		5.5V		1.2	0.5	V	I _{OL} = +12 mA	
V _{OFFSET}	Comparator Input Offset Voltage	3.0V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I _{IL}	Input Leakage	3.0V	-1.0	2.0	0.064	μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	2.0	0.064	μA	V _{IN} = 0V, V _{CC}	
I _{OL}	Output Leakage	3.0V	-1.0	2.0	0.114	μA	V _{IN} = 0V, V _{CC}	
		5.5V	-1.0	2.0	0.114	μA	V _{IN} = 0V, V _{CC}	
V _{ICR}	Comparator Input Common Mode Voltage Range	3.0V	V _{SS} -0.3	V _{CC} -1.0		V		3
		5.5V	V _{SS} -0.3	V _{CC} -1.0		V		3
R _{PB5}	PB5 Pull-up Resistor	3.0V	100		200	kOhm		4
		5.5V	100		200			
V _{LV}	V _{CC} Low-Voltage Protection		2.45	2.85	2.60	V		

Notes:

1. The V_{CC} voltage specification of 3.0V guarantees 3.0V; the V_{CC} voltage specification of 5.5V guarantees 5.0V ±0.5V.
2. Typical values are measured at V_{CC} = 3.3V and V_{CC} = 5.0V; V_{SS} = 0V = GND.
3. For the analog comparator input when the analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC}. External protection is recommended.
5. All outputs are unloaded and all inputs are at the V_{CC} or V_{SS} level.
6. CL1 = CL2 = 22 pF.
7. Same as note 5, except inputs are at V_{CC}.

DC ELECTRICAL CHARACTERISTICS (Continued)

Table 6. DC Electrical Characteristics

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ Extended Temperatures								
Sym	Parameter	V_{CC}^1	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
V_{CH}	Clock Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
		5.5V	$0.7 V_{CC}$	$V_{CC}+0.3$	2.5	V		
V_{IL}	Input Low Voltage	4.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
		5.5V	$V_{SS}-0.3$	$0.2 V_{CC}$	1.5	V		
V_{OH}	Output High Voltage	4.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0 \text{ mA}$	
		5.5V	$V_{CC}-0.4$		4.8	V	$I_{OH} = -2.0 \text{ mA}$	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	$I_{OL} = +4.0 \text{ mA}$	
		5.5V		0.4	0.1	V	$I_{OL} = +4.0 \text{ mA}$	
V_{OL2}	Output Low Voltage	4.5V		1.2	0.5	V	$I_{OL} = +12 \text{ mA}$	
		5.5V		1.2	0.5	V	$I_{OL} = +12 \text{ mA}$	
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25.0	10.0	mV		
		5.5V		25.0	10.0	mV		
I_{IL}	Input Leakage	4.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
I_{OL}	Output Leakage	4.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
		5.5V	-1.0	2.0	<1.0	μA	$V_{IN} = 0\text{V}, V_{CC}$	
V_{ICR}	Comparator Input Common Mode Voltage Range	4.5V	0	$V_{CC}-1.5\text{V}$		V		3
		5.5V	0	$V_{CC}-1.5\text{V}$		V		3
R_{PB5}	PB5 Pull-up Resistor	4.5V	100		200	kOhm		4
		5.5V	100		200			
V_{LV}	V_{CC} Low-Voltage Protection		2.45	2.85	2.60	V		
I_{CC}	Supply Current	4.5V		7.0	4.0	mA	@ 10 MHz	5,6
		5.5V		7.0	4.0	mA	@ 10 MHz	5,6

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees $5.0\text{V} \pm 0.5\text{V}$.
2. Typical values are measured at $V_{CC} = 5.0\text{V}$; $V_{SS} = 0\text{V} = \text{GND}$.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC} . External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. $CL1 = CL2 = 22 \text{ pF}$.
7. Same as note 5, except inputs are at V_{CC} .

Table 6. DC Electrical Characteristics (Continued)

$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$ Extended Temperatures								
Sym	Parameter	V_{CC}^1	Min	Max	Typical ² @ 25°C	Units	Conditions	Notes
I_{CC1}	Standby Current	4.5V		2.0	1.0	mA	HALT mode $V_{IN} = 0V$, $V_{CC} @ 10\text{ MHz}$	5,6
		5.5V		2.0	1.0	mA	HALT mode $V_{IN} = 0V$, $V_{CC} @ 10\text{ MHz}$	5,6
I_{CC2}	Standby Current	4.5V		700	250	nA	STOP mode V_{IN} $= 0V, V_{CC}$	7
		5.5V		700	250	nA	STOP mode V_{IN} $= 0V, V_{CC}$	7

Notes:

1. The V_{CC} voltage specification of 4.5V and 5.5V guarantees $5.0V \pm 0.5V$.
2. Typical values are measured at $V_{CC} = 5.0V$; $V_{SS} = 0V = \text{GND}$.
3. For analog comparator input when analog comparator is enabled.
4. No protection diode is provided from the pin to V_{CC} . External protection is recommended.
5. All outputs are unloaded and all inputs are at V_{CC} or V_{SS} level.
6. $CL1 = CL2 = 22\text{ pF}$.
7. Same as note 5, except inputs are at V_{CC} .

INTERRUPT SOURCES

Table 10 presents the interrupt types, sources, and vectors available in the Z8Plus. Other processors from the Z8Plus family may define the interrupts differently.

Table 10. Interrupt Types, Sources, and Vectors

Name	Sources	Vector Location	Comments	Fixed Priority
IREQ ₀	Timer0 Time-out	2,3	Internal	1 (Highest)
IREQ ₁	PB4 High-to-Low Transition	4,5	External (PB4), Edge Triggered	2
IREQ ₂	Timer1 Time-out	6,7	Internal	3
IREQ ₃	PB2 High-to-Low Transition	8,9	External (PB2), Edge Triggered	4
IREQ ₄	PB4 Low-to-High Transition	A,B	External (PB4), Edge Triggered	5
IREQ ₅	Timer2 Time-out	C,D	Internal	6 (Lowest)
IREQ ₆ –IREQ ₁₅	Reserved		Reserved for future expansion	

External Interrupt Sources

External sources can be generated by a transition on the corresponding Port pin. The interrupt may detect a rising edge, a falling edge, or both.

Notes: The interrupt sources and trigger conditions are device dependent. See the device product specification to determine available sources (internal and external), triggering edge options, and exact programming details.

Although interrupts are edge triggered, minimum interrupt request Low and High times must be observed for proper operation. See the device product specification for exact timing requirements on external interrupt requests ($T_{W/L}$, $T_{W/H}$).

Internal Interrupt Sources

Internal interrupt sources and trigger conditions are device dependent. On-chip peripherals may set interrupt under various conditions. Some peripherals always set their corresponding IREQ bit while others must be specifically configured to do so.

See the device product specification to determine available sources, triggering edge options, and exact programming

details. For more details on the interrupt sources, refer to the chapters describing the timers, comparators, I/O ports, and other peripherals.

Interrupt Mask Register (IMASK) Initialization

The IMASK register individually or globally enables or disables the interrupts (Table 11). When bits 0 through 5 are set to 1, the corresponding interrupt requests are enabled. Bit 7 is the master enable bit and must be set before any of the individual interrupt requests can be recognized. Resetting bit 7 disables all the interrupt requests. Bit 7 is set and reset by the EI and DI instructions. It is automatically set to 0 during an interrupt service routine and set to 1 following the execution of an Interrupt Return (IRET) instruction. The IMASK registers are reset to 00h, disabling all interrupts.

Notes: It is not good programming practice to directly assign a value to the master enable bit. A value change should always be accomplished by issuing the EI and DI instructions.

Care should be taken not to set or clear IMASK bits while the master enable is set.

Table 11. Interrupt Mask Register—IMASK (FBh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate U = Undefined/ Undetermined								

Bit Position	R/W	Value	Description
7		0 1	Disables Interrupts Enables Interrupts
6		0	Reserved, must be 0
5		0 1	Disables IRQ5 Enables IRQ5
4		0 1	Disables IRQ4 Enables IRQ4
3		0 1	Disables IRQ3 Enables IRQ3
2		0 1	Disables IRQ2 Enables IRQ2
1		0 1	Disables IRQ1 Enables IRQ1
0		0 1	Disables IRQ0 Enables IRQ0

Interrupt Request (IREQ) Register Initialization

IREQ (Table 12) is a register that stores the interrupt requests for both vectored and polled interrupts. When an interrupt is issued, the corresponding bit position in the register is set to 1. Bits 0 to 5 are assigned to interrupt requests IRQ0 to IRQ5, respectively.

Whenever RESET is executed, the IREQ register is set to 00h.

Table 12. Interrupt Request Register—IREQ (FAh)

Bit	7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate U = Undefined/ Undetermined								

Bit Position	R/W	Value	Description
7	R/W	0	Reserved, must be 0
6	R/W	0	Reserved, must be 0
5	R/W	0 1	IRQ5 reset IRQ5 set
4	R/W	0 1	IRQ4 reset IRQ4 set
3	R/W	0 1	IRQ3 reset IRQ3 set
2	R/W	0 1	IRQ2 reset IRQ2 set
1	R/W	0 1	IRQ1 reset IRQ1 set
0	R/W	0 1	IRQ0 reset IRQ0 set

IREQ SOFTWARE INTERRUPT GENERATION

IREQ can be used to generate software interrupts by specifying IREQ as the destination of any instruction referencing the Z8Plus Standard Register File. These software interrupts (SWI) are controlled in the same manner as hardware generated requests. In other words, the IMASK controls the enabling of each SWI.

To generate a SWI, the request bit in IREQ is set by the following statement:

```
OR IREQ, #NUMBER
```

The immediate data variable, **NUMBER**, has a 1 in the bit position corresponding to the required level of SWI. For example, an SWI must be issued when an IREQ5 occurs. Bit 5 of **NUMBER** must have a value of 1.

```
OR IREQ, #00100000B
```

If the interrupt system is globally enabled, IREQ5 is enabled, and there are no higher priority requests pending, control is transferred to the service routine pointed to by the IREQ5 vector.

Note: Software may modify the IREQ register at any time. Care should be taken when using any instruction that modifies the IREQ register while interrupt sources are active. The software writeback always takes precedence over the hardware. If a software writeback takes place on the same cycle as an interrupt source tries to set an IREQ bit, the new interrupt is lost.

Nesting of Vectored Interrupts

Nesting vectored interrupts allows higher priority requests to interrupt a lower priority request. To initiate vectored interrupt nesting, perform the following steps during the interrupt service routine:

- PUSH the old IMASK on the stack
- Load IMASK with a new mask to disable lower priority interrupts
- Execute an EI instruction
- Proceed with interrupt processing
- Execute a DI instruction after processing is complete
- Restore the IMASK to its original value by POPing the previous mask from the stack
- Execute IRET

Depending on the application, some simplification of the above procedure may be possible.

RESET Conditions

The IMASK and IREQ registers initialize to 00h on RESET.

PROGRAMMABLE OPTIONS

EPROM Protect. When selecting the DISABLE EPROM PROTECT/ENABLE TESTMODE option, the user can read the software code in the program memory. ZiLOG's internal factory test mode, or any of the standard test mode methods, are useful for reading or verifying the code in the microcontroller when using an EPROM programmer. If the user should select the ENABLE EPROM PROTECT/DISABLE TESTMODE option, it is not possible to read the code using a tester, programmer, or any other standard method. As a result, ZiLOG is unable to test the EPROM memory at any time after customer delivery.

This option bit only affects the user's ability to read the code and has no effect on the operation of the part in an application. ZiLOG tests the EPROM memory before customer delivery whether or not the ENABLE EPROM PROTECT/DISABLE TESTMODE option is selected; ZiLOG provides a standard warranty for the part.

System Clock Source. When selecting the RC OSCILLATOR ENABLE option, the oscillator circuit on the microcontroller is configured to work with an external RC circuit. When selecting the Crystal/Other Clock Source option, the oscillator circuit is configured to work with an external crystal, ceramic resonator, or LC oscillator.

Note: The WDT can only be disabled via software if the first instruction out of the `RESET` performs this function. Logic within the device detects that it is in the process of executing the first instruction after the processor leaves `RESET`. During the execution of this instruction, the upper five bits of the TCTLHI register can be written. After this first instruction, hardware does not allow the upper five bits of this register to be written.

The TCTLHI bits for control of the WDT are described below:

WDT Time Select (D6, D5, D4). Bits 6, 5, and 4 determine the time-out period. Table 13 indicates the range of time-out values that can be obtained. The default values of D6, D5, and D4 are 001, which sets the WDT to its minimum time-out period when coming out of `RESET`.

WDT During HALT (D7). This bit determines whether or not the WDT is active during HALT mode. A 1 indicates active during HALT mode. A 0 prevents the WDT from resetting the part while halted. Coming out of `RESET`, the WDT is enabled during HALT mode.

POWER-DOWN MODES

In addition to the standard RUN mode, the Z8Plus MCU supports two Power-Down modes to minimize device cur-

STOP MODE (D3). Coming out of `RESET`, the device STOP mode is disabled. If an application requires use of STOP mode, bit D3 must be cleared immediately at leaving `RESET`. If bit D3 is set, the STOP instruction executes as a NOP. If bit D3 is cleared, the STOP instruction enters STOP mode.

Bits 2, 1 and 0. These bits are reserved and must be 0.

Table 13. WDT Time-Out

D6	D5	D4	Crystal Clocks* to Timeout	Time-Out Using a 10-MHz Crystal
0	0	0	Disabled	Disabled
0	0	1	65,536 TpC	6.55 ms
0	1	0	131,072 TpC	13.11 ms
0	1	1	262,144 TpC	26.21 ms
1	0	0	524,288 TpC	52.43 ms
1	0	1	1,048,576 TpC	104.86 ms
1	1	0	2,097,152 TpC	209.72 ms
1	1	1	8,388,608 TpC	838.86 ms

Note: *TpC is an XTAL clock cycle. The default at reset is 001.

rent consumption. The two modes supported are HALT and STOP.

HALT MODE OPERATION

The HALT mode suspends instruction execution and turns off the internal CPU clock. The on-chip oscillator circuit remains active so the internal clock continues to run and is applied to the timers and interrupt logic.

To enter HALT mode, the device only requires a HALT instruction. It is *not* necessary to execute a NOP instruction immediately before the HALT instruction.

```
7F    HALT    ; enter HALT mode
```

HALT mode can be exited by servicing an external or internal interrupt. The first instruction executed is the interrupt service routine. At completion of the interrupt service routine, the user program continues from the instruction after the HALT instruction.

The HALT mode can also be exited via a `RESET` activation or a Watch-Dog Timer (WDT) time-out. In these cases, program execution restarts at 0020H, the reset restart address.

CLOCK

The Z8Plus MCU derives its timing from on-board clock circuitry connected to pins XTAL1 and XTAL2. The clock circuitry consists of an oscillator, a glitch filter, and a divide-by-two shaping circuit. Figure 12 illustrates the clock circuitry. The oscillator's input is XTAL1 and its output is XTAL2. The clock can be driven by a crystal, a ceramic resonator, LC clock, or an external clock source.

By selecting the RC OSCILLATOR option in the graphical user interface (GUI), the circuit may instead be driven by an external Resistor and Capacitor (RC) oscillator. Figure 13 illustrates this configuration. This design is limited to no more than 4 MHz to restrict EMI noise.

Note: The reduced drive strength of this configuration also allows the clock circuit to use a micropower-type crystal (also known as a tuning fork) without reduction resistors.

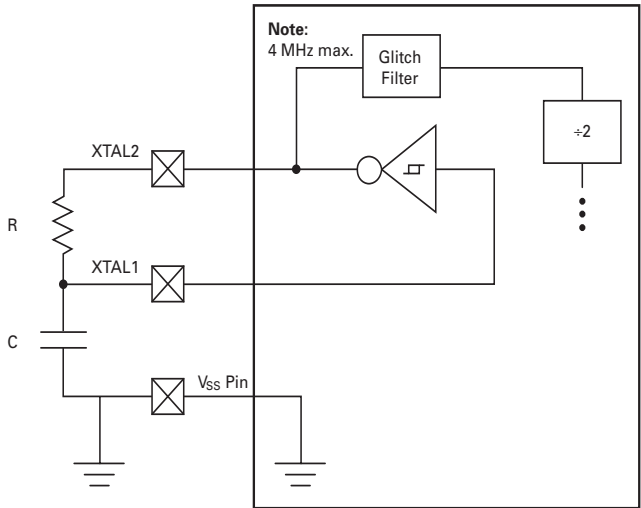


Figure 13. Z8Plus in RC Oscillator Mode

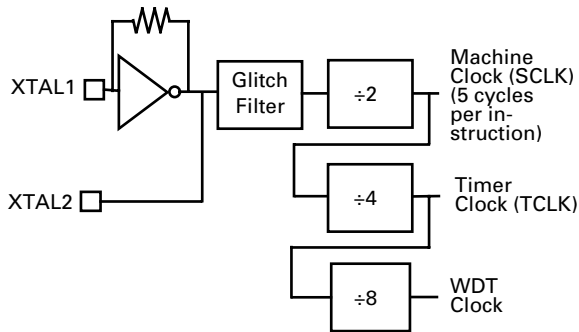


Figure 12. Clock Circuit

LC OSCILLATOR

The Z8Plus oscillator can use an inductor capacitor oscillator (LC) network to generate an XTAL clock (Figure 17). The frequency stays stable over V_{CC} and temperature. The oscillation frequency is determined by the equation:

$$\text{Frequency} = \frac{1}{2\pi (LC_T)^{1/2}}$$

where L is the total inductance including parasitics, and C_T is the total series capacitance including parasitics. Simple series capacitance is calculated using the equation at the top of the next column.

$$\begin{aligned} 1/C_T &= 1/C_1 + 1/C_2 \\ \text{If } C_1 &= C_2 \\ 1/C_T &= 2/C_1 \\ C_1 &= 2C_T \end{aligned}$$

A sample calculation of capacitance C₁ and C₂ for 5.83-MHz frequency and inductance value of 27 μH is displayed as follows:

$$5.83 (10^6) = \frac{1}{2\pi [27 (10^{-6}) C_T]^{1/2}}$$

$$C_T = 27.6 \text{ pF}$$

Thus, C₁ = 55.2 pF and C₂ = 55.2 pF.

TIMERS

Two 8-bit timers, timer 0 (T0) and timer 1 (T1) are available to function as a pair of independent 8-bit standard timers. They may also be cascaded to function as a 16-bit Pulse-

Width Modulator (PWM) timer. Two additional 8-bit timers (T2 and T3) are provided, but they can only operate as one 16-bit standard timer.

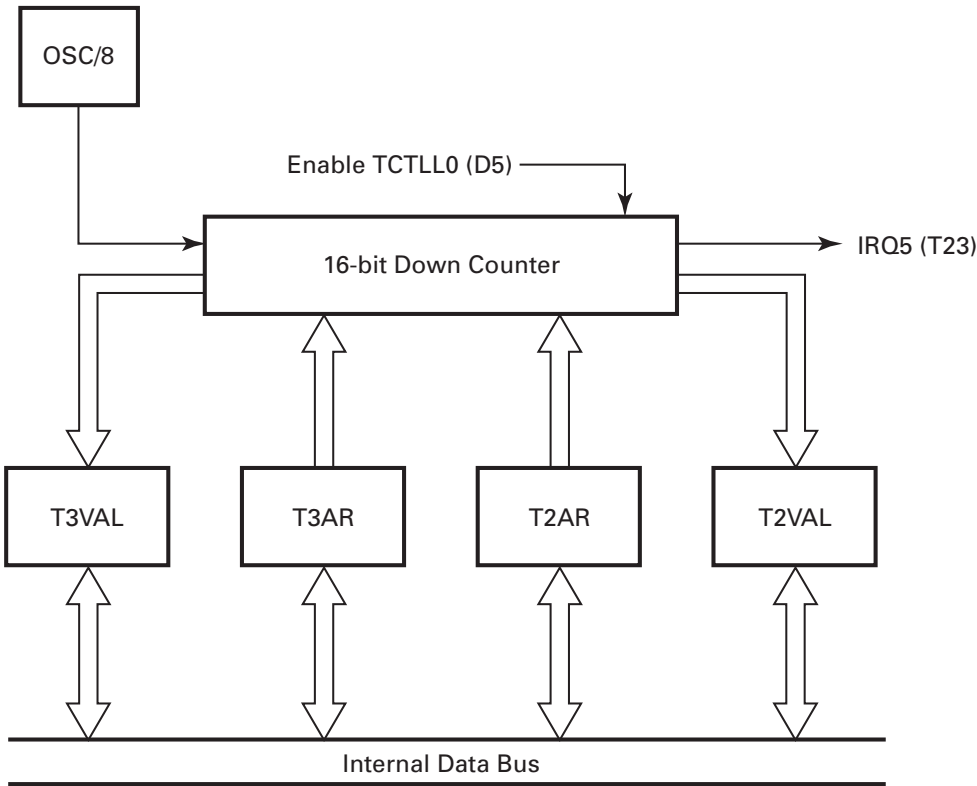


Figure 19. 16-Bit Standard Timer

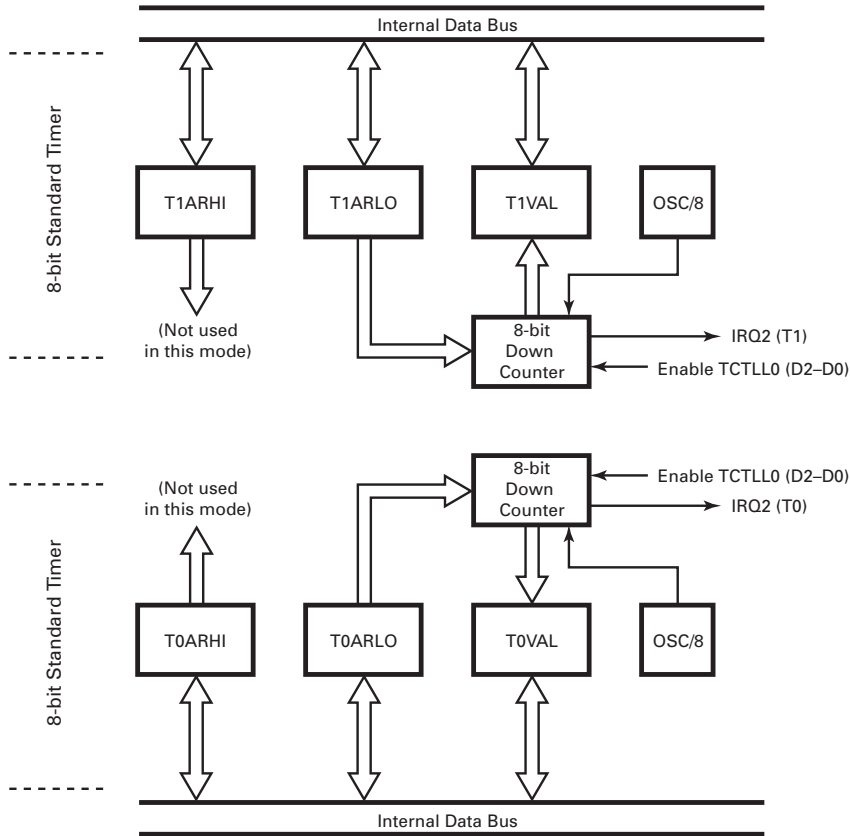


Figure 20. 8-Bit Standard Timers

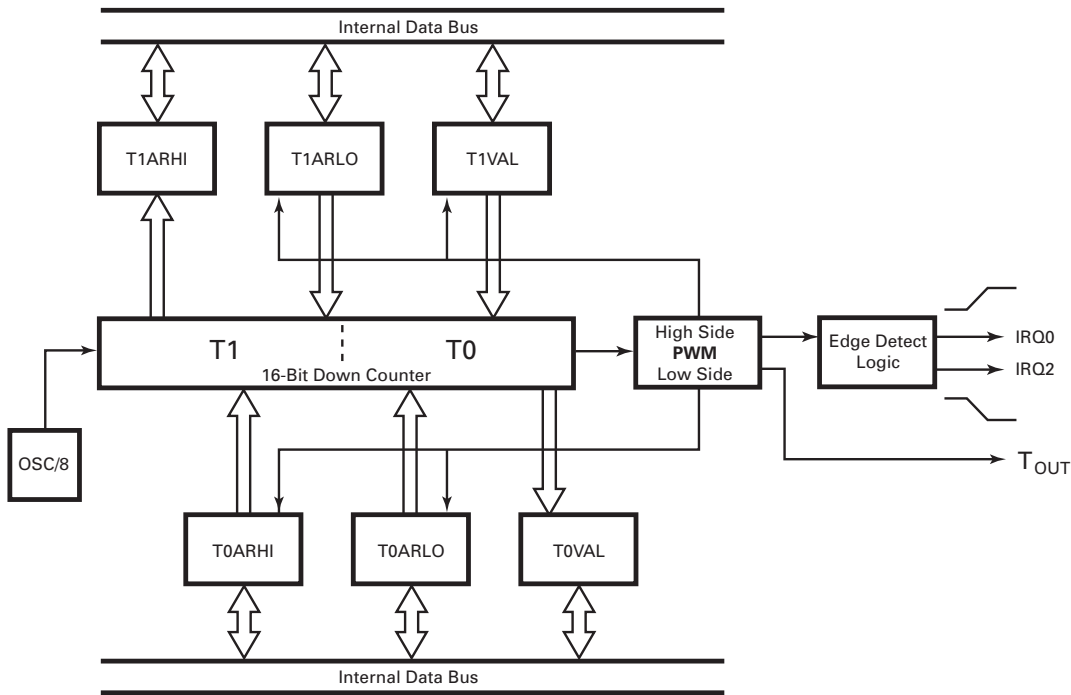


Figure 21. 16-Bit Standard PWM Timer

If a timer pair is defined to operate as a single 16-bit entity, the entire 16-bit value must reach 0 before an interrupt is generated. In this case, a single interrupt is generated, and the interrupt corresponds to the even 8-bit timer.

Example: Timers T2 and T3 are cascaded to form a single 16-bit timer. The interrupt for the combined timer is defined to be generated by timer T2 rather than T3. When a timer pair is specified to act as a single 16-bit timer, the even timer registers in the pair (timer T0 or T2) is defined to hold the timer's least significant byte. In contrast, the odd timer in the pair holds the timer's most significant byte.

In parallel with the posting of the interrupt request, the interrupting timer's count value is initialized by copying the contents of the auto-initialization value register to the count value register.

Note: Any time that a timer pair is defined to act as a single 16-bit timer, the auto-reload function is performed automatically.

All 16-bit timers continue counting while their interrupt requests are active and operate independently of each other.

If interrupts are disabled for a long period of time, it is possible for the timer to decrement to 0 again before its initial interrupt is responded to. This condition is termed a degenerate case, and hardware is not required to detect it.

When the timer control register is written, all timers that are enabled by the WRITE begin counting from the value in the count register. In this case, an auto-initialization is not performed. All timers can receive an internal clock source input only. Each enabled timer is updated every 8th XTAL clock cycle.

If T0 and T1 are defined to work independently, then each works as an 8-bit timer with a single auto-initialization register (T0ARLO for T0, and T1ARLO for T1). Each timer asserts its predefined interrupt when it times out, optionally performing the auto-initialization function. If T0 and T1 are cascaded to form a single 16-bit timer, then the single 16-bit timer is capable of performing as a Pulse-Width Modulator (PWM). This timer is referred to as T01 to distinguish it as having special functionality that is not available when T0 and T1 act independently.

When T01 is enabled, it can use a pair of 16-bit auto-initialization registers. In this mode, one 16-bit auto-initial-

ization value is composed of the concatenation of T1ARLO and T0ARLO. The second auto-initialization value is composed of the concatenation of T1ARHI and T0ARHI. When T01 times out, it alternately initializes its count value using the Low auto-init pair, followed by the High auto-init pair. This functionality corresponds to a PWM. That is, the T1 interrupt defines the end of the High section of the waveform, and the T0 interrupt marks the end of the Low portion of the PWM waveform.

The PWM begins counting with whatever data is held in the count registers. After this value expires, the first reload depends on the state of the PB1 pin if T_{OUT} mode is selected. Otherwise, the Low value is applied first.

After the auto-initialization is completed, decrementing occurs for the number of counts defined by the PWM_LO registers. When decrementing again reaches 0, the T0 interrupt is asserted; and auto-init using the PWM_HI registers occurs. Decrementing occurs for the number of counts defined by the PWM_HI registers until reaching 0. From there, the T1 interrupt IRQ2 is asserted, and the cycle begins again.

The internal timers can be used to trigger external events by toggling the PB1 output when generating an interrupt. This functionality can only be achieved in conjunction with the port unit defining the appropriate pin as an output signal with the timer output special function enabled. In this mode, the port output is toggled when the timer count reaches 0, and continues toggling each time that the timer times out.

T_{OUT} Mode

The PortB special function register PTBSFR (0D7H; Figure 23) is used in conjunction with the Port B directional control register PTBDIR (0D6; Figure 24) to configure PB1 for T_{OUT} operation for T0. In order for T_{OUT} to function, PB1 must be defined as an output line by setting PTBDIR bit 1 to 1. Configured in this way, PB1 is capable of being a clock output for T0, toggling the PB1 output pin on each T0 time-out.

At end-of-count, the interrupt request line (IRQ0), clocks a toggle flip-flop. The output of this flip-flop drives the T_{OUT} line, PB1. In all cases, when T0 reaches its end-of-count, T_{OUT} toggles to its opposite state (Figure 25). If, for example, T0 is in Continuous Counting Mode, T_{OUT} exhibits a 50-percent duty cycle output. If the timer pair is selected (T01) as a PWM, the duty cycle depends on the High and Low reload values. At the end of each High time, PB1 toggles Low. At the end of each Low time, PB1 toggles HI.

TIMERS (Continued)

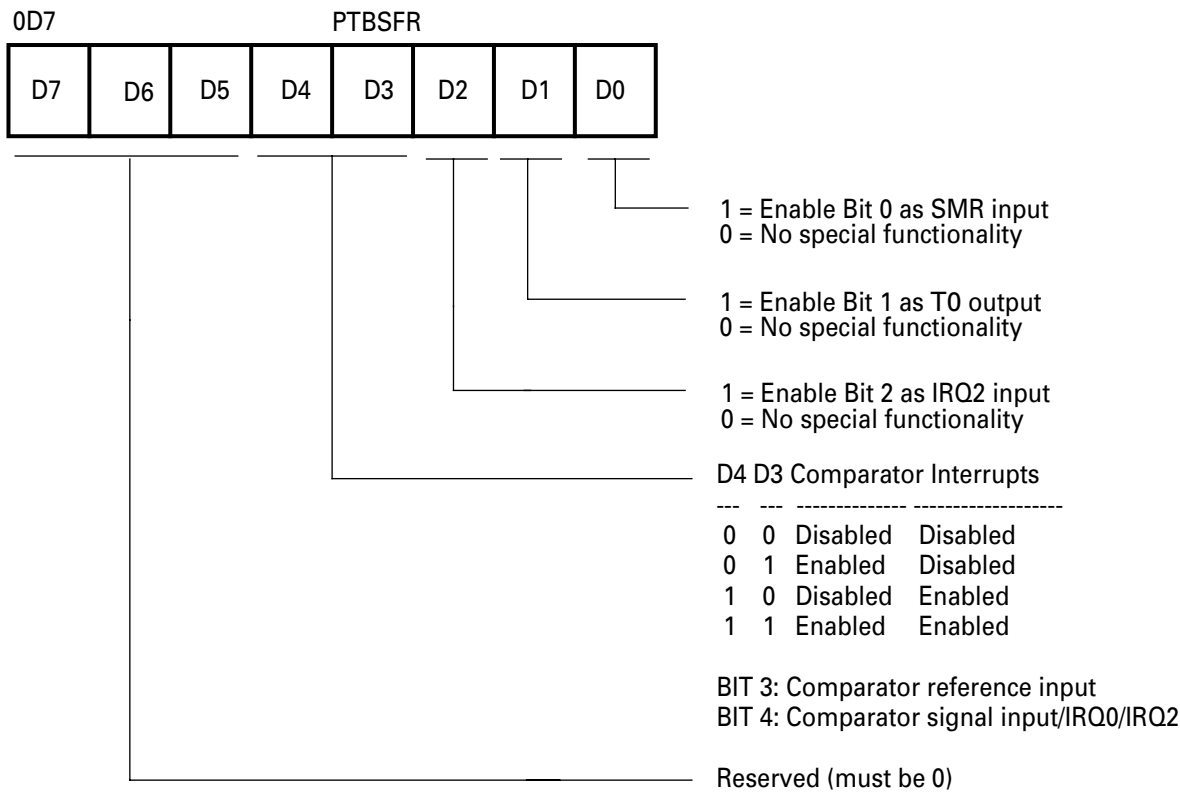


Figure 23. PortB Special Function Register

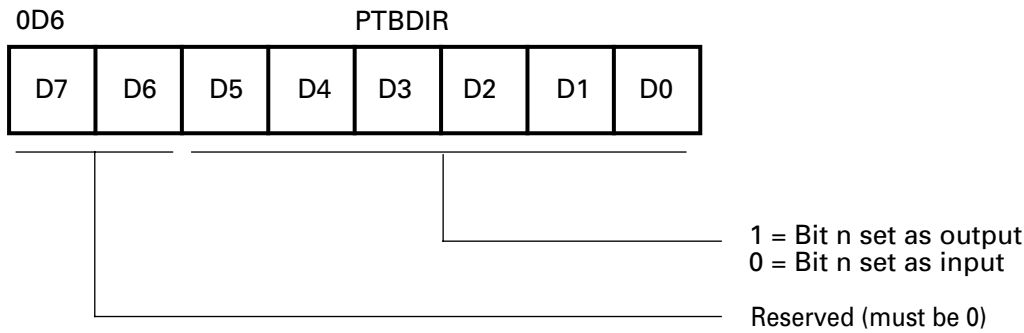


Figure 24. Port B Directional Control Register

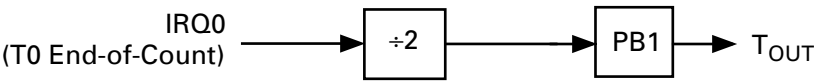


Figure 25. Timer T0 Output Through TOUT

RESET CONDITIONS

After a $\overline{\text{RESET}}$, the timers are disabled. See Table 8 for timer control, value, and auto-initialization register status after $\overline{\text{RESET}}$.

I/O PORTS

The Z8Plus dedicates 14 lines to input and output. These lines are grouped into two ports known as Port A and Port B. Port A is an 8-bit port, bit programmable as either inputs or outputs. Port B can be programmed to provide either standard input/output, or the following special functions: T0 output, comparator input, SMR input, and external interrupt inputs.

All pins except PB5 include push-pull CMOS outputs. In addition, the outputs of Port A on a bit-wise basis can be configured for open-drain operation. The ports operate on a bit-wise basis. As such, the register values for/at a given bit position only affect the bit in question.

Each port is defined by a set of four control registers (Figure 26).

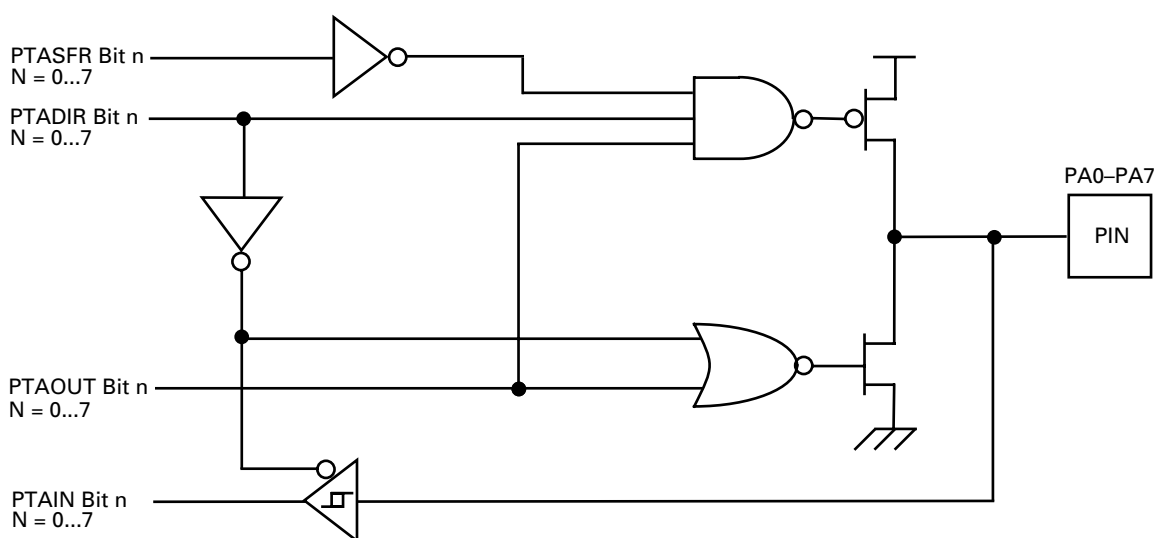


Figure 26. Port A Configuration with Open-Drain Capability and Schmitt-Trigger

Directional Control and Special Function Registers

Each port on the Z8Plus features a dedicated directional control register that determines (on a bit-wise basis) if a given port bit operates as input or output.

Each port on the Z8Plus features a special function register (SFR) that, in conjunction with the directional control register, implements (on a bit-by-bit basis) any special functionality that can be defined for each particular port bit.

Table 14. I/O Ports Registers

Register	Address	Identifier
Port B Special Function	0D7H	PTBSFR
Port B Directional Control	0D6H	PTBDIR
Port B Output Value	0D5H	PTBOUT
Port B Input Value	0D4H	PTBIN
Port A Special Function	0D3H	PTASFR
Port A Directional Control	0D2H	PTADIR
Port A Output Value	0D1H	PTAOUT
Port A Input Value	0D0H	PTAIN

Input and Output Value Registers

Each port features an Output Value Register and an input value register. For port bits configured as an input by means of the directional control register, the input value register

for that bit position contains the current synchronized input value.

For port bits configured as an output by means of the directional control register, the value held in the corresponding bit of the Output Value Register is driven directly onto

the output pin. The opposite register bit for a given pin (the output register bit for an input pin and the input register bit for an output pin) holds their previous value. These bits are not changed and do not exhibit any effect on the hardware.

READ/WRITE OPERATIONS

The control for each port is done on a bit-by-bit basis. All bits are capable of operating as inputs or outputs, depending on the setting of the port’s directional control register. If configured as an input, each bit is provided a Schmitt-trigger. The output of the Schmitt-trigger is latched twice to perform a synchronization function, and the output of the synchronizer is fed to the port input register, which can be read by software.

A WRITE to a port input register carries the effect of updating the contents of the input register, but subsequent READs do not necessarily return the same value that was written. If the bit in question is defined as an input, the input register for that bit position contains the current synchronized input value. WRITEs to that bit position are overwritten on the next clock cycle with the newly sampled input data. However, if the particular bit is programmed as an output, the input register for that bit retains the software-updated value. The port bits that are programmed as outputs do not sample the value being driven out.

Any bit in either port can be defined as an output by setting the appropriate bit in the directional control register. In this instance, the value held in the appropriate bit of the port output register is driven directly onto the output pin.

Note: The preceding result does not necessarily reflect the actual output value. If an external error is holding an output pin either High or Low against the output driver, the software READ returns the *requested* value, not the actual state caused by the contention. When a bit is defined as an output, the Schmitt-trigger on the input is disabled to save power.

Updates to the output register take effect based on the timing of the internal instruction pipeline; however, this timing is referenced to the rising edge of the clock. The output register can be read at any time, and returns the current output value that is held. No restrictions are placed on the timing of READs and/or WRITEs to any of the port registers with respect to the others.

Note: Care should be taken when updating the directional control and special function registers.

When updating a directional control register, the special function register (SFR) should first be disabled. If this precaution is not taken, unpredicted events could occur as a result of the change in the port I/O status. This precaution is especially important when defining changes in Port B, as the unpredicted event referred to above could be one or more interrupts. Clearing of the SFR register should be the first step in configuring the port, while setting the SFR register should be the final step in the port configuration process. To ensure unpredictable results, the SFR register should not be written until the pins are being driven appropriately, and all initialization is completed.

PORT A

Port A is a general-purpose port. Figure 27 features a block diagram of Port A. Each of its lines can be independently programmed as input or output via the Port A directional control register (PTADIR at 0D2H) as seen in Figure 26. A bit set to a 1 in PTADIR configures the corresponding bit in Port A as an output, while a bit cleared to 0 configures the corresponding bit in Port A as an input.

The input buffers are Schmitt-triggered. Bits programmed as outputs can be individually programmed as either push-

pull or open-drain by setting the corresponding bit in the special function register (PTASFR, Figure 26).

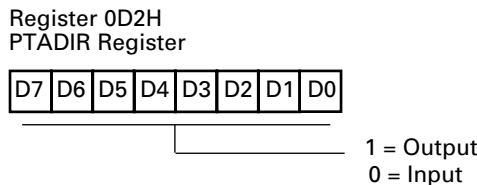


Figure 27. Port A Directional Control Register

PORT A REGISTER DIAGRAMS

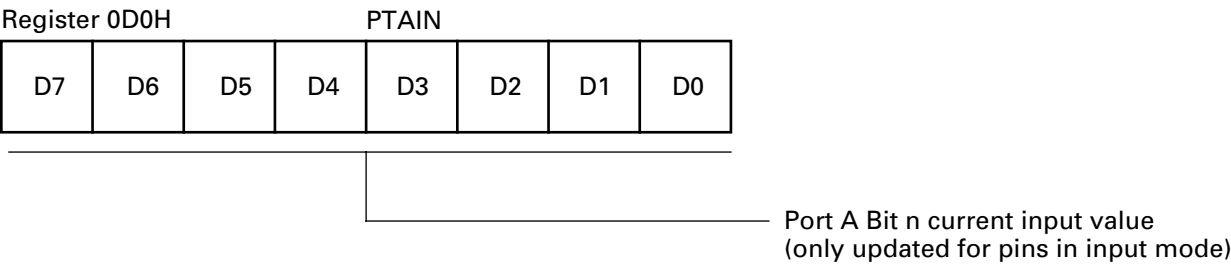


Figure 28. Port A Input Value Register

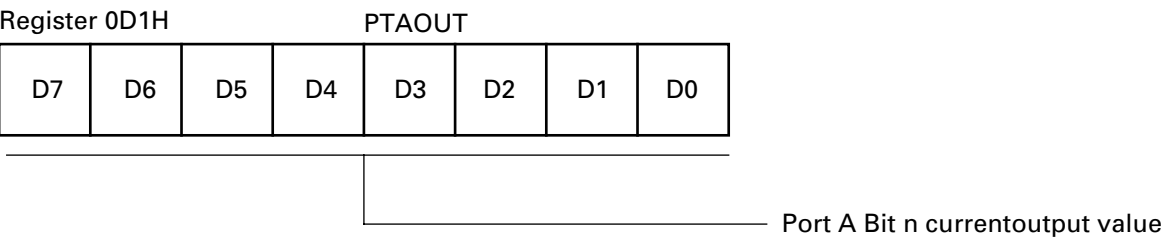


Figure 29. Port A Output Value Register

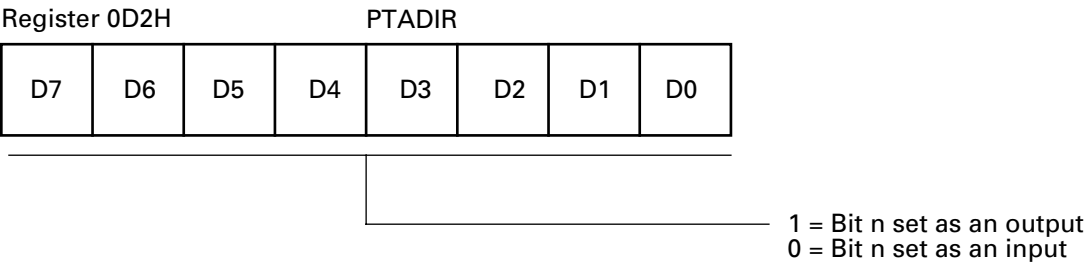


Figure 30. Port A Directional Control Register

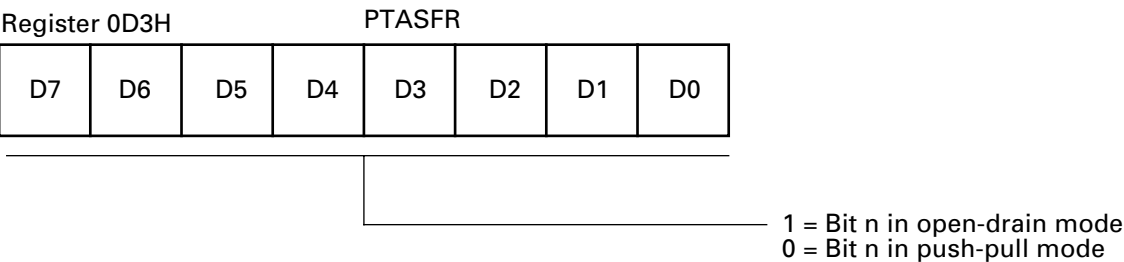


Figure 31. Port A Special Function Register

PORT B—PIN 2 CONFIGURATION

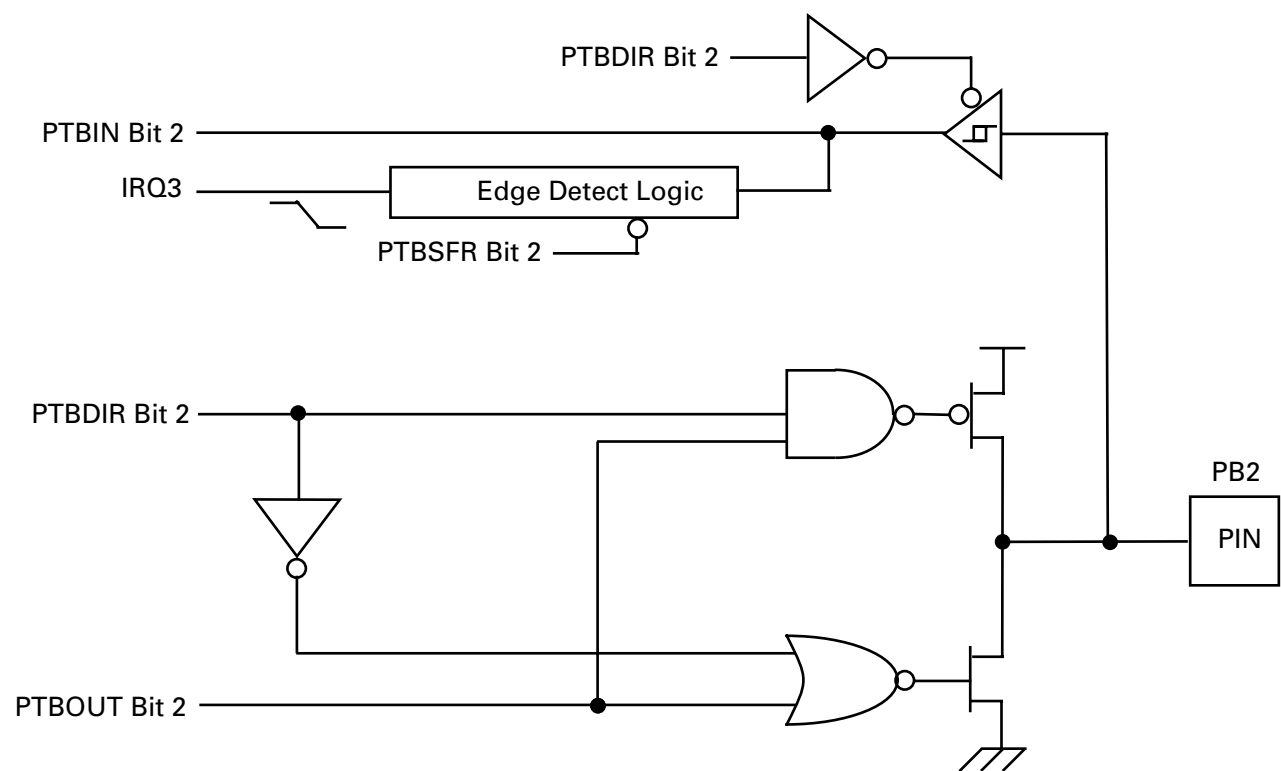


Figure 36. Port B Pin 2 Diagram

COMPARATOR OPERATION (Continued)

age Protection trip point (V_{LV}) is reached. The actual Low-Voltage Protection trip point is a function of process parameters.

Low-Voltage Protection is active in RUN and HALT modes only, but is disabled in STOP mode (Figure 42).

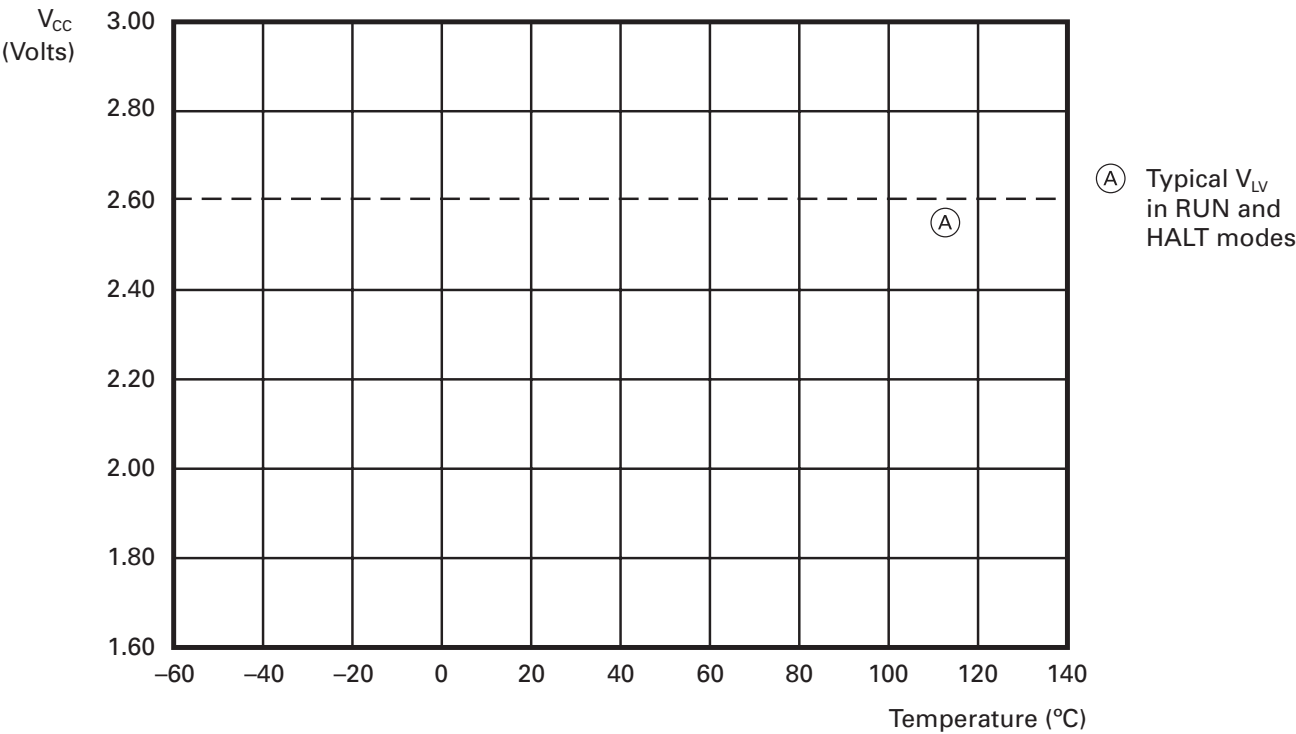


Figure 42. Typical Low Voltage Protection vs. Temperature