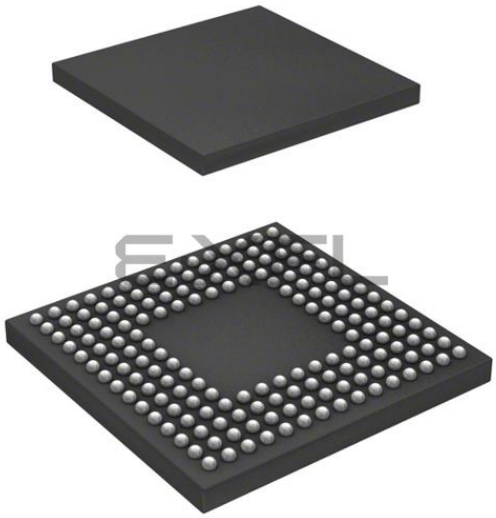
Renesas Electronics America Inc - R7FS5D97C2A01CBG#AC0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LFBGA
Supplier Device Package	176-LFBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d97c2a01cbg-ac0

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(2012.4)

1. Overview

The S5D9 MCU integrates multiple series of software- and pin-compatible ARM®-based 32-bit MCUs that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU provides a high-performance ARM Cortex®-M4 core running up to 120 MHz with the following features:

- Up to 2-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 ARM core

Feature	Functional description
ARM Cortex-M4	• Maximum operating frequency: up to 120 MHz • ARM Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating point unit compliant with the ANSI/IEEE Std 754-2008 • ARM Memory Protection Unit (MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions • SysTick timer: - Driven by LOCO clock

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2 MB of code flash memory. See section 55, Flash Memory in User's Manual.
Data flash memory	64 KB of data flash memory. See section 55, Flash Memory in User's Manual.
Memory Mirror Function (MMF)	The MMF can be configured to mirror the wanted application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF) in User's Manual.
SRAM	On-chip high-speed SRAM providing either parity-bit or Error Correction Code (ECC). The first 32 KB of SRAM0 is subject to ECC. Parity check is performed for other areas. See section 53, SRAM in User's Manual.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 54, Standby SRAM in User's Manual.

Table 1.3 System (1 of 3)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes in User's Manual.

Table 1.11 Graphics

Feature	Functional description
Graphics LCD Controller (GLCDC)	The GLCDC provides multiple functions and supports various data formats and panels. Key GLCDC features include: • GPX bus master function for accessing graphics data • Superimposition of three planes (single color background plane, graphic 1 plane, and graphic 2 plane) • Support for many types of 32- or 16-bit per pixel graphics data and 8-, 4-, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. See section 58, Graphics LCD Controller (GLCDC) in User's Manual.
2D Drawing Engine (DRW)	The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW) in User's Manual.
JPEG Codec (JPEG)	The JPEG Codec (JPEG) incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec (JPEG) in User's Manual.
Parallel Data Capture Unit (PDC)	One PDC unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual.

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The DOC compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC) in User's Manual.
Sampling Rate Converter (SRC)	The SRC converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC) in User's Manual.

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA and DSA. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH - 128-bit unique ID.

1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

Table 1.16 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal.
	SDCS	Output	SDRAM chip select signal, active low.
	RAS	Output	SDRAM low address strobe signal, active low.
	CAS	Output	SDRAM column address strobe signal, active low.
	WE	Output	SDRAM write enable signal, active low.
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00.
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08.
	A00 to A15	Output	Address bus.
	DQ00 to DQ15	I/O	Data bus.
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins.
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins.
	GTIU	Input	Hall sensor input pin U.
	GTIV	Input	Hall sensor input pin V.
	GTIW	Input	Hall sensor input pin W.
	GTOUUP	Output	Three-phase PWM output for BLDC motor control (positive U phase).
	GTOULO	Output	Three-phase PWM output for BLDC motor control (negative U phase).
	GTOVUP	Output	Three-phase PWM output for BLDC motor control (positive V phase).
	GTOVLO	Output	Three-phase PWM output for BLDC motor control (negative V phase).
	GTOWUP	Output	Three-phase PWM output for BLDC motor control (positive W phase).
	GTOWLO	Output	Three-phase PWM output for BLDC motor control (negative W phase).
AGT	AGTEE0, AGTEE1	Input	External event input enable signals.
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins.
	AGTO0, AGTO1	Output	Pulse output pins.
	AGTOA0, AGTOA1	Output	Output compare match A output pins.
	AGTOB0, AGTOB1	Output	Output compare match B output pins.
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock.
	RTCIC0 to RTCIC2	Input	Time capture event input pins.
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode).
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode).
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode).
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active low.
	SCL0 to SCL9	I/O	Input/output pins for the I^2C clock (simple IIC mode).
	SDA0 to SDA9	I/O	Input/output pins for the I^2C data (simple IIC mode).
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode).
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode).
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode).
	SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active low.
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock.
	SDA0 to SDA2	I/O	Input/output pins for data.
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins.
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins.
	SSILRCK1/SSIFS1		
	SSITXD0	Output	Serial data output pins.
	SSIRXD0	Input	Serial data input pins.
	SSIDATA1	I/O	Serial data input/output pins.
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock).

Pin number								Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
A8	66	A6	54	37	TRDATA3	-	P208	-	-	-	GTOVLO	-	-	-	-	-	-	QIO3	-	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT0_B	-	-	-	LCD_DATA18_B
C9	67	C7	55	38	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	68	B6	56	39	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	69	C8	57	40	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	70	-	-	-	-	-	P908	CS7	-	-	-	GTIOC2A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA14_B
D7	71	-	-	-	-	-	P907	CS6	-	-	-	GTIOC2B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA13_B
A7	72	-	-	-	-	-	P906	CS5	-	-	-	GTIOC3A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA12_B
B7	73	-	-	-	-	-	P905	CS4	-	-	-	GTIOC3B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA11_B
C7	74	C6	58	-	-	-	P312	CS3	CAS	AGTOA1	-	-	-	-	-	CTS3_RTS3/SS3	-	-	-	-	-	-	-	-	-	-	-
D6	75	B5	59	-	-	-	P311	CS2	RAS	AGTOB1	-	-	-	-	-	SCK3	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_A
A6	76	D7	60	-	-	-	P310	A15	A15	AGTEE1	-	-	-	-	-	TXD3	-	QIO3	-	-	-	-	-	-	-	-	LCD_DATA22_A
B6	77	A5	61	-	-	-	P309	A14	A14	-	-	-	-	-	-	RXD3	-	QIO2	-	-	-	-	-	-	-	-	LCD_DATA21_A
A5	78	C5	62	-	-	-	P308	A13	A13	-	-	-	-	-	-	-	-	QIO1	-	-	-	-	-	-	-	-	LCD_DATA20_A
C6	79	A4	63	41	-	-	P307	A12	A12	-	GTOUUP	-	-	-	CTS6	-	-	QIO0	-	-	-	-	-	-	-	-	LCD_DATA19_A
A4	80	B4	64	42	-	-	P306	A11	A11	-	GTOULO	-	-	-	SCK6	-	-	QSSL	-	-	-	-	-	-	-	-	LCD_DATA18_A
B5	81	D6	65	43	-	IRQ8	P305	A10	A10	-	GTOWUP	-	-	-	TXD6/MOSI6/SDA6	-	-	QSPCLK	-	-	-	-	-	-	-	-	LCD_DATA17_A
B4	82	C4	66	44	-	IRQ9	P304	A09	A09	-	GTOWLO	GTIOC7A	-	-	RXD6/MISO6/SCL6	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_A
C5	83	A3	67	45	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D5	84	B3	68	46	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	85	D5	69	47	-	-	P303	A08	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
B3	86	A2	70	48	-	IRQ5	P302	A07	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-	-	-	-	LCD_DATA14_A
A2	87	C3	71	49	-	IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-	-	-	-	LCD_DATA13_A
C4	88	B2	72	50	TCK/SWCLK	-	P300	-	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-
C3	89	A1	73	51	TMS/SWDIO	-	P108	-	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-	-	-	-	-
A1	90	D4	74	52	CLKOUT/TDO/SWO	-	P109	-	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-	-	-	-	-
D3	91	B1	75	53	TDI	IRQ3	P110	-	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	-
D4	92	C2	76	54	-	IRQ4	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-	-	-	-	LCD_DATA12_A
B2	93	D3	77	55	-	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-	-	-	-	LCD_DATA11_A
B1	94	C1	78	56	-	-	P113	A03	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-	-	-	-	LCD_DATA10_A
C2	95	E4	79	57	-	-	P114	A02	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-	-	-	-	LCD_DATA09_A
C1	96	E3	80	58	-	-	P115	A01	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-	-	-	-	LCD_DATA08_A
E3	97	D2	81	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E4	98	D1	82	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	99	F4	83	59	-	-	P608	A00/BC0	A00/DQM1	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A
D1	100	E2	84	60	-	-	P609	CS1	CKE	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
F3	101	F3	85	61	-	-	P610	CS0	WE	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	102	E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-	-
E1	103	F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-	-
F4	104	F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-	-
F2	105	G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-	-
F1	106	-	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G1	107	-	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B

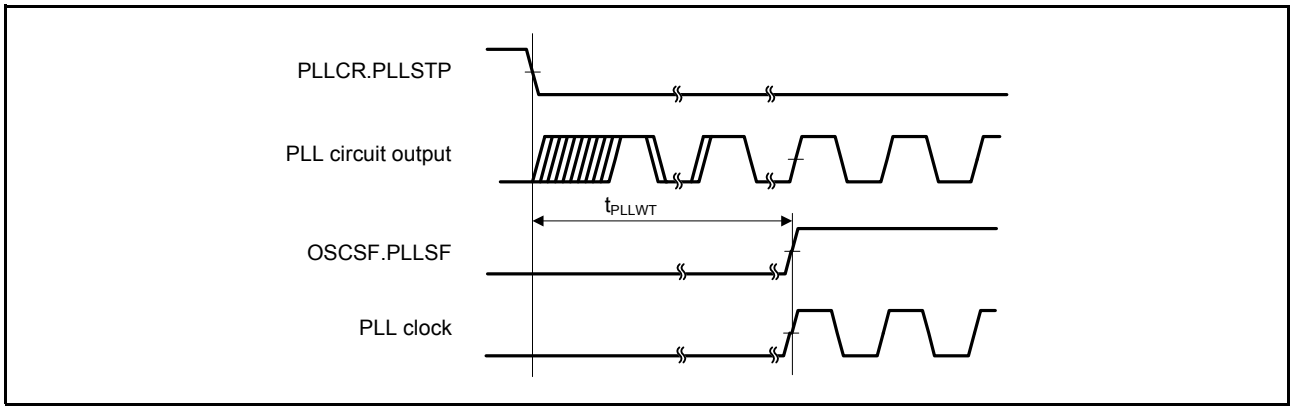


Figure 2.7 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

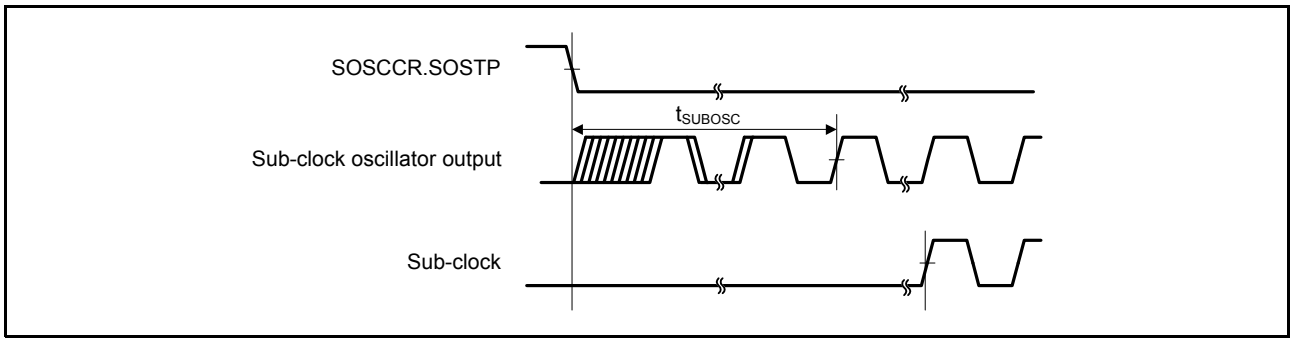


Figure 2.8 Sub-clock oscillation start timing

2.3.3 Reset Timing

Table 2.15 Reset timing

Item		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 2.9
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 2.10
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	µs	
Wait time after RES cancellation		t_{RESWT}	-	29	33	µs	Figure 2.9
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	408	µs	-

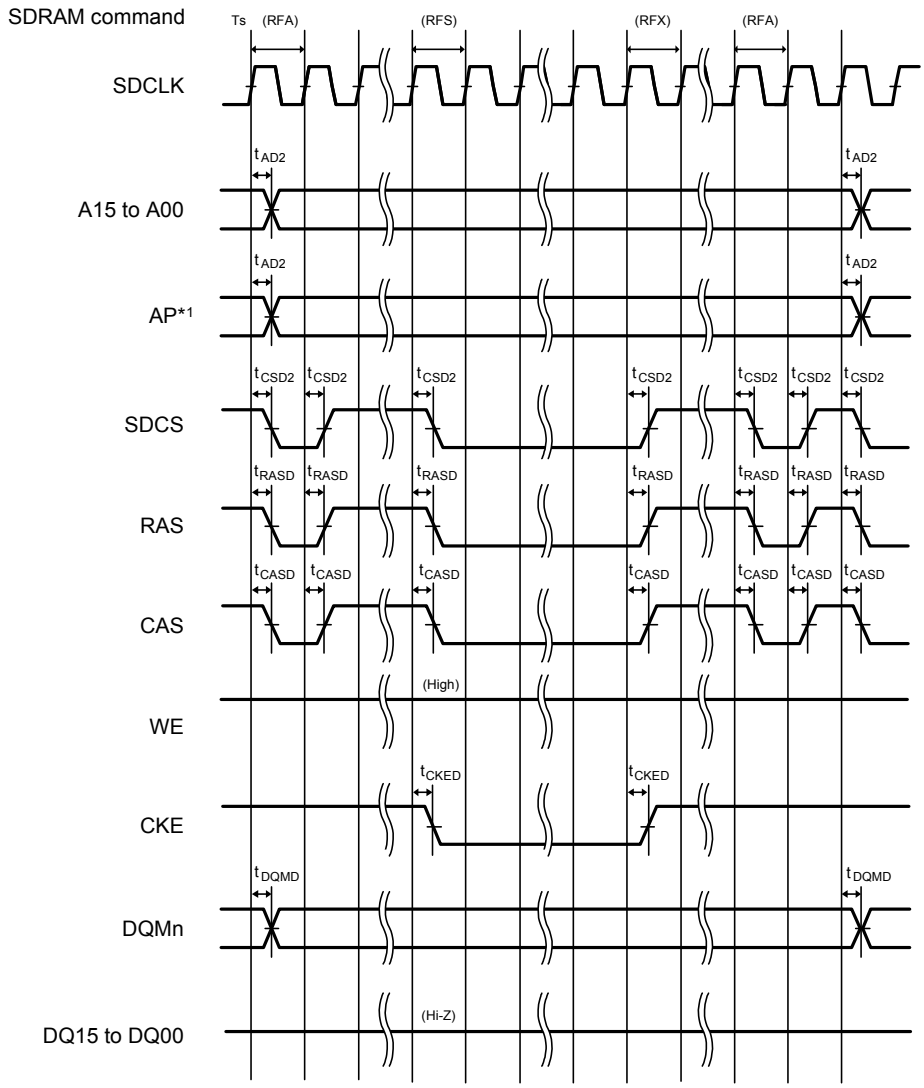
Table 2.18 Bus timing (2 of 2)

Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Item	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	t_{AD2}	0.8	6.8	ns	Figure 2.23 to Figure 2.29
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	2.9	-	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	1.5	-	ns	
Write data delay 2 (SDRAM)	t_{WDD2}	-	6.8	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	-	ns	
WE delay (SDRAM)	t_{WED}	0.8	6.8	ns	
RAS delay (SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS delay (SDRAM)	t_{CASD}	0.8	6.8	ns	



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.29 SDRAM self-refresh timing

2.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)

GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 2.30
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 2.31

Table 2.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)

GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 2.32
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*2	-	4	ns	Figure 2.33
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 2.34
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*3	-	2.0	ns	Figure 2.35
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*4	100	-	ns	Figure 2.36
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 2.37
KINT	Key interrupt input low width		t_{KR}	250	-	ns	Figure 2.38

Note 1. t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 2. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 3. The load is 30 pF.
Note 4. Constraints on AGTIO input: $t_{Pcyc} \times 2$ (t_{Pcyc}: PCLKB cycle) < t_{ACYC}.

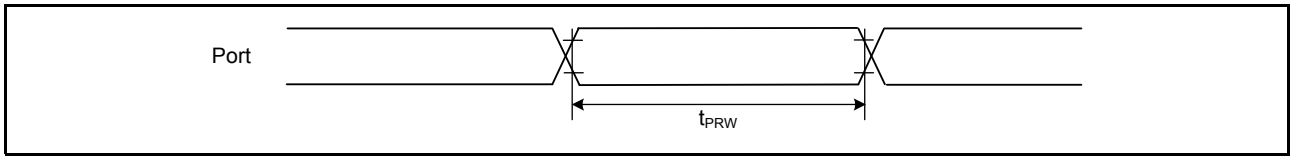


Figure 2.30 I/O ports input timing

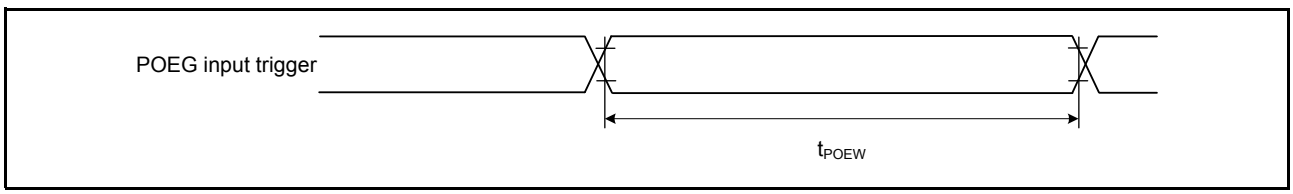


Figure 2.31 POEG input trigger timing

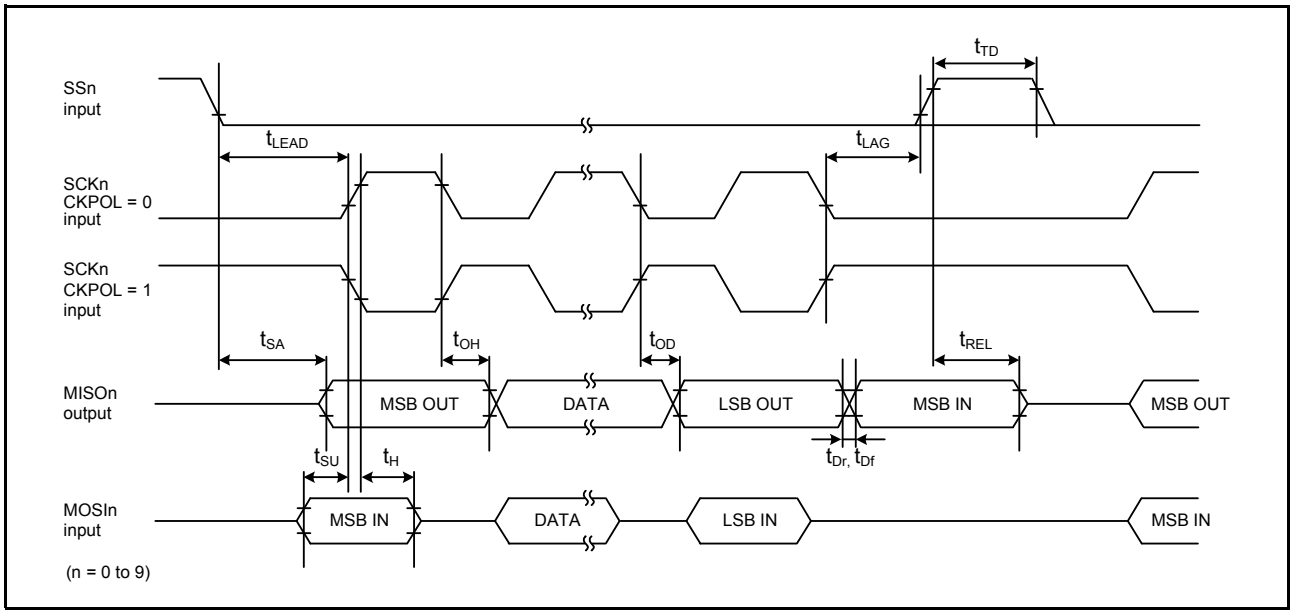


Figure 2.44 SCI simple SPI mode timing for slave when CKPH = 1

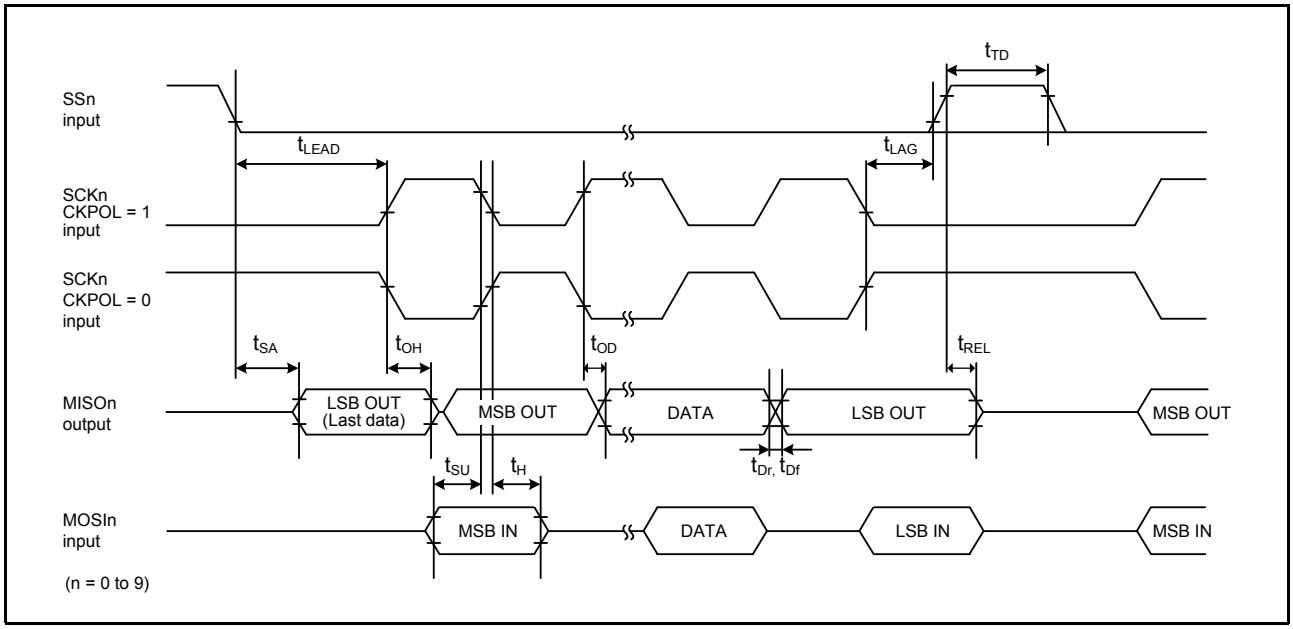


Figure 2.45 SCI simple SPI mode timing for slave when CKPH = 0

Table 2.24 SCI timing (3) (1 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 2.46
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Table 2.24 SCI timing (3) (2 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 2.46
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_{b}*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKA cycle.
Note 1. Cb indicates the total capacity of the bus line.

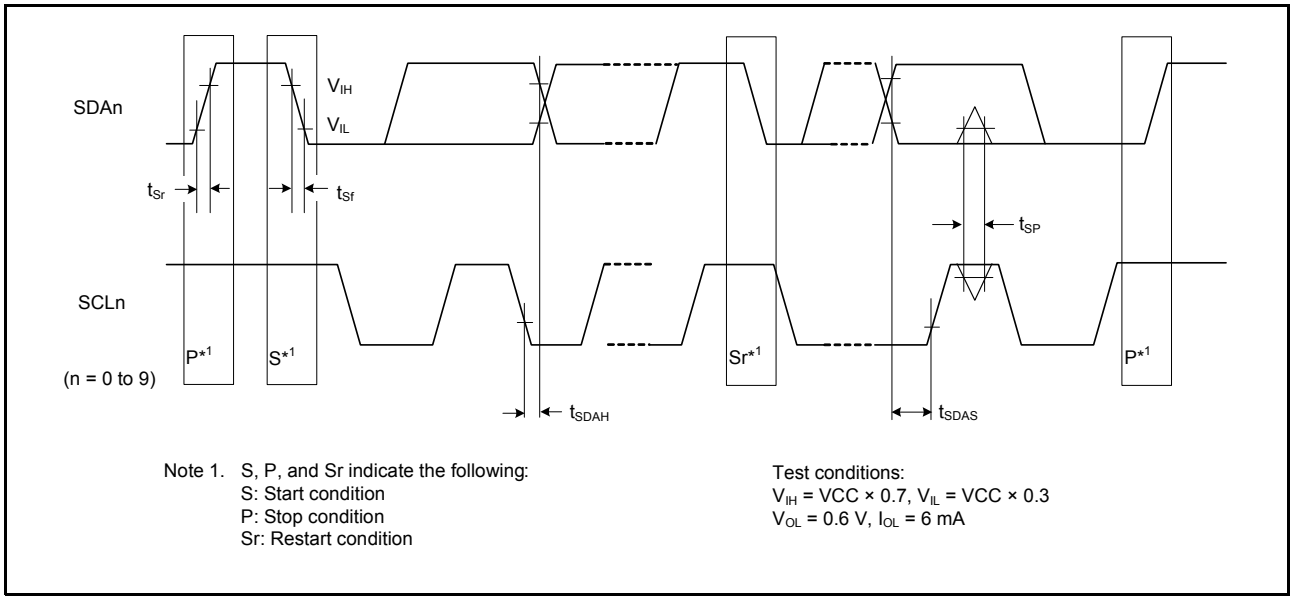


Figure 2.46 SCI simple IIC mode timing

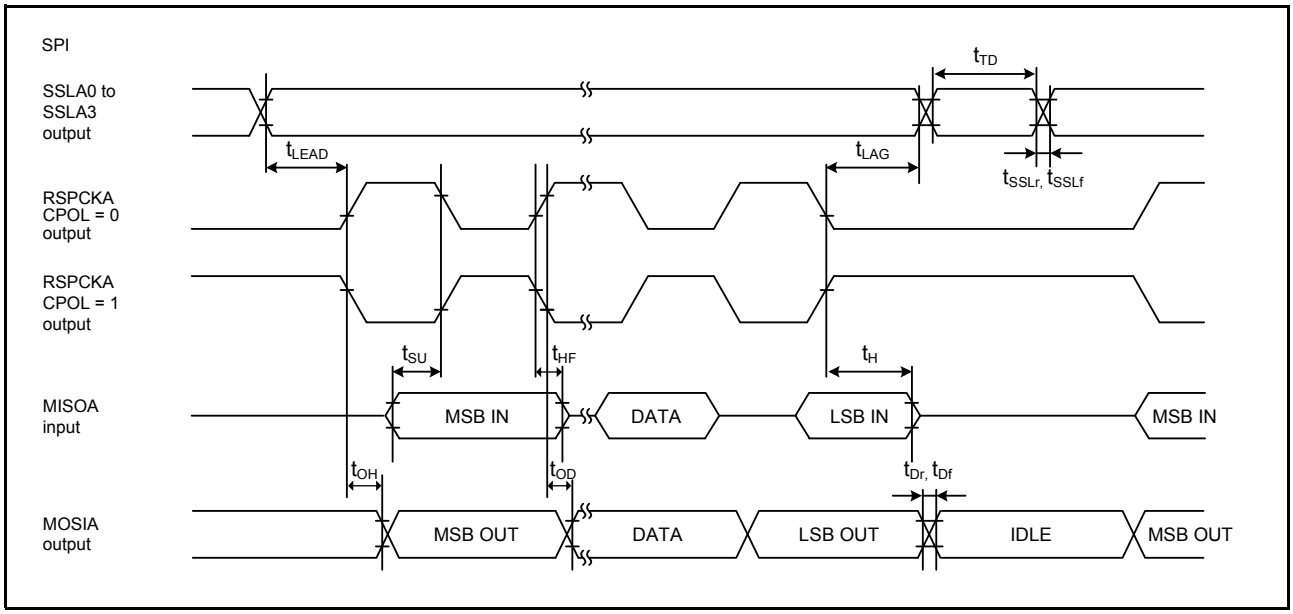


Figure 2.51 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

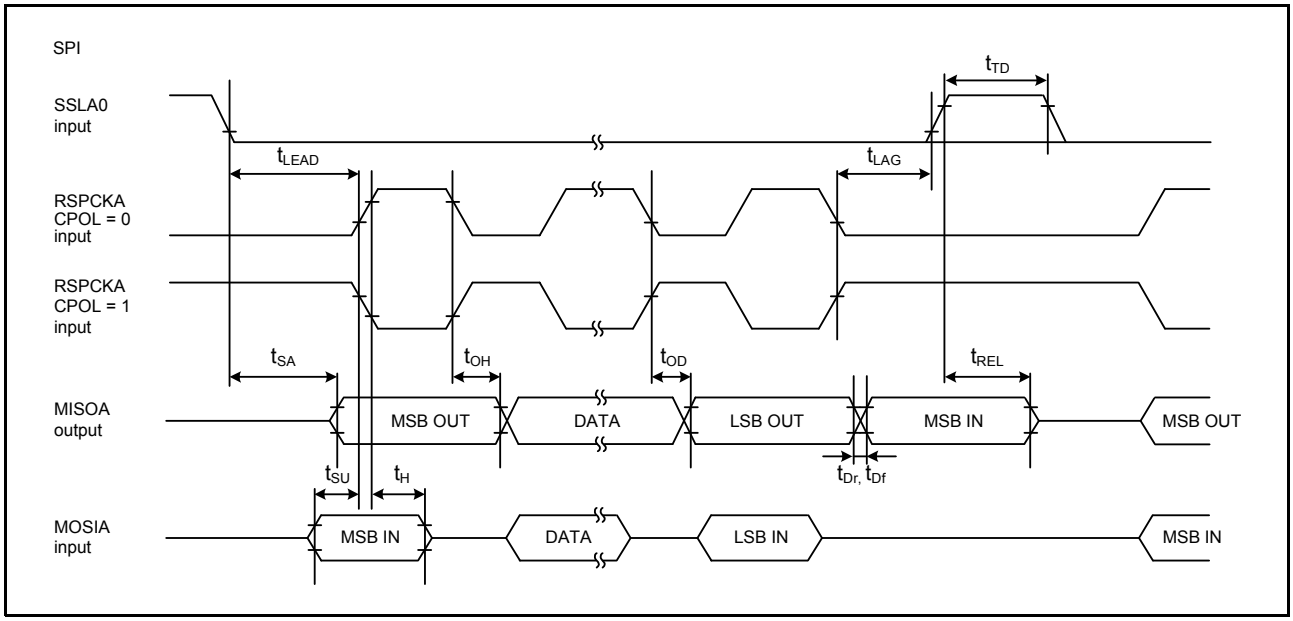


Figure 2.52 SPI timing for slave when CPHA = 0

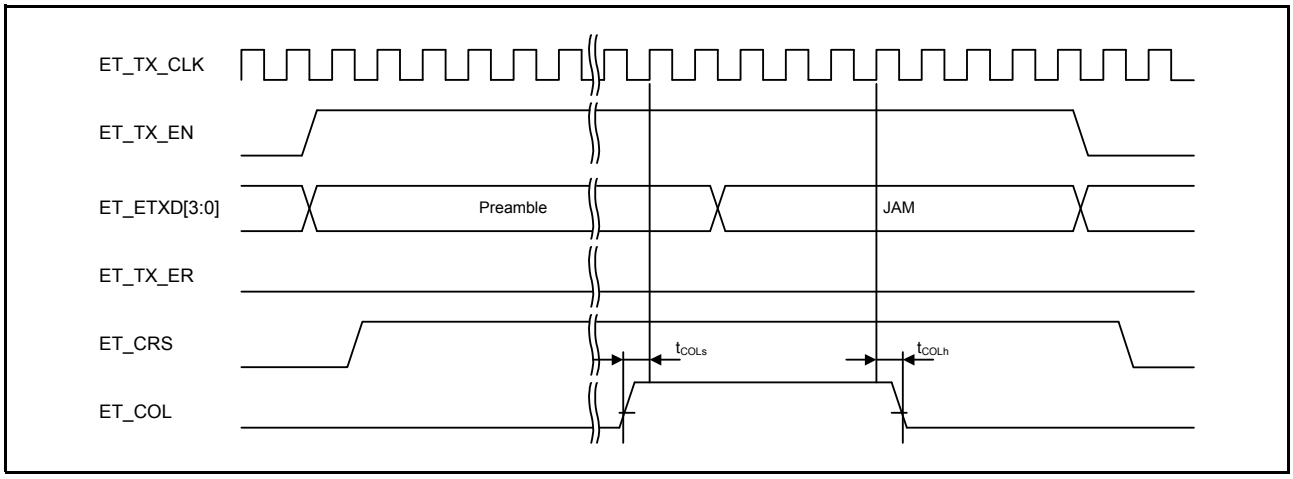


Figure 2.69 MII transmission timing when a conflict occurs

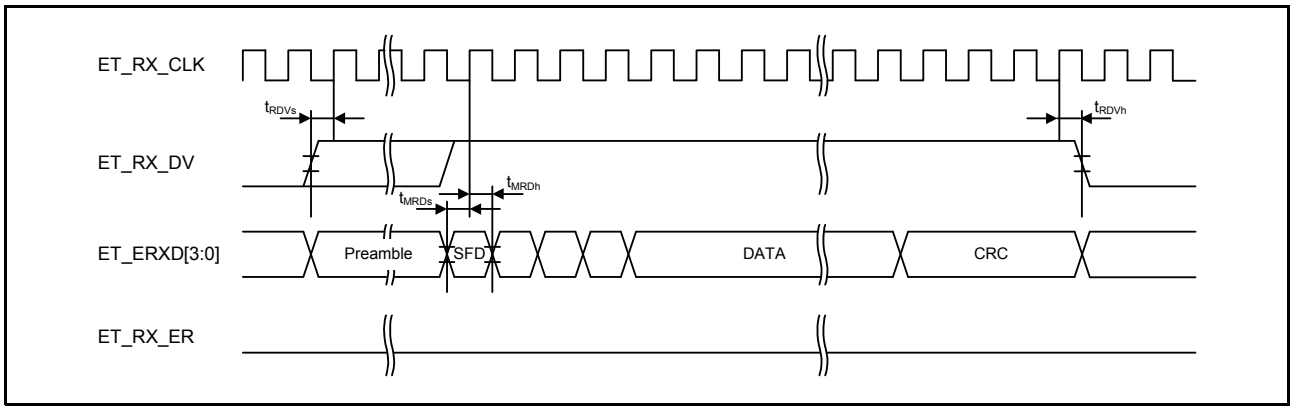


Figure 2.70 MII reception timing in normal operation

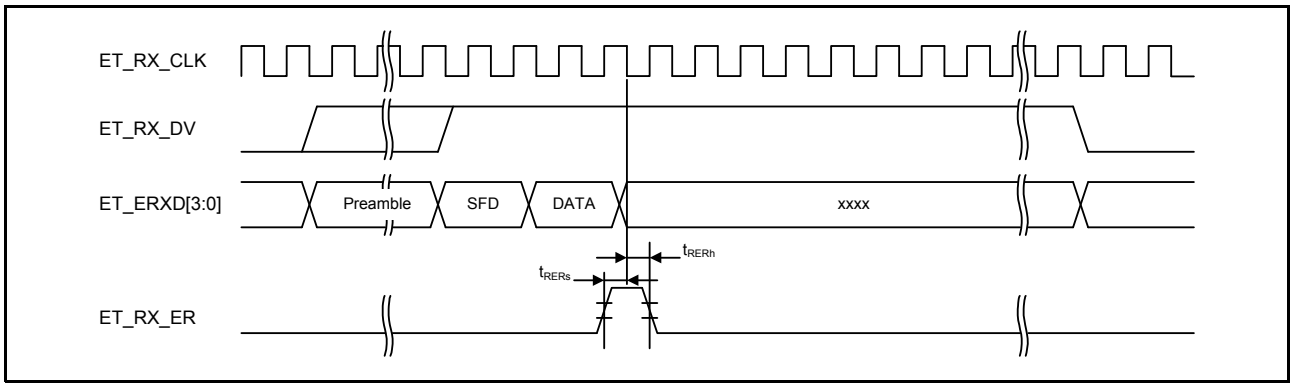


Figure 2.71 MII reception timing when an error occurs

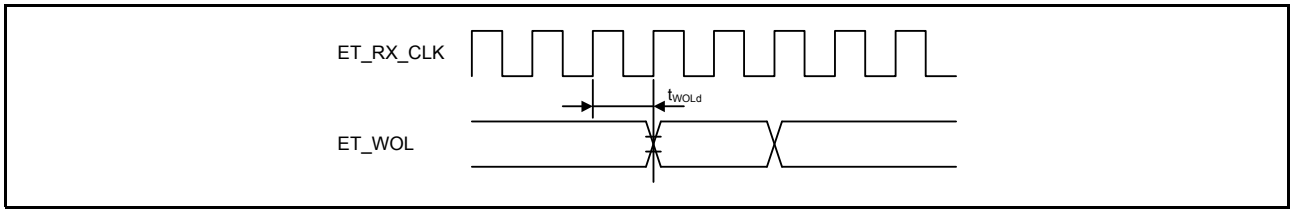


Figure 2.72 WOL output timing for MII

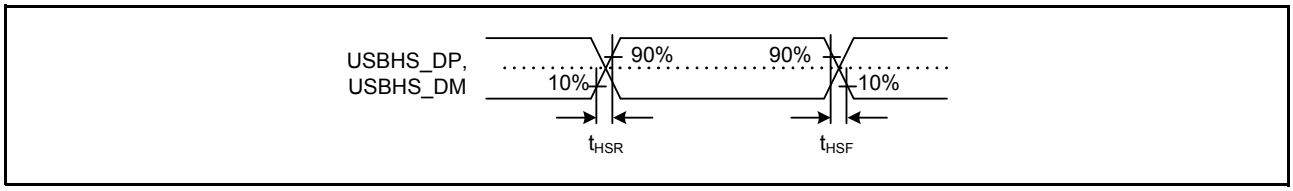


Figure 2.85 USBHS_DP and USBHS_DM output timing in high-speed mode

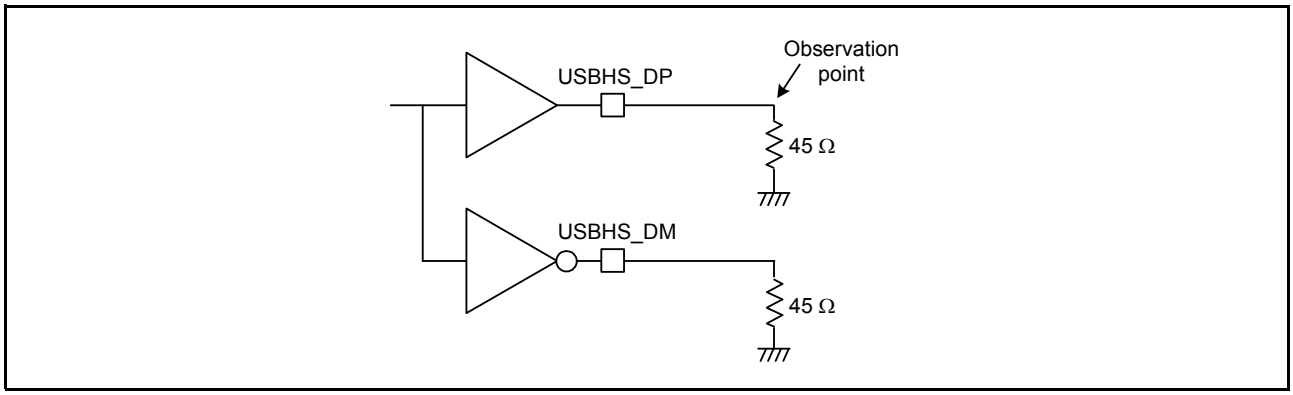


Figure 2.86 Test circuit in high-speed mode

Table 2.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Item		Symbol	Min	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	175	µA	-
	D– sink current	I_{DM_SINK}	25	175	µA	-
	DCD source current	I_{DP_SRC}	7	13	µA	-
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA
	D– source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA

2.4.2 USBFS Timing

Table 2.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Item		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = –200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 2.87
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

2.6 DAC12 Characteristics

Table 2.44 D/A conversion characteristics

Item	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH – 0.2	V	-

2.7 TSN Characteristics

Table 2.45 TSN characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

2.8 OSC Stop Detect Characteristics

Table 2.46 Oscillation stop detection circuit characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 2.92

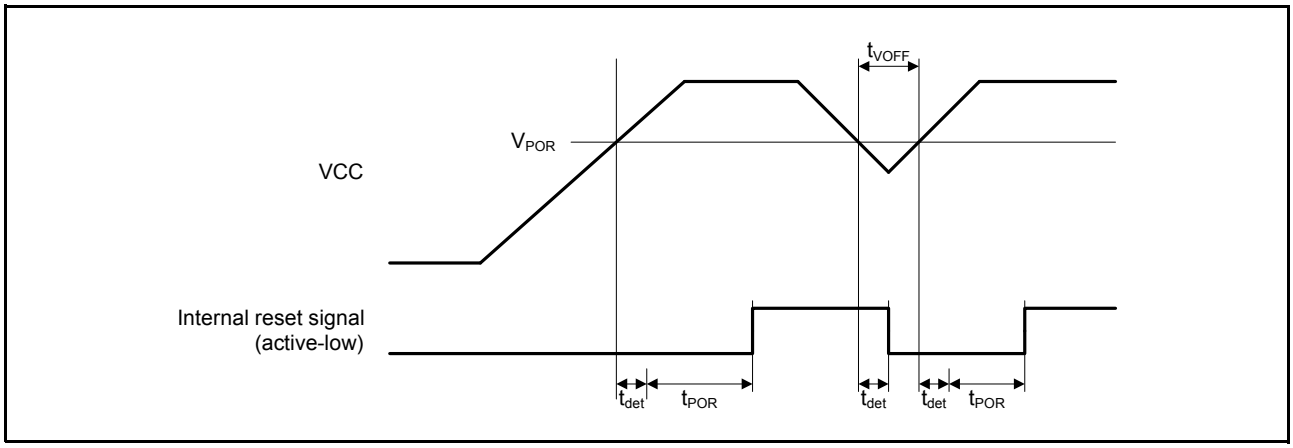


Figure 2.93 Power-on reset timing

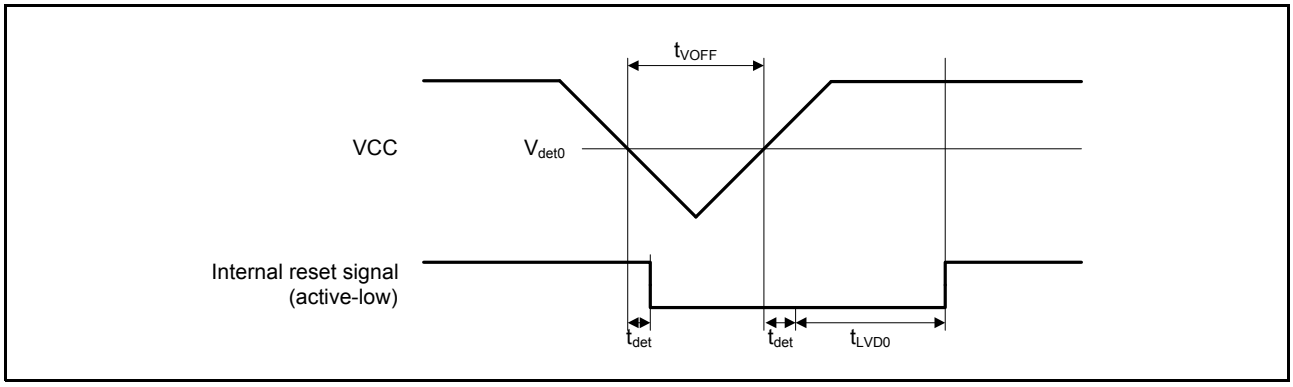


Figure 2.94 Voltage detection circuit timing (V_{det0})

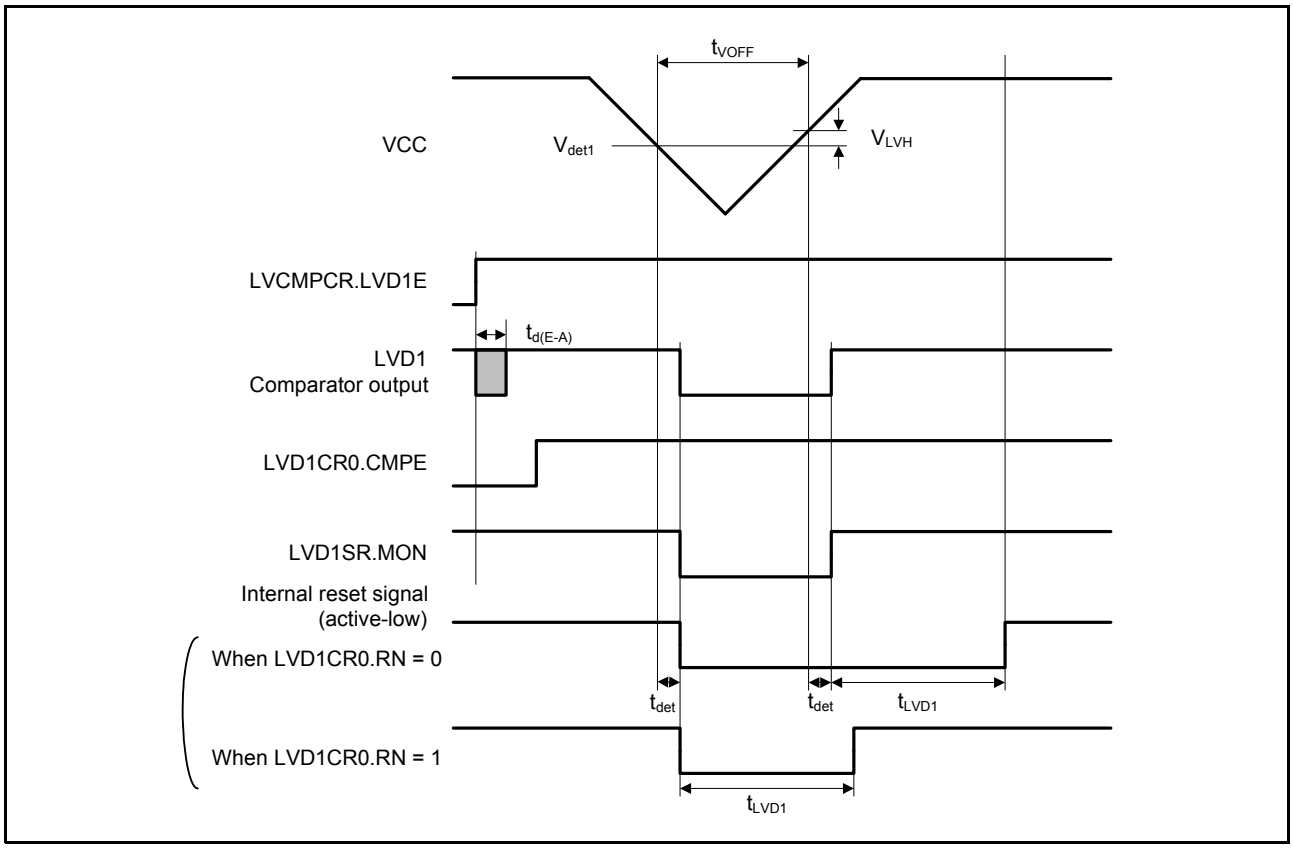


Figure 2.95 Voltage detection circuit timing (V_{det1})

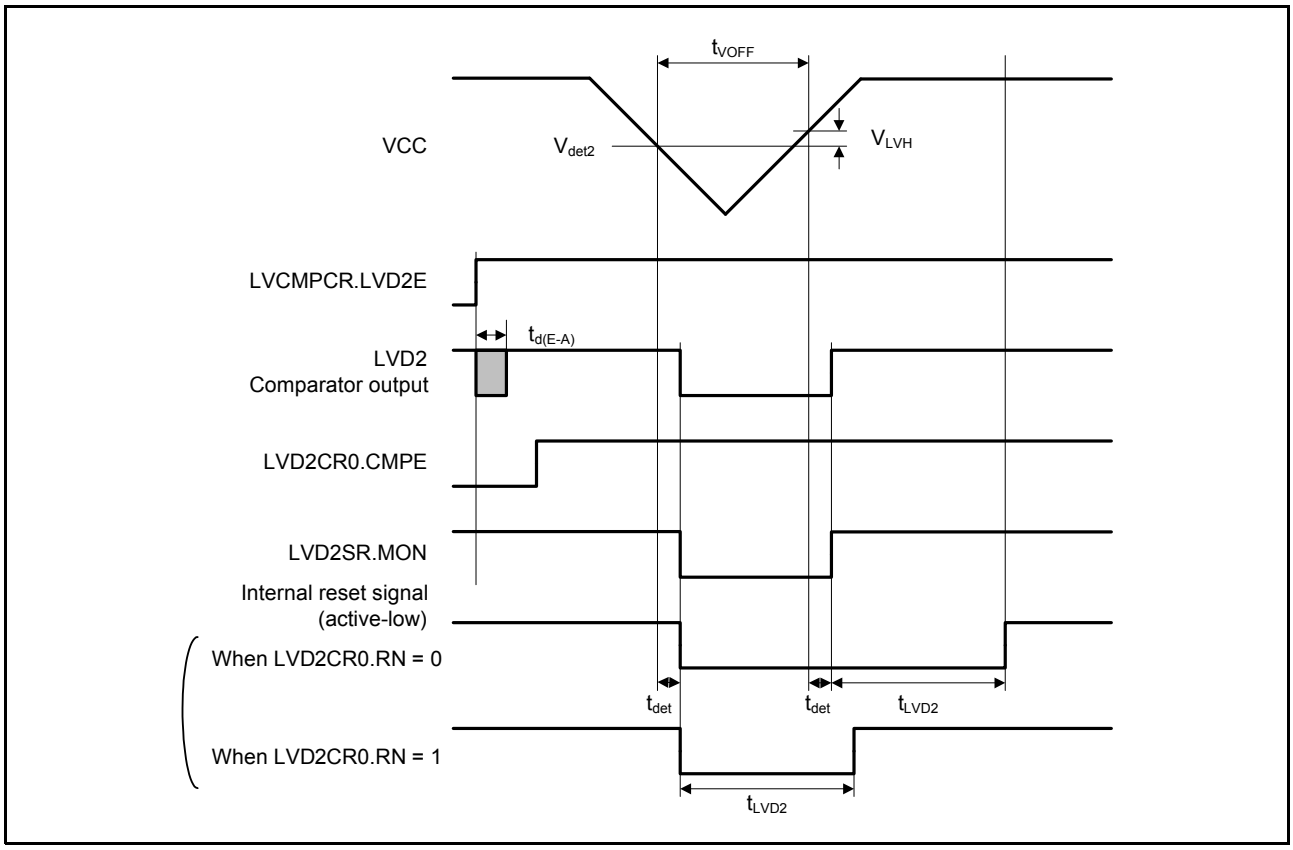


Figure 2.96 Voltage detection circuit timing (V_{det2})

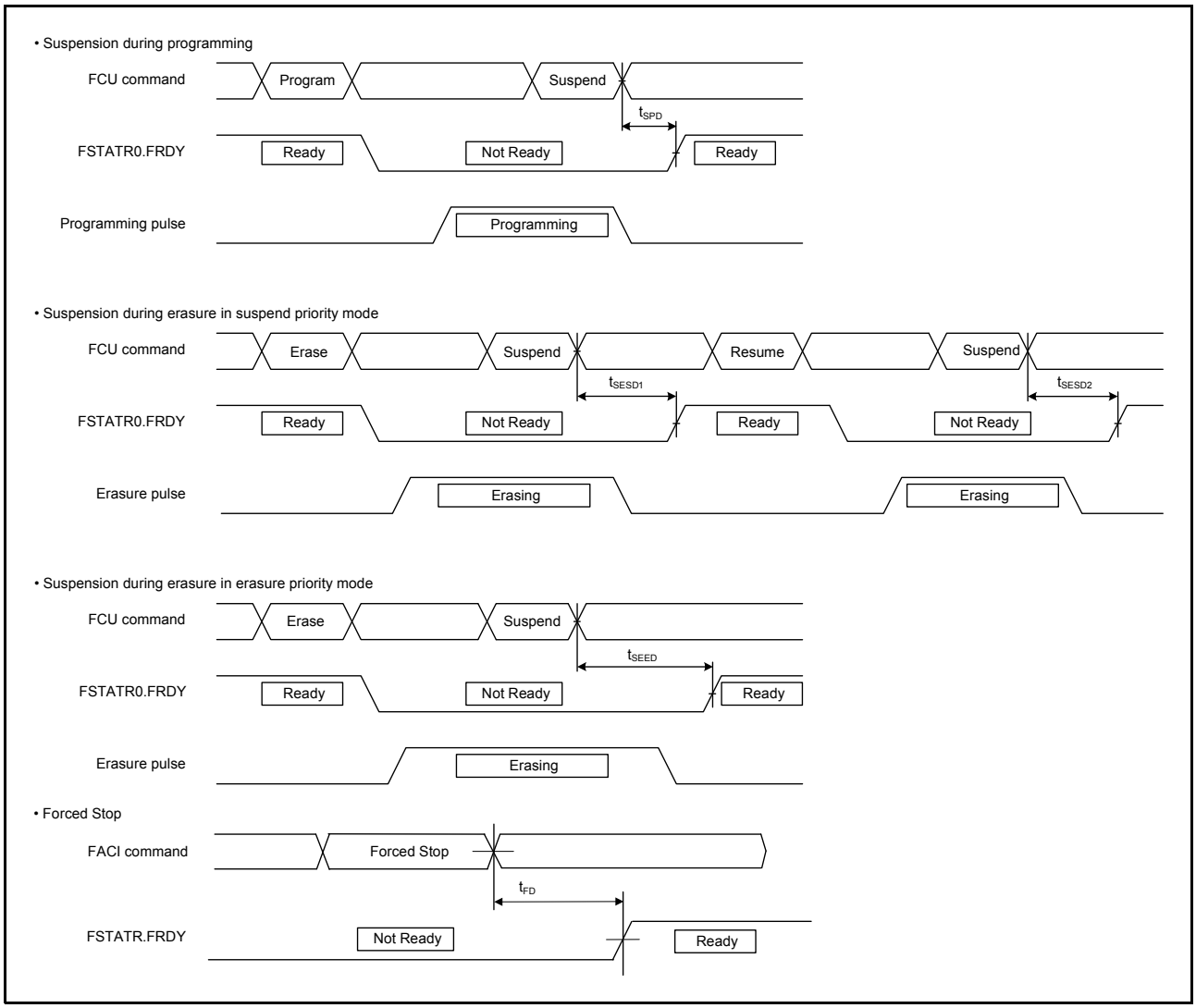


Figure 2.98 Suspension and forced stop timing for flash memory programming and erasure

2.14.2 Data Flash Memory Characteristics

Table 2.54 Data flash memory characteristics (1 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.46	3.8	-	0.21	1.7	ms	
	8-byte	t_{DP8}	-	0.48	4.0	-	0.22	1.8		
	16-byte	t_{DP16}	-	0.53	4.5	-	0.24	2.0		
Erasure time	64-byte	t_{DE64}	-	4.03	18	-	2.24	10	ms	
	128-byte	t_{DE128}	-	6.2	27	-	3.4	15		
	256-byte	t_{DE256}	-	11.6	50	-	6.4	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

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