Renesas Electronics America Inc - R7FS5D97C3A01CFB#AA0 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	110
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LFQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d97c3a01cfb-aa0

Table 1.3 System (2 of 3)

Feature	Functional description
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor reset 0 • Voltage monitor reset 1 • Voltage monitor reset 2 • Independent Watchdog Timer reset • Watchdog Timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected in the software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer (WDT) on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The ICU controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low-power modes	Power consumption can be reduced in multiple ways, including by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low-power modes. See section 11, Low-Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four MPUs and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The WDT is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.

Table 1.11 Graphics

Feature	Functional description
Graphics LCD Controller (GLCDC)	The GLCDC provides multiple functions and supports various data formats and panels. Key GLCDC features include: • GPX bus master function for accessing graphics data • Superimposition of three planes (single color background plane, graphic 1 plane, and graphic 2 plane) • Support for many types of 32- or 16-bit per pixel graphics data and 8-, 4-, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. See section 58, Graphics LCD Controller (GLCDC) in User's Manual.
2D Drawing Engine (DRW)	The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW) in User's Manual.
JPEG Codec (JPEG)	The JPEG Codec (JPEG) incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec (JPEG) in User's Manual.
Parallel Data Capture Unit (PDC)	One PDC unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC) in User's Manual.

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The CRC calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator in User's Manual.
Data Operation Circuit (DOC)	The DOC compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC) in User's Manual.
Sampling Rate Converter (SRC)	The SRC converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC) in User's Manual.

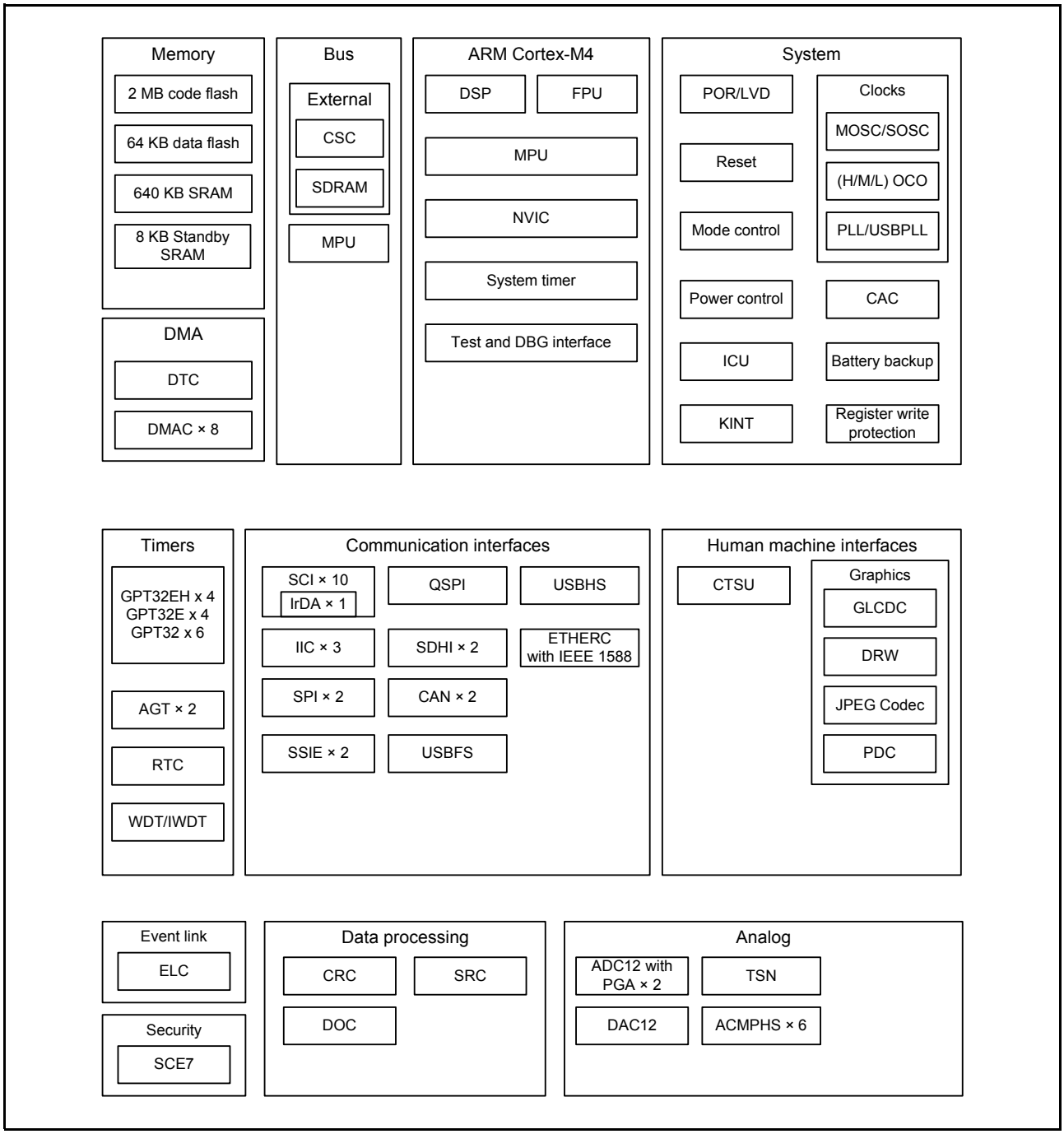


Figure 1.1 Block diagram

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Digital voltage supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect to the system power supply. Connect to VSS through a 0.1-µF smoothing capacitor close to each VCC pin.
	VCL0	-	Connect to VSS through a 0.1-µF smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ15	Input	Maskable interrupt request pins.
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins.
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TDATA0 to TDATA3	Output	Trace data output.
	SWDIO	I/O	Serial wire debug data input/output pin.
	SWCLK	Input	Serial wire clock pin.
	SWO	Output	Serial wire trace output pin.
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active low.
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active low.
	WR0 to WR1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active low.
	BC0 to BC1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active low.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT	Input	Input pin for wait request signals in access to the external space, active low.
	CS0 to CS7	Output	Select signals for CS areas, active low.
	A00 to A23	Output	Address bus.
	D00 to D15	I/O	Data bus.
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus.

Table 1.16 Pin functions (5 of 5)

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	Input pins for the analog signals to be processed by the ADC12.
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion.
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	Differential input pins.
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter.
ACMPHS	VCOUT	Output	Comparator output pin.
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator.
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator.
CTSU	TS00 to TS17	Input	Capacitive touch detection pins (touch pins).
	TSCAP	-	Secondary power supply pin for the touch driver.
I/O ports	P000 to P007	Input	General-purpose input pins.
	P008 to P010, P014, P015	I/O	General-purpose input/output pins.
	P100 to P115	I/O	General-purpose input/output pins.
	P200	Input	General-purpose input pin.
	P201 to P214	I/O	General-purpose input/output pins.
	P300 to P315	I/O	General-purpose input/output pins.
	P400 to P415	I/O	General-purpose input/output pins.
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins.
	P600 to P615	I/O	General-purpose input/output pins.
	P700 to P713	I/O	General-purpose input/output pins.
	P800 to P806	I/O	General-purpose input/output pins.
	P900, P901, P905 to P908	I/O	General-purpose input/output pins.
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins.
	PB00, PB01	I/O	General-purpose input/output pins.
GLCDC	LCD_DATA23 to LCD_DATA00	Output	Data output pins for panel.
	LCD_TCON3 to LCD_TCON0	Output	Output pins for panel timing adjustment.
	LCD_CLK	Output	Panel clock output pin.
	LCD_EXTCLK	Input	Panel clock source input pin.
PDC	PIXCLK	Input	Image transfer clock pin.
	VSYNC	Input	Vertical synchronization signal pin.
	HSYNC	Input	Horizontal synchronization signal pin.
	PIXD0 to PIXD7	Input	8-bit image data pins.
	PCKO	Output	Output pin for dot clock.

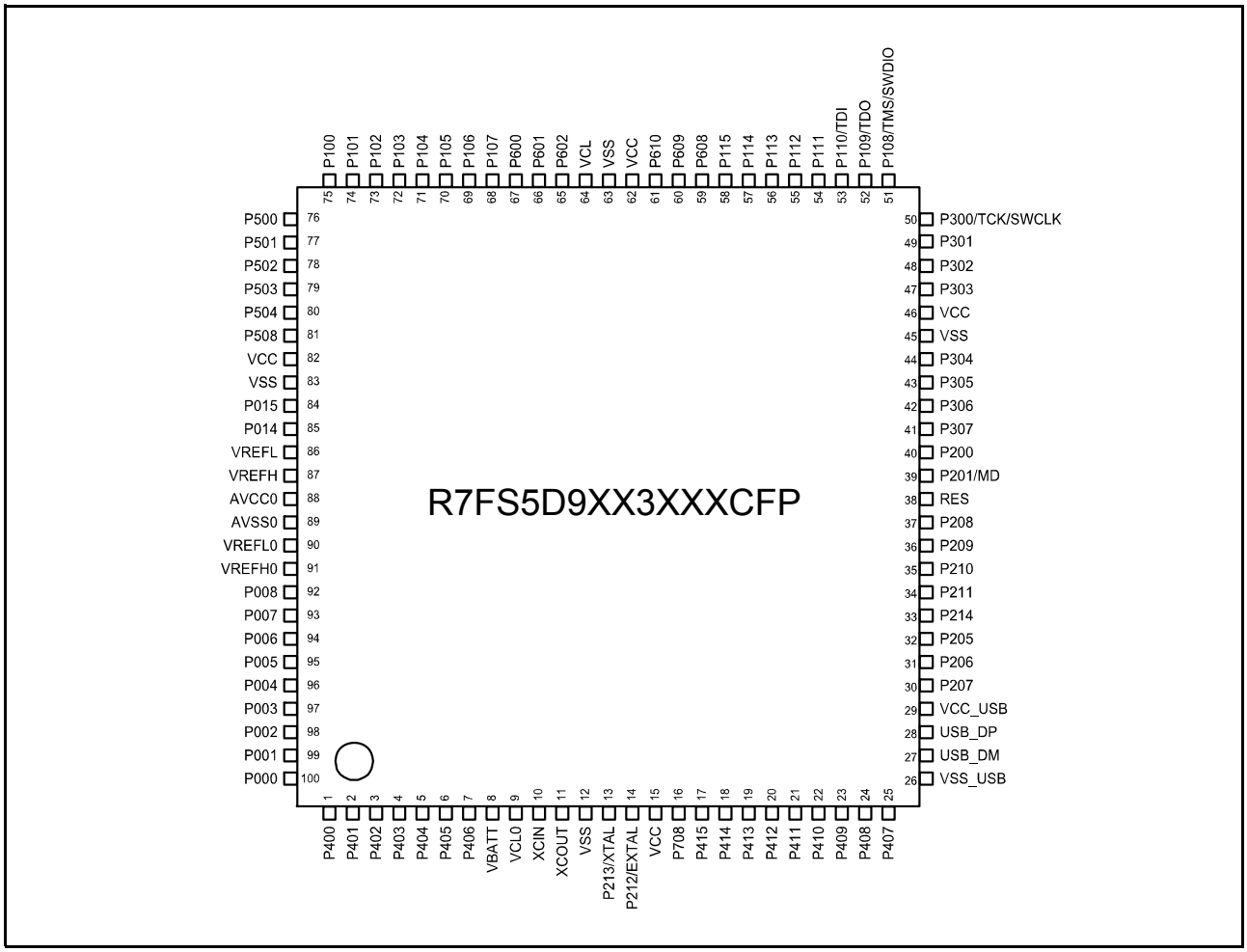


Figure 1.7 Pin assignment for 100-pin LQFP (top view)

1.7 Pin Lists

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
N13	1	N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_W OL	ET0_ WOL	-	-	ADTRG 1	-	-	-
R15	2	L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_ RTS4/ SS4	TXD7/ MOSI7 /SDA7	SDA0 _A	-	-	ET0_M DC	ET0_M DC	-	-	-	-	-	-
P14	3	M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTC IC0	CRX0	-	RXD7/ MISO7 /SCL7	-	-	AUDIO _CLK	ET0_M DIO	ET0_M DIO	-	-	-	-	-	VSYNC
M12	4	K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTC IC1	-	-	CTS7_ RTS7/ SS7	-	-	SSIBC K0_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD1 DAT7 _B	-	-	-	PIXD7
M13	5	L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTC IC2	-	-	-	-	-	SSILR CK0/S SIFS0_ A	ET0_EX OUT	ET0_E XOUT	-	SD1 DAT6 _B	-	-	-	PIXD6
P15	6	L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX _EN	RMII0_ TXD_E N_B	-	SD1 DAT5 _B	-	-	-	PIXD5
N14	7	J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX _ER	RMII0_ TXD1_ B	-	SD1 DAT4 _B	-	-	-	PIXD4
N15	8	H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ET XD1	RMII0_ TXD0_ B	-	SD1 DAT3 _B	-	-	-	PIXD3
M14	9	K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ET XD0	REF50 CK0_B	-	SD1 DAT2 _B	-	-	-	PIXD2
L12	10	K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ER XD1	RMII0_ RXD0_ B	-	SD1 DAT1 _B	-	-	-	PIXD1
M15	11	J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ER XD0	RMII0_ RXD1_ B	-	SD1 DAT0 _B	-	VCOUT	-	PIXD0
L13	12	H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	SSLB1 _C	-	ET0_RX _CLK	RMII0_ RX_E R_B	-	SD1 CLK_ B	-	-	-	HSYNC
K12	13	G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	SSLB2 _C	-	ET0_C RS	RMII0_ CRS_ DV_B	-	SD1 CMD _B	-	-	-	PIXCLK
L14	14	-	-	-	-	IRQ7	P706	-	-	-	-	-	-	-	-	RXD3/ MISO3 /SCL3	-	-	-	-	-	USB HS_ OVR CUR B	SD1 CD_ B	-	-	-	-
L15	15	-	-	-	-	IRQ8	P707	-	-	-	-	-	-	-	-	TXD3/ MOSI3 /SDA3	-	-	-	-	-	USB HS_ OVR CUR A	SD1 WP_ B	-	-	-	-
J12	16	-	-	-	-	-	PB00	-	-	-	-	-	-	-	-	SCK3	-	-	-	-	-	USB HS_ VBU SEN	-	-	-	-	-
K13	17	-	-	-	-	-	PB01	-	-	-	-	-	-	-	-	CTS3_ RTS3/ SS3	-	-	-	-	-	USB HS_ VBU S	-	-	-	-	-
K14	18	J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K15	19	J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J15	20	H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J14	21	H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	22	F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H14	23	G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	-	-	-	ADTRG 1	-	-	-
H15	24	G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/ MISO1 /SCL1	-	-	-	-	-	-	-	-	-	-	-
H12	25	F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	26	-	-	-	AVCC_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G13	27	-	-	-	USBHS_ RREF	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G14	28	-	-	-	AVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G15	29	-	-	-	PVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	30	-	-	-	VSS2_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F15	31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DM	-	-	-	-	-
F14	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DP	-	-	-	-	-
F12	33	-	-	-	VSS1_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F13	34	-	-	-	VCC_US BHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E15	35	-	-	-	-	-	P708	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

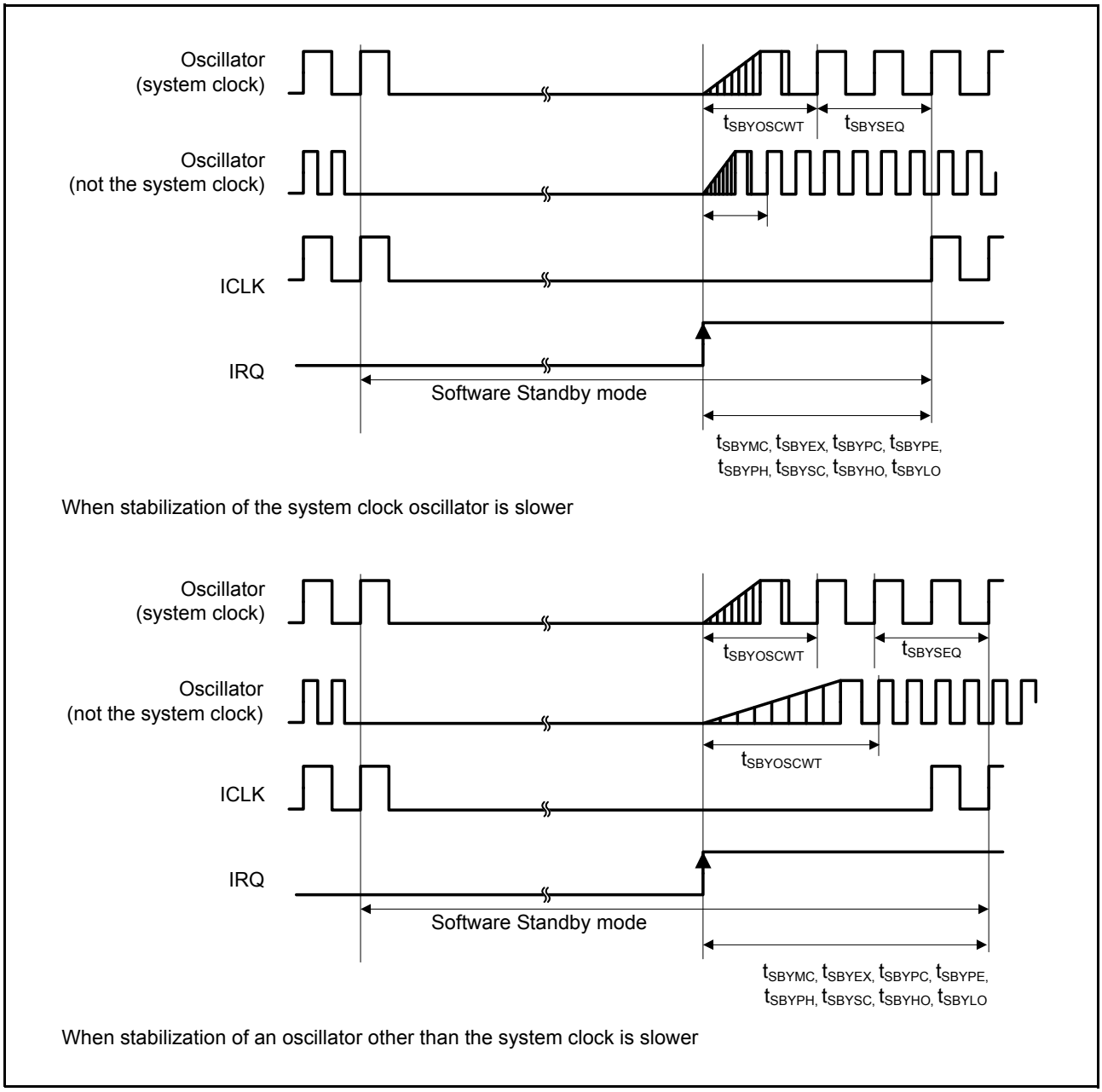


Figure 2.11 Software Standby mode cancellation timing

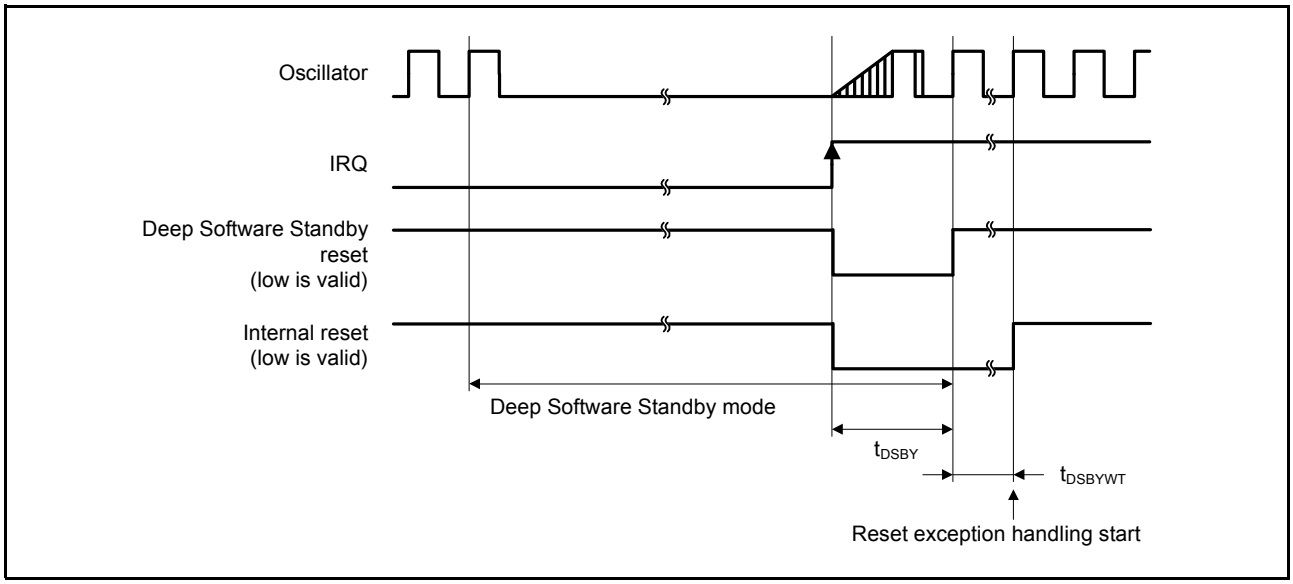


Figure 2.12 Deep Software Standby mode cancellation timing

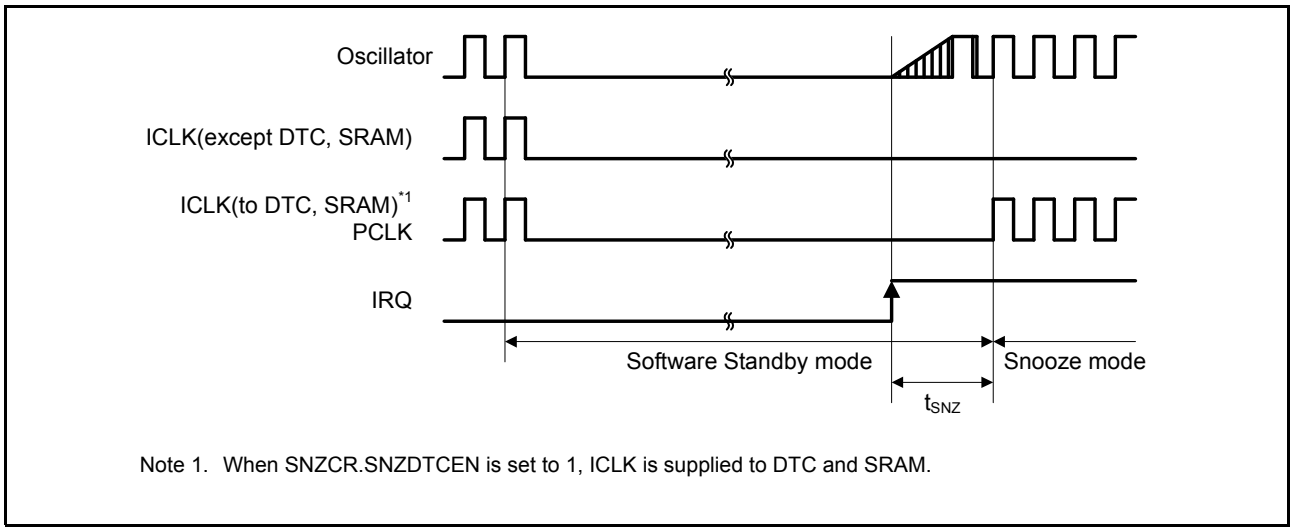


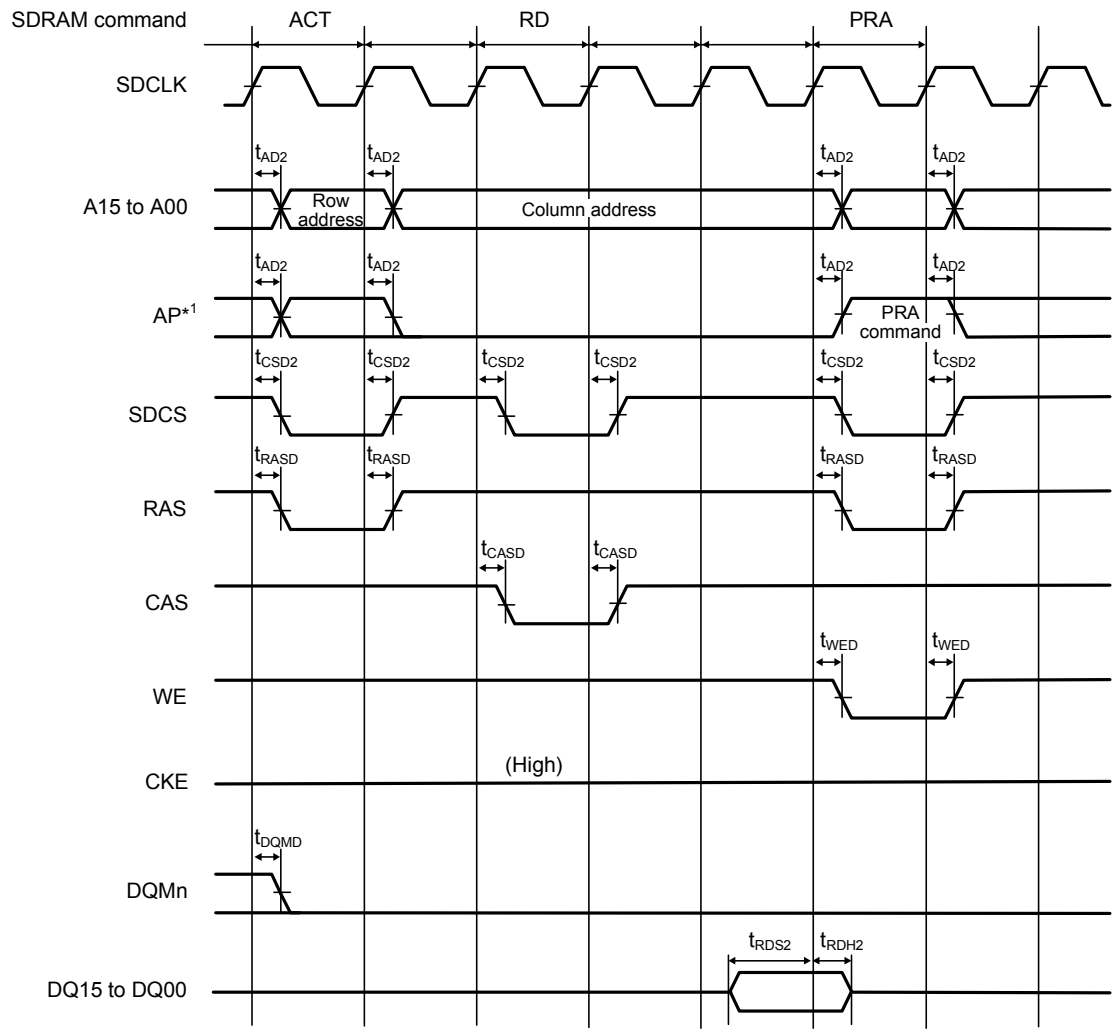
Figure 2.13 Recovery timing from Software Standby mode to Snooze mode

2.3.5 NMI and IRQ Noise Filter

Table 2.17 NMI and IRQ noise filter

Item	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the PCLKB cycle.



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.23 SDRAM single read timing

2.3.11 SPI Timing

Table 2.25 SPI timing
Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 2.47 C = 30 pF
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKR} - t_{SPCKF}) / 2 - 3$	-	ns	
		Slave		$2 \times t_{Pcyc}$	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 2.48 to Figure 2.53 C = 30 pF
		Slave		5	-		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL setup time	Master	t_{LEAD}	$N \times t_{SPcyc}$ - 10*3	$N \times t_{SPcyc}$ + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL hold time	Master	t_{LAG}	$N \times t_{SPcyc}$ - 10 *4	$N \times t_{SPcyc}$ + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	Data output delay	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave		$6 \times t_{Pcyc}$			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	2 x t_{Pcyc} + 28	ns	Figure 2.52 and Figure 2.53 C = 30pF
	Slave output release time		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

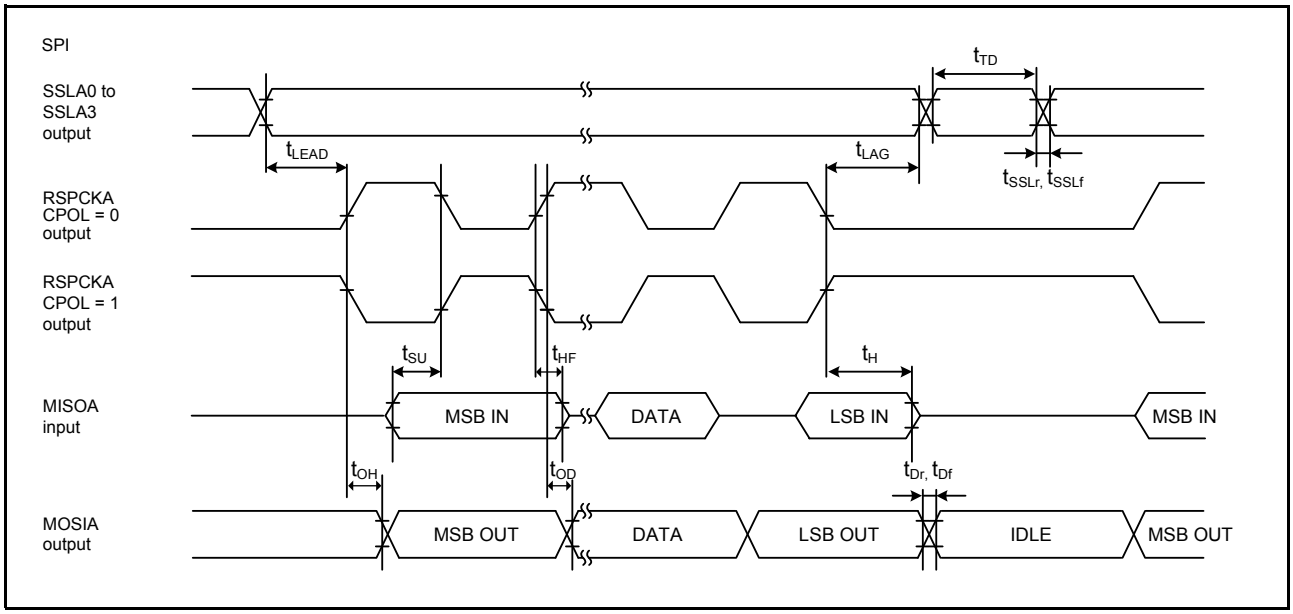


Figure 2.51 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

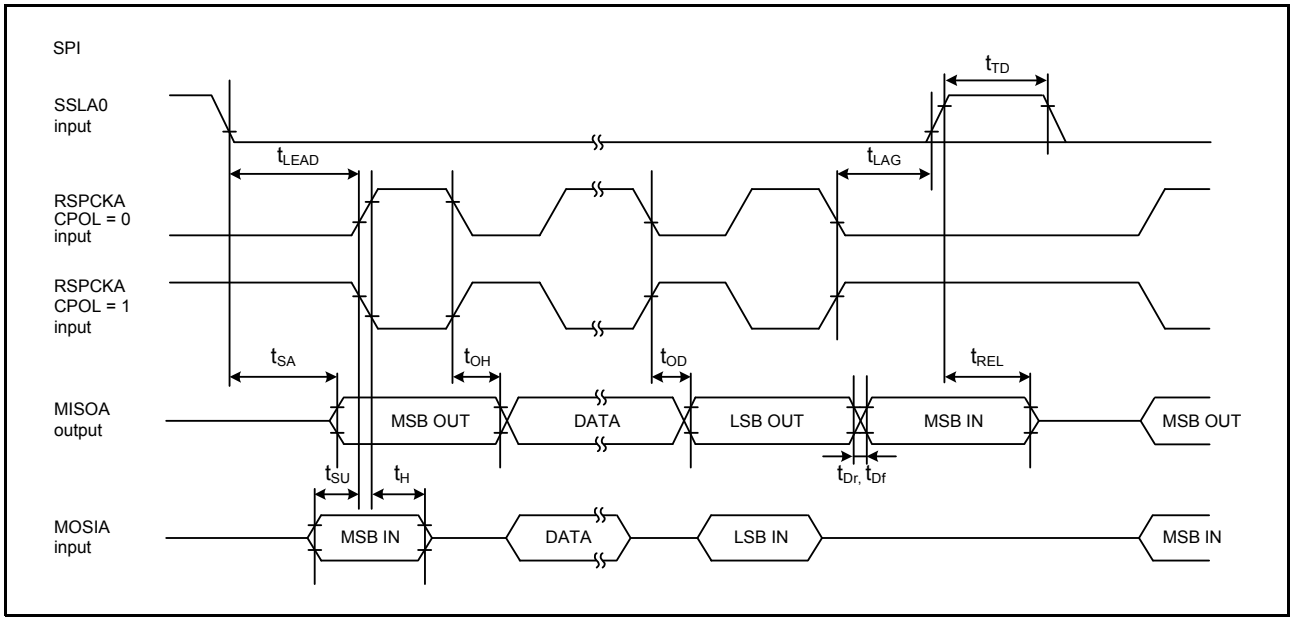


Figure 2.52 SPI timing for slave when CPHA = 0

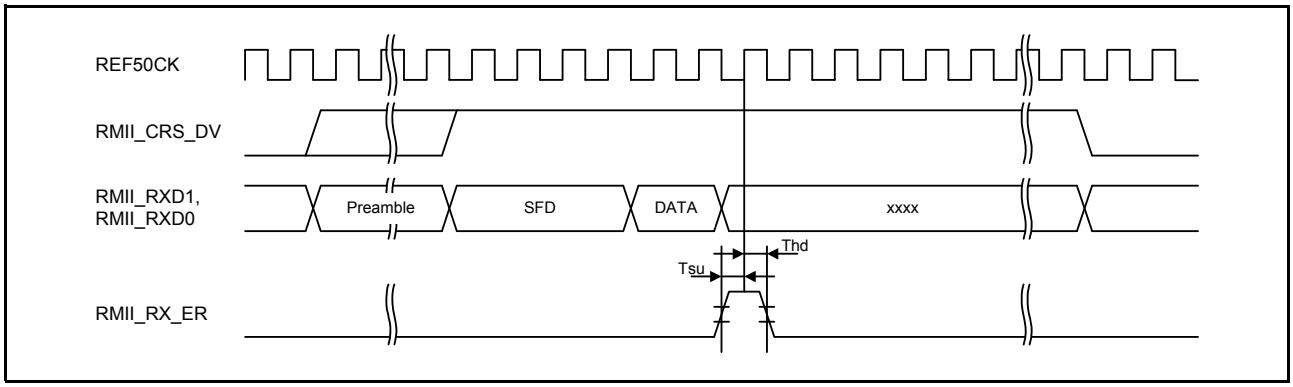


Figure 2.66 RMII reception timing when an error occurs

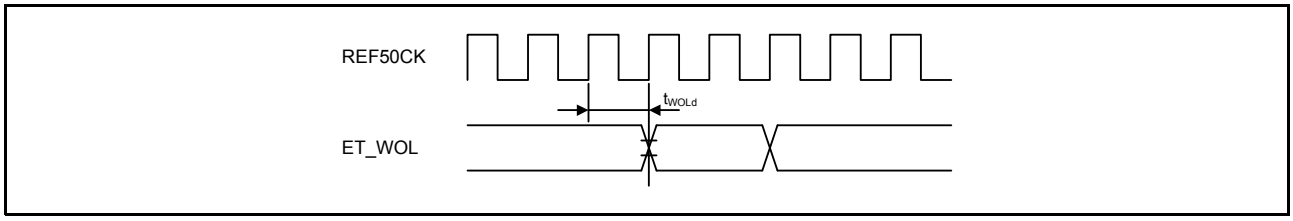


Figure 2.67 WOL output timing for RMII

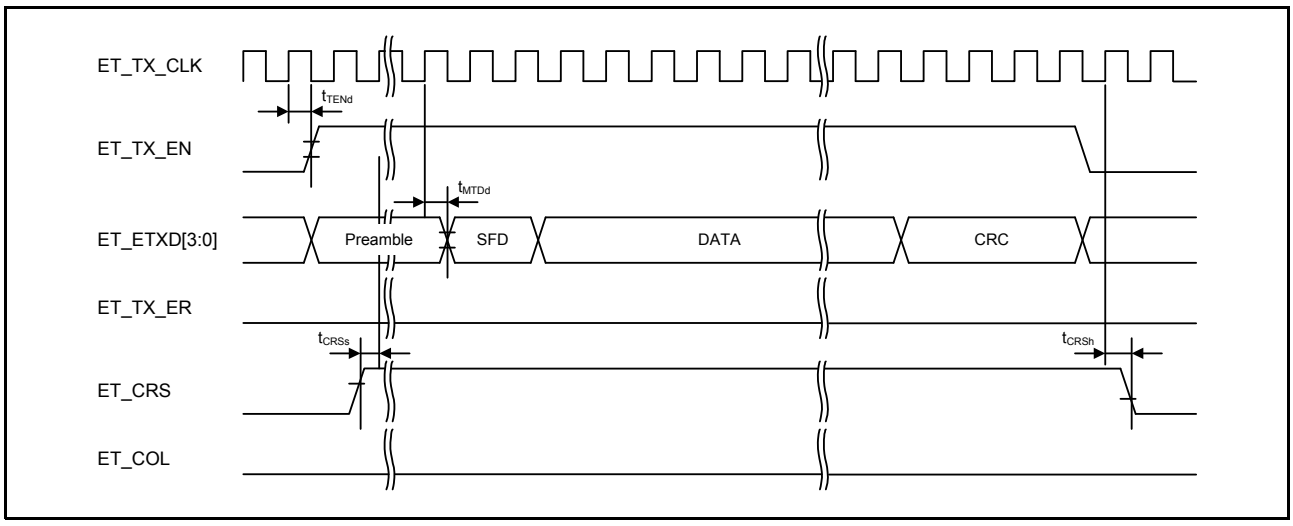


Figure 2.68 MII transmission timing in normal operation

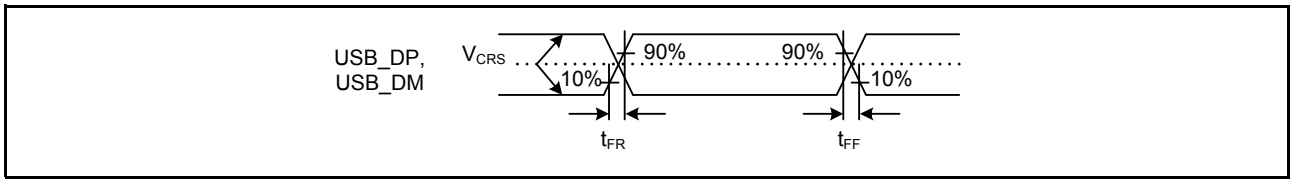


Figure 2.89 USB_DP and USB_DM output timing in full-speed mode

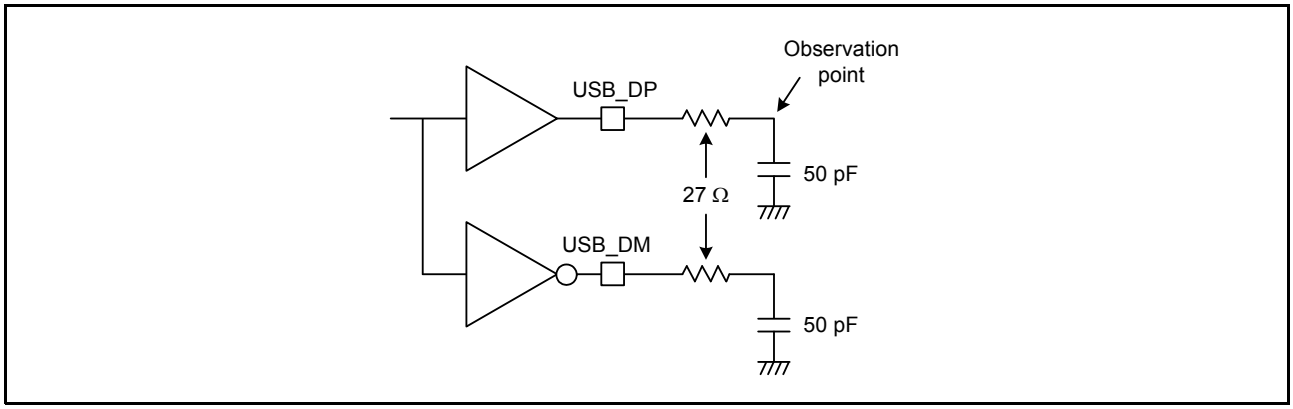


Figure 2.90 Test circuit in full-speed mode

2.5 ADC12 Characteristics

[Normal-precision channel]

Table 2.40 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH 0 – 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-

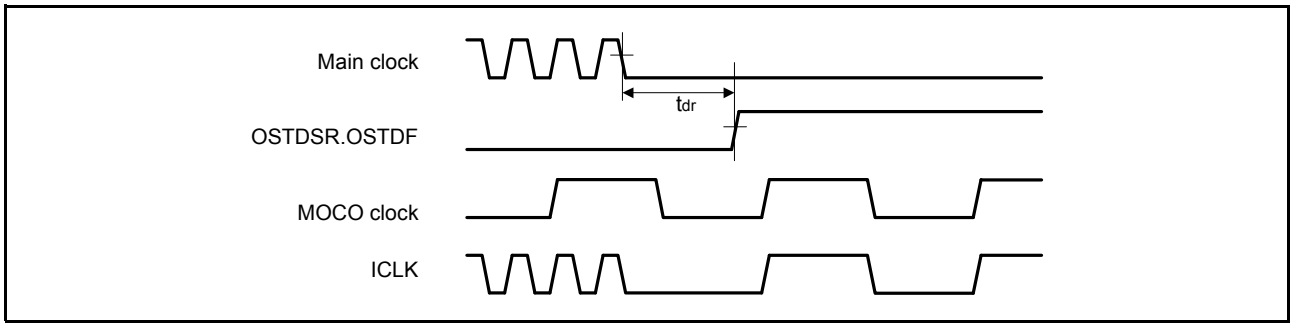


Figure 2.92 Oscillation stop detection timing

2.9 POR and LVD Characteristics

Table 2.47 Power-on reset circuit and voltage detection circuit characteristics

Item			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	Module-stop function disabled*2	V_{POR}	2.5	2.6	2.7	V	Figure 2.93
		Module-stop function enabled*3		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 2.94
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 2.95
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 2.96
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	-	4.5	-	ms	Figure 2.93
	LVD0 reset time		t_{LVD0}	-	0.51	-		Figure 2.94
	LVD1 reset time		t_{LVD1}	-	0.38	-		Figure 2.95
	LVD2 reset time		t_{LVD2}	-	0.38	-		Figure 2.96
Minimum VCC down time*1			t_{VOFF}	200	-	-	µs	Figure 2.93, Figure 2.94
Response delay			t_{det}	-	-	200	µs	Figure 2.93 to Figure 2.96
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	-	-	10	µs	Figure 2.95, Figure 2.96
Hysteresis width (LVD1 and LVD2)			V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.
Note 2. The low-power function is disabled and DEEPCUT[1:0] = 00b or 01b.
Note 3. The low-power function is enabled and DEEPCUT[1:0] = 11b.

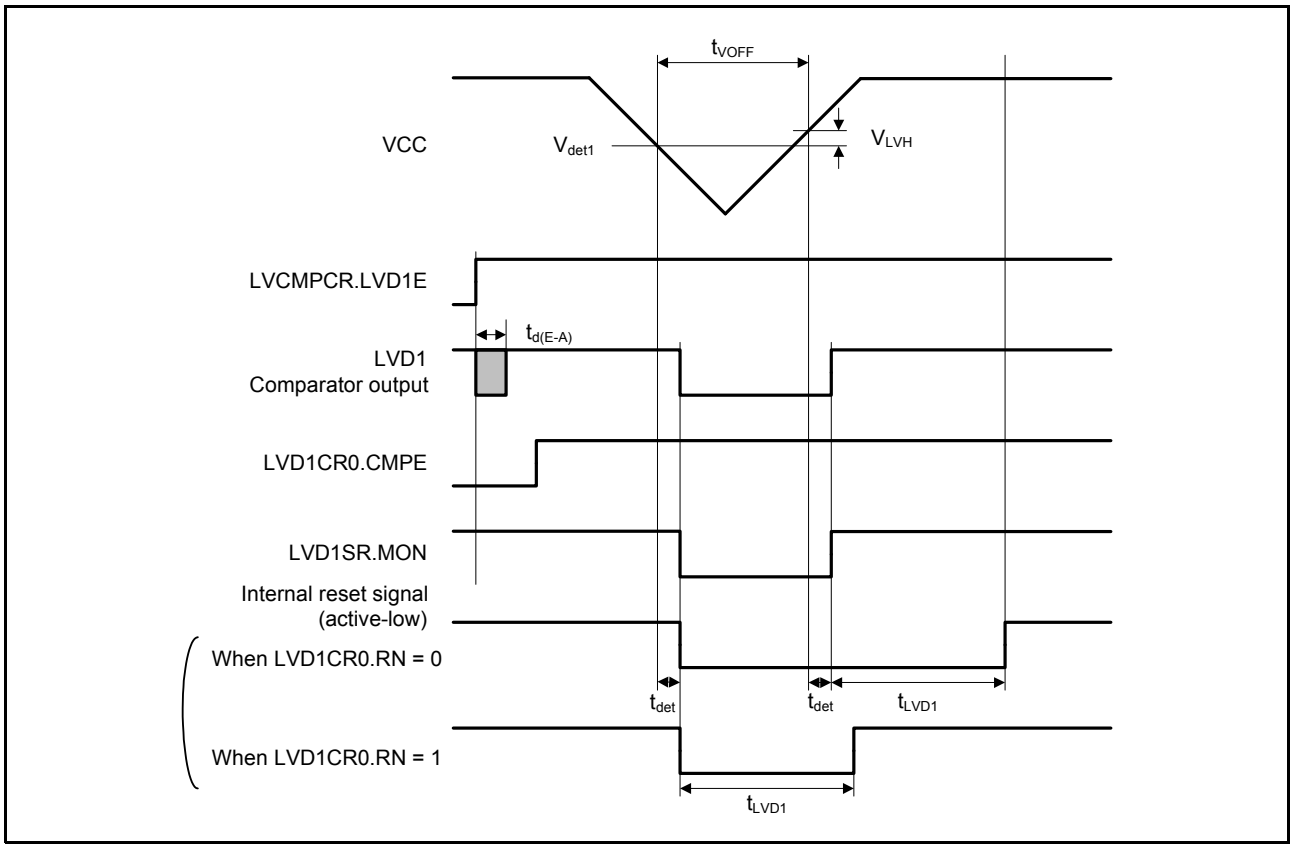


Figure 2.95 Voltage detection circuit timing (V_{det1})

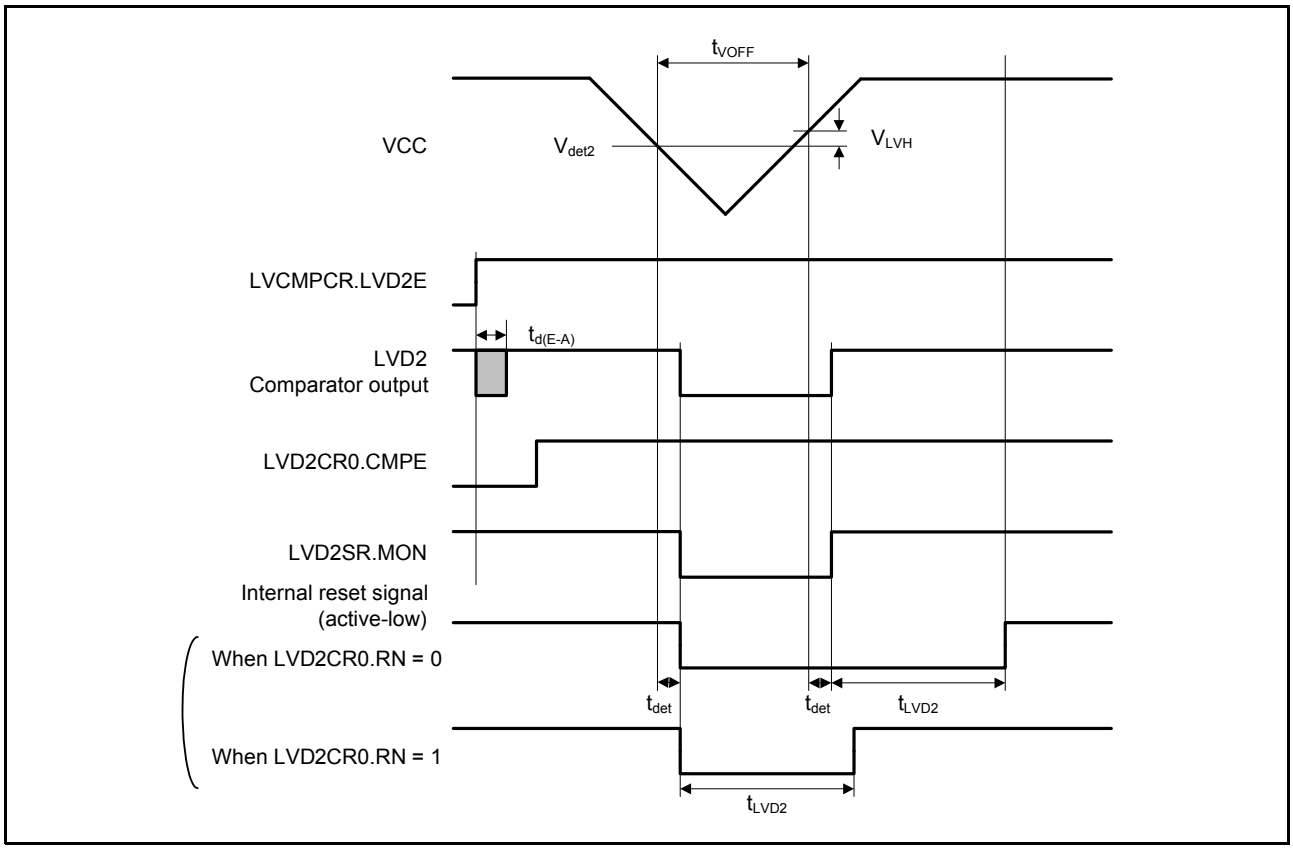


Figure 2.96 Voltage detection circuit timing (V_{det2})

Table 2.54 Data flash memory characteristics (2 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

2.15 Boundary Scan

Table 2.55 Boundary scan characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 2.99
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 2.100
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 2.101

Note 1. Boundary scan does not function until the power-on reset becomes negative.

2.17 Serial Wire Debug (SWD)

Table 2.57 SWD

Item	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 2.104
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 2.105
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

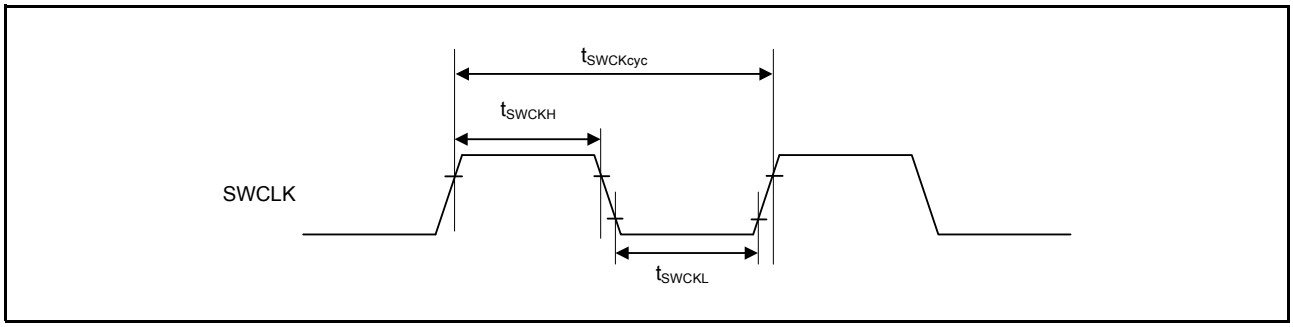
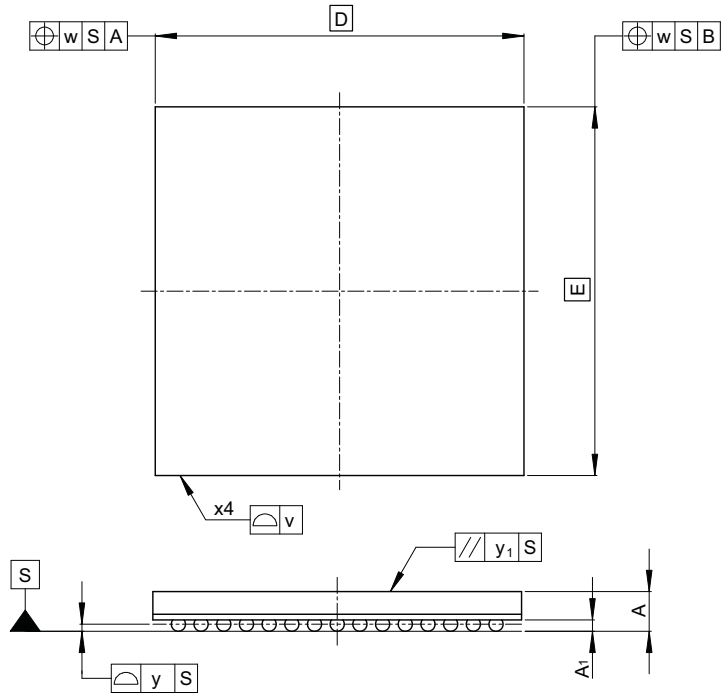


Figure 2.104 SWD SWCLK timing

Appendix 1.Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g

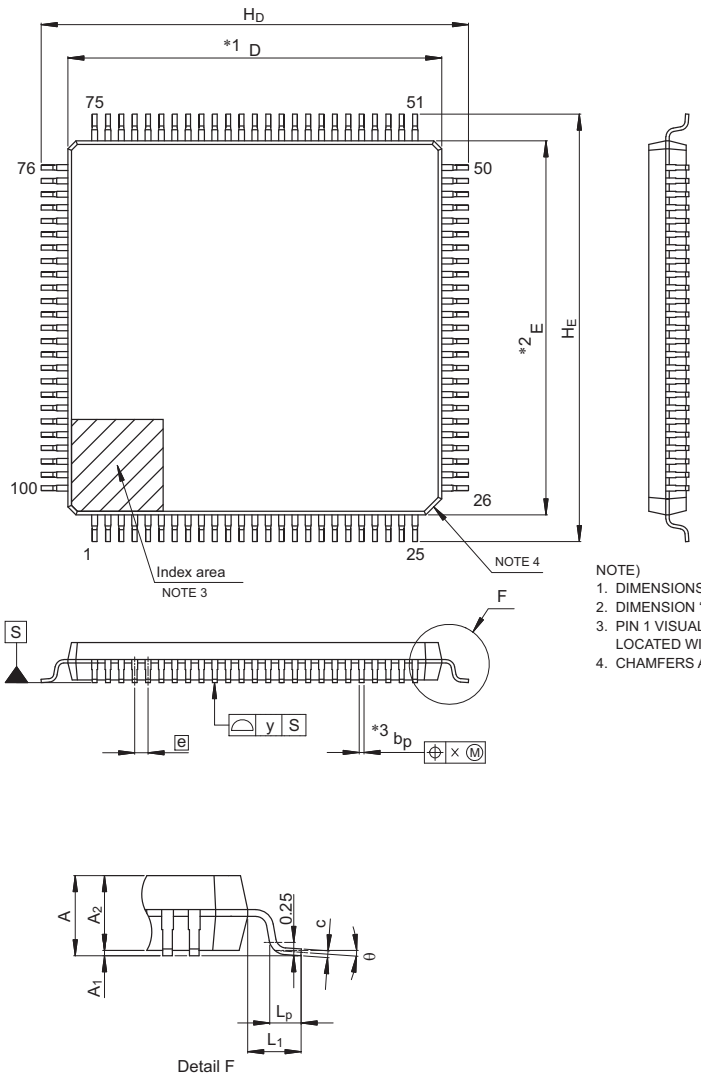


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 1.1 176-pin BGA

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 1.5 100-pin LQFP