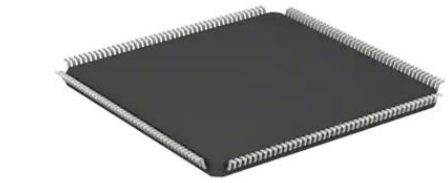
Renesas Electronics America Inc - R7FS5D97C3A01CFC#AA0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	133
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	640K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d97c3a01cfc-aa0

General Precautions

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table 1.3 System (2 of 3)

Feature	Functional description
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor reset 0 • Voltage monitor reset 1 • Voltage monitor reset 2 • Independent Watchdog Timer reset • Watchdog Timer reset • Deep Software Standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets in User's Manual.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected in the software program. See section 8, Low Voltage Detection (LVD) in User's Manual.
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • Independent Watchdog Timer (WDT) on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit in User's Manual.
Clock Frequency Accuracy Measurement Circuit (CAC)	The CAC checks the system clock frequency with a reference clock signal by counting the number of pulses of the system clock to be measured. The reference clock can be provided externally through a CACREF pin or internally from various on-chip oscillators. Event signals can be generated when the clock does not match or measurement ends. This feature is particularly useful in implementing a fail-safe mechanism for home and industrial automation applications. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC) in User's Manual.
Interrupt Controller Unit (ICU)	The ICU controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU) in User's Manual.
Key interrupt function (KINT)	A key interrupt can be generated by setting the Key Return Mode register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT) in User's Manual.
Low-power modes	Power consumption can be reduced in multiple ways, including by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low-power modes. See section 11, Low-Power Modes in User's Manual.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function in User's Manual.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection in User's Manual.
Memory Protection Unit (MPU)	Four MPUs and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU) in User's Manual.
Watchdog Timer (WDT)	The WDT is a 14-bit down-counter. It can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT) in User's Manual.

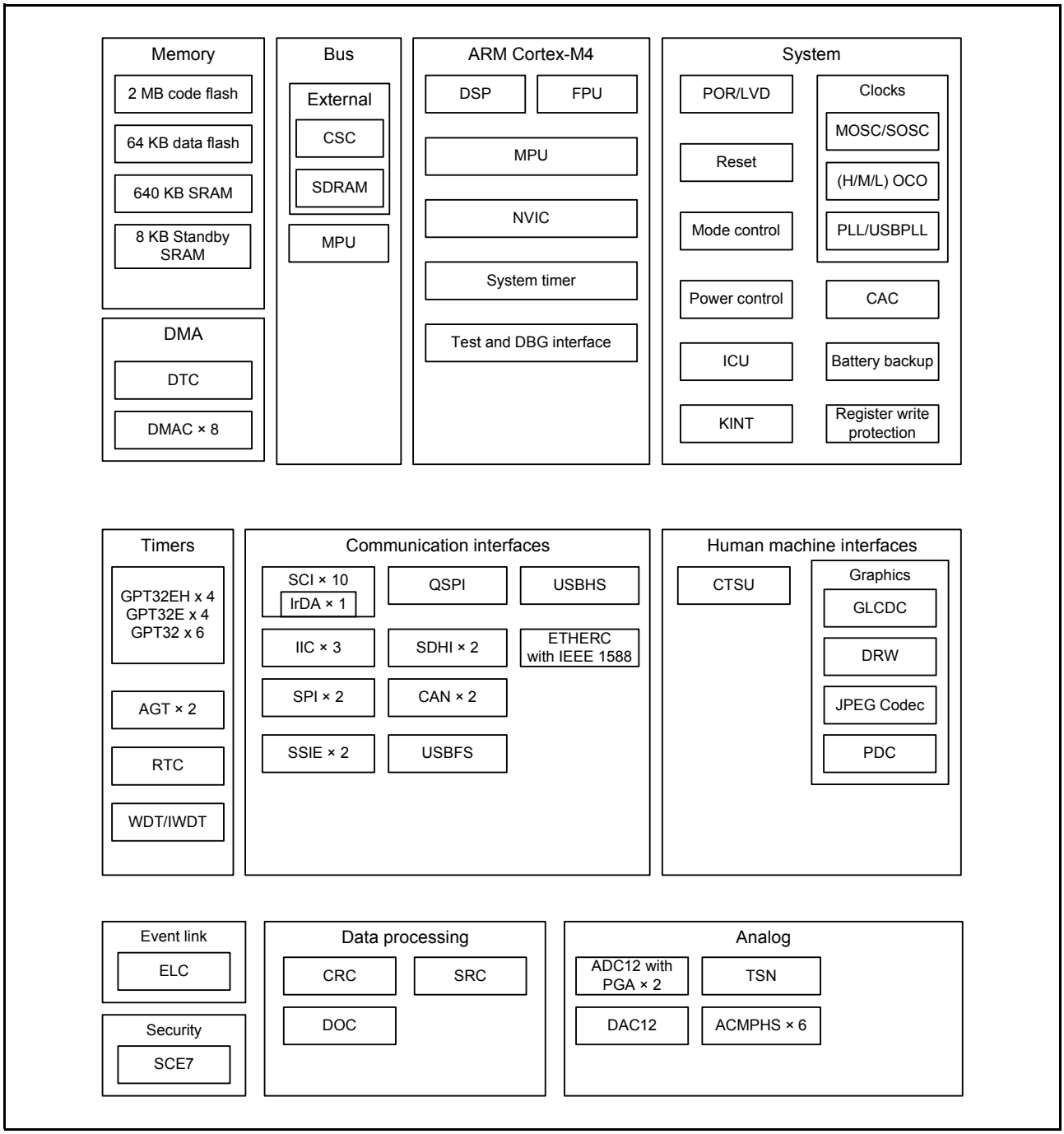


Figure 1.1 Block diagram

1.3 Part Numbering

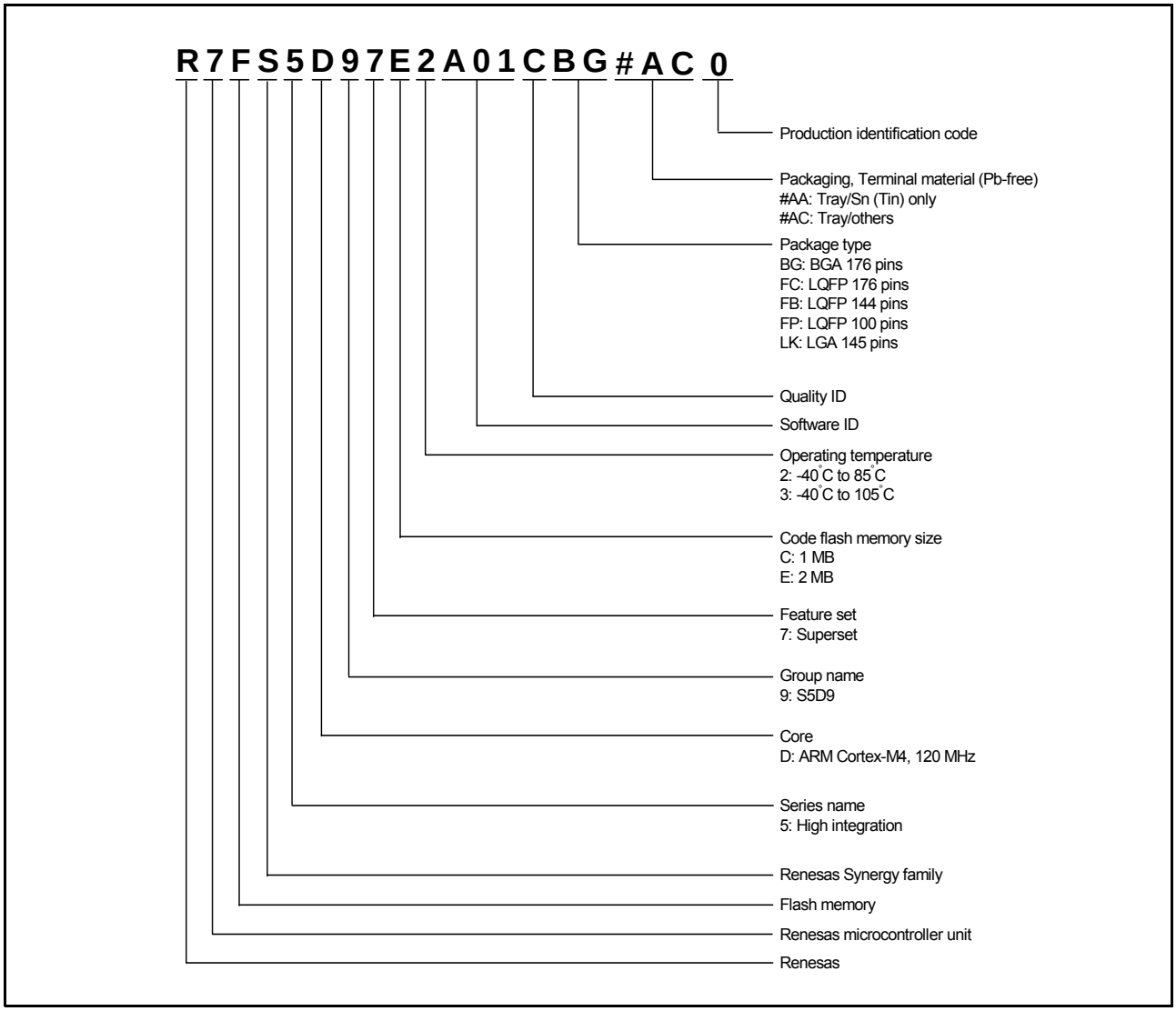


Figure 1.2 Part numbering scheme

Table 1.14 List of Products

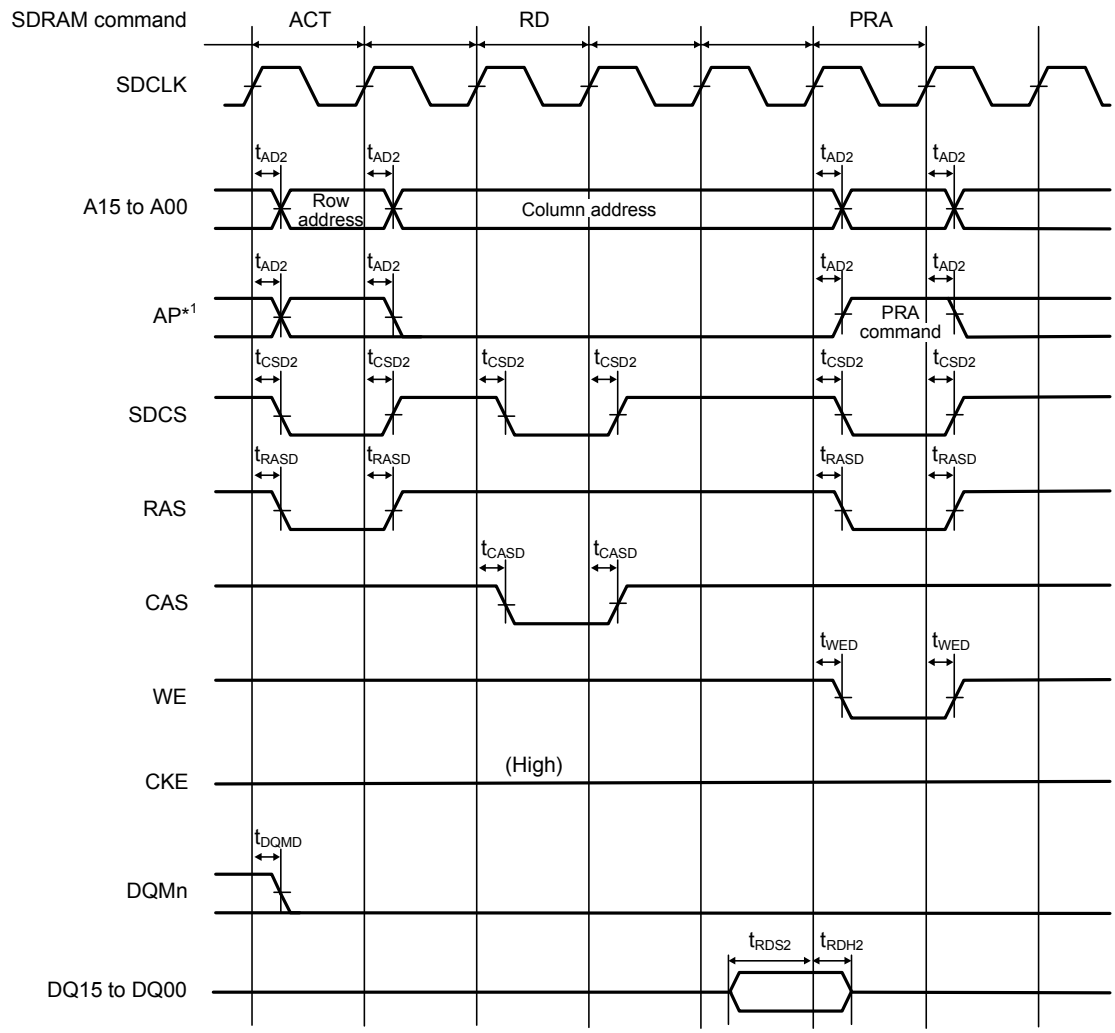
Part Number	Orderable Part Number	Package	Code flash	Data flash	SRAM	Operating Temperature
R7FS5D97E2A01CBG	R7FS5D97E2A01CBG#AC0	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FS5D97E3A01CFC	R7FS5D97E3A01CFC#AA0	PLQP0176KB-A				-40 to +105°C
R7FS5D97E2A01CLK	R7FS5D97E2A01CLK#AC0	PTLG0145KA-A				-40 to +85°C
R7FS5D97E3A01CFB	R7FS5D97E3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS5D97E3A01CFP	R7FS5D97E3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C
R7FS5D97C2A01CBG	R7FS5D97C2A01CBG#AC0	PLBG0176GE-A	1 MB			-40 to +85°C
R7FS5D97C3A01CFC	R7FS5D97C3A01CFC#AA0	PLQP0176KB-A				-40 to +105°C
R7FS5D97C2A01CLK	R7FS5D97C2A01CLK#AC0	PTLG0145KA-A				-40 to +85°C
R7FS5D97C3A01CFB	R7FS5D97C3A01CFB#AA0	PLQP0144KA-B				-40 to +105°C
R7FS5D97C3A01CFP	R7FS5D97C3A01CFP#AA0	PLQP0100KB-B				-40 to +105°C

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

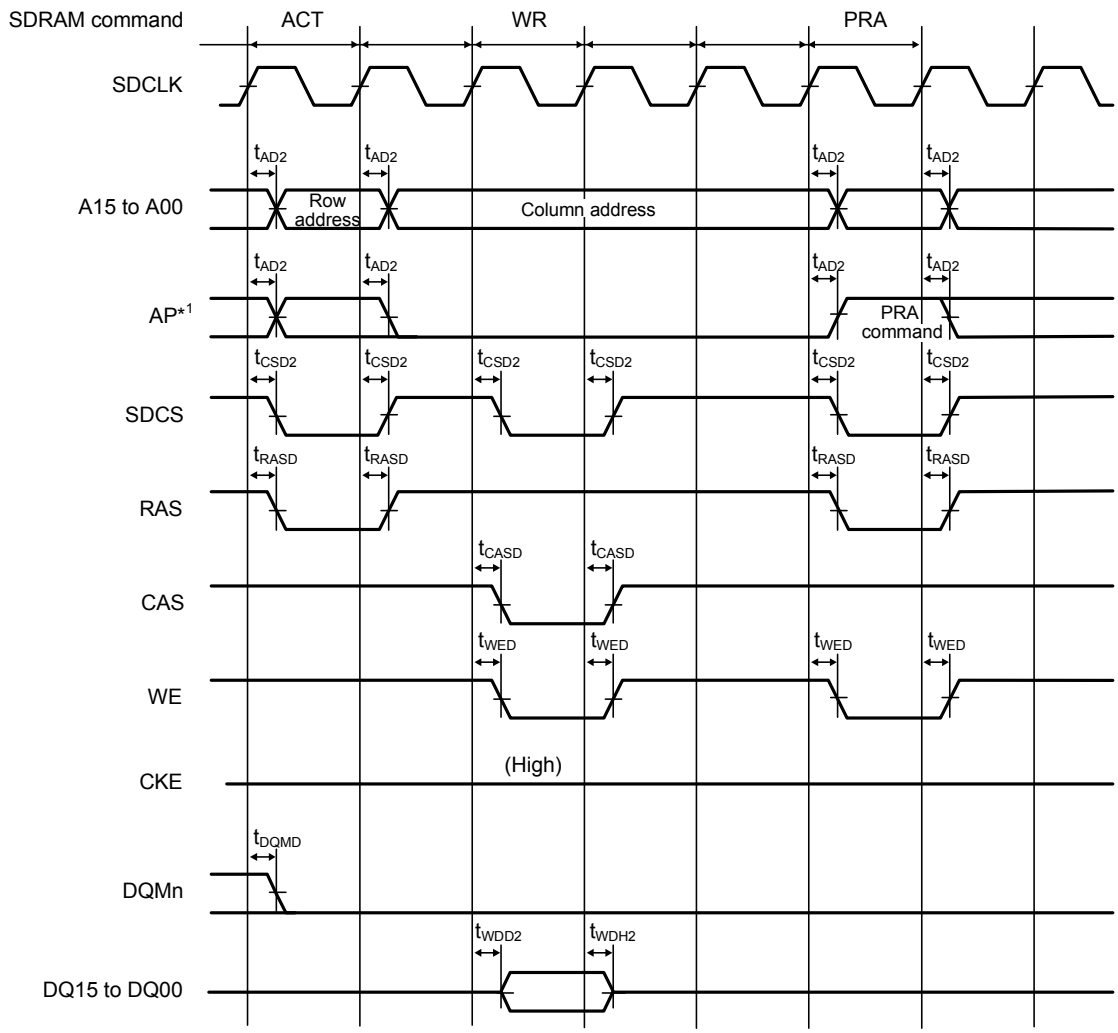
Function	Signal	I/O	Description
Power supply	VCC	Input	Digital voltage supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect to the system power supply. Connect to VSS through a 0.1-µF smoothing capacitor close to each VCC pin.
	VCL0	-	Connect to VSS through a 0.1-µF smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin.
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices.
	SDCLK	Output	Outputs the SDRAM-dedicated clock.
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin.
Interrupt	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ15	Input	Maskable interrupt request pins.
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins.
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins.
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data.
	TDATA0 to TDATA3	Output	Trace data output.
	SWDIO	I/O	Serial wire debug data input/output pin.
	SWCLK	Input	Serial wire clock pin.
	SWO	Output	Serial wire trace output pin.
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active low.
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active low.
	WR0 to WR1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active low.
	BC0 to BC1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active low.
	ALE	Output	Address latch signal when address/data multiplexed bus is selected.
	WAIT	Input	Input pin for wait request signals in access to the external space, active low.
	CS0 to CS7	Output	Select signals for CS areas, active low.
	A00 to A23	Output	Address bus.
	D00 to D15	I/O	Data bus.
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus.

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces											Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
G4	108	-	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA08_B
G2	109	-	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_B
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	113	-	-	-	-	-	PA01	-	-	-	-	-	-	-	SCK8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_B
H4	114	-	-	-	-	-	PA00	-	-	-	-	-	-	-	TXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_B
J4	115	-	-	-	-	-	P607	-	-	-	-	-	-	-	RXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_B
J1	116	-	-	-	-	-	P606	-	-	-	-	-	RTCOUT	-	CTS8_RTS8/SS8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_B
J2	117	H2	93	-	-	-	P605	D11[A11/D11]	DQ11	-	-	GTIOC8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	-	P604	D12[A12/D12]	DQ12	-	-	GTIOC8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	-	P603	D13[A13/D13]	DQ13	-	-	GTIOC7A	-	-	-	CTS9_RTS9/SS9	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	-	P602	EBCLK	SDCLK	-	-	GTIOC7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA04_A
K2	121	J2	97	66	-	-	P601	WR/WR0	DQM0	-	-	GTIOC6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA03_A
L1	122	H4	98	67	CLKOUT/CACREF	-	P600	RD	-	-	-	GTIOC6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	LCD_DATA02_A
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L2	125	J3	101	68	-	KR07	P107	D07[A07/D07]	DQ07	AGTOA0	-	GTIOC8A	-	-	CTS8_RTS8/SS8	-	-	-	-	-	-	-	-	-	-	LCD_DATA01_A
M1	126	K3	102	69	-	KR06	P106	D06[A06/D06]	DQ06	AGTOB0	-	GTIOC8B	-	-	SCK8	-	-	SSLA3_A	-	-	-	-	-	-	-	-	LCD_DATA00_A
L3	127	J4	103	70	-	IRQ0/KR05	P105	D05[A05/D05]	DQ05	-	GTETRGA	GTIOC1A	-	-	TXD8/MOSI8/SDA8	-	-	SSLA2_A	-	-	-	-	-	-	-	-	LCD_TCON3_A
M2	128	L3	104	71	-	IRQ1/KR04	P104	D04[A04/D04]	DQ04	-	GTETRGB	GTIOC1B	-	-	RXD8/MISO8/SCL8	-	-	SSLA1_A	-	-	-	-	-	-	-	-	LCD_TCON2_A
N1	129	L1	105	72	-	KR03	P103	D03[A03/D03]	DQ03	-	GTOWUP	GTIOC2A_A	-	CTX0	CTS0_RTS0/SS0	-	-	SSLA0_A	-	-	-	-	-	-	-	-	LCD_TCON1_A
M3	130	M1	106	73	-	KR02	P102	D02[A02/D02]	DQ02	AGTO0	GTOWLO	GTIOC2B_A	-	CRX0	SCK0	-	-	RSPCKA_A	-	-	-	-	-	ADTRG0	-	-	LCD_TCON0_A
N2	131	M2	107	74	-	IRQ1/KR01	P101	D01[A01/D01]	DQ01	AGTEE0	GTETRGB	GTIOC5A	-	-	TXD0/MOSI0/SDA0	CTS1_RTS1/SS1	SDA1_B	MOSIA_A	-	-	-	-	-	-	-	-	LCD_CLK_A
P1	132	N1	108	75	-	IRQ2/KR00	P100	D00[A00/D00]	DQ00	AGTIO0	GTETRGA	GTIOC5B	-	-	RXD0/MISO0/SCL0	SCK1	SCL1_B	MISOA_A	-	-	-	-	-	-	-	-	LCD_EXTCLK_A
N3	133	L2	109	-	-	-	P800	D14[A14/D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R1	134	N2	110	-	-	-	P801	D15[A15/D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT4_A	-	-	-	-
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT5_A	-	-	-	LCD_DATA02_B
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT6_A	-	-	-	LCD_DATA01_B
P3	137	-	-	-		-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1DAT7_A	-	-	-	LCD_DATA00_B
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC11A	-	USB_VBUSEN	-	-	-	QSPCLK	-	-	-	-	SD1CLK_A	AN016	IVREF0	-	-
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC11B	-	USB_OVRCURA	-	TXD5/MOSI5/SDA5	-	QSSL	-	-	-	-	SD1CMD_A	AN116	IVREF1	-	-
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC12A	-	USB_OVRCURB	-	RXD5/MISO5/SCL5	-	QIO0	-	-	-	-	SD1DAT0_A	AN017	IVCMP0	-	-
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC12B	-	USB_EXICEN	CTS6_RTS6/SS6	SCK5	-	QIO1	-	-	-	-	SD1DAT1_A	AN117	-	-	-
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC13A	-	USB_ID	SCK6	CTS5_RTS5/SS5	-	QIO2	-	-	-	-	SD1DAT2_A	AN018	-	-	-
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC13B	-	-	RXD6/MISO6/SCL6	-	-	QIO3	-	-	-	-	SD1DAT3_A	AN118	-	-	-



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.23 SDRAM single read timing



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 2.24 SDRAM single write timing

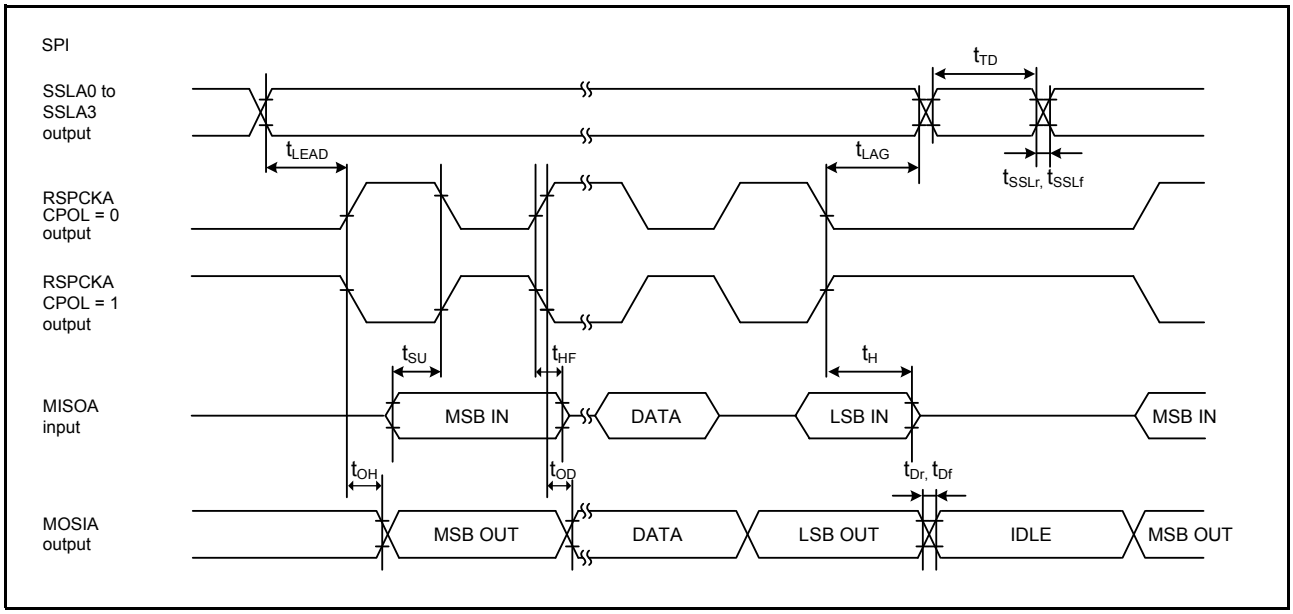


Figure 2.51 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

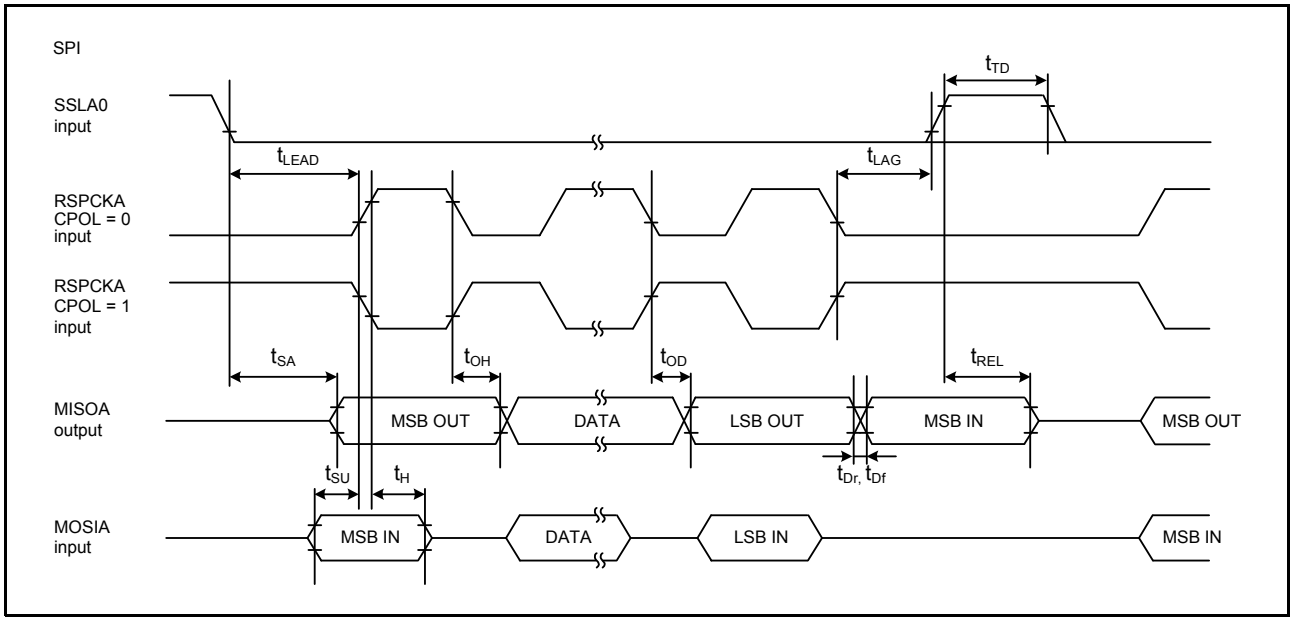


Figure 2.52 SPI timing for slave when CPHA = 0

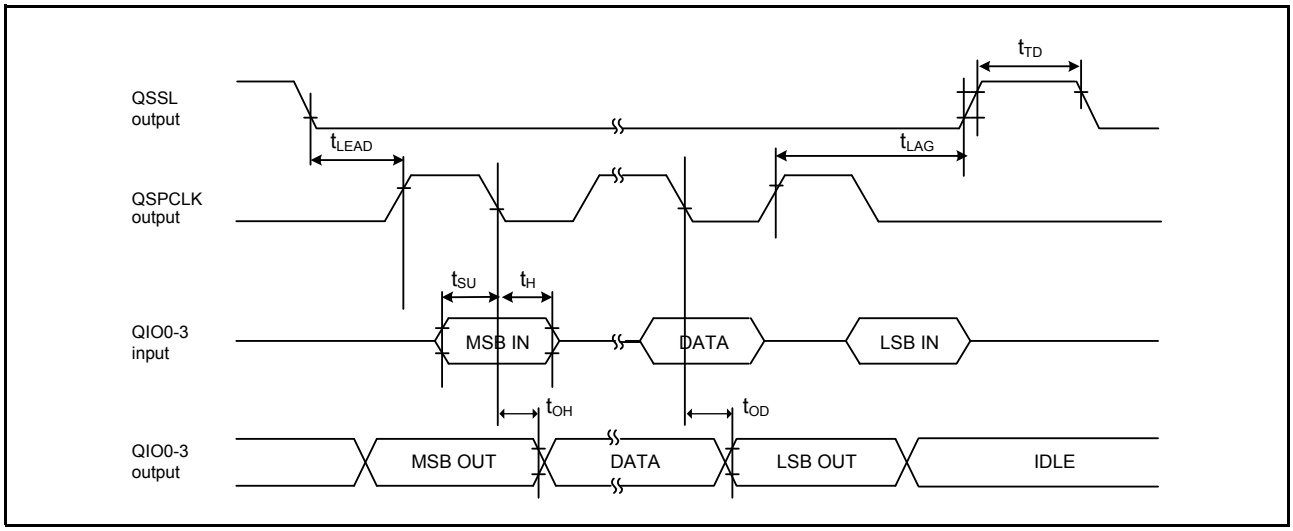


Figure 2.55 Transmit and receive timing

2.3.13 IIC Timing

Table 2.27 IIC timing (1) (1 of 2)

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.

(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.

(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Item		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 2.56
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

2.3.14 SSIE Timing

Table 2.29 SSIE timing

(1) High drive output is selected with the port drive capability bit in the PmnPFS register.

(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Item			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 2.57
		Slave	t_I	80	-	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	Input set up time	Master	t_{SR}	12	-	ns	Figure 2.59, Figure 2.60
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 2.59, Figure 2.60
	Output delay time from SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 2.61*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 2.58
	High level/ low level		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK/SSIFS pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA1 pin.

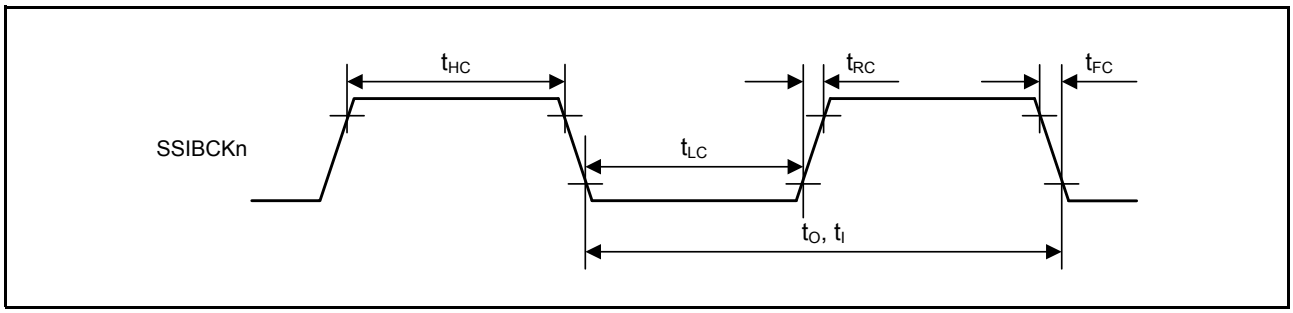


Figure 2.57 SSIE clock input/output timing

Table 2.40 A/D conversion characteristics for unit 0 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN003 to AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of pins AN000 to AN007 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0/VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 2.41 A/D conversion characteristics for unit 1 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Item			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-

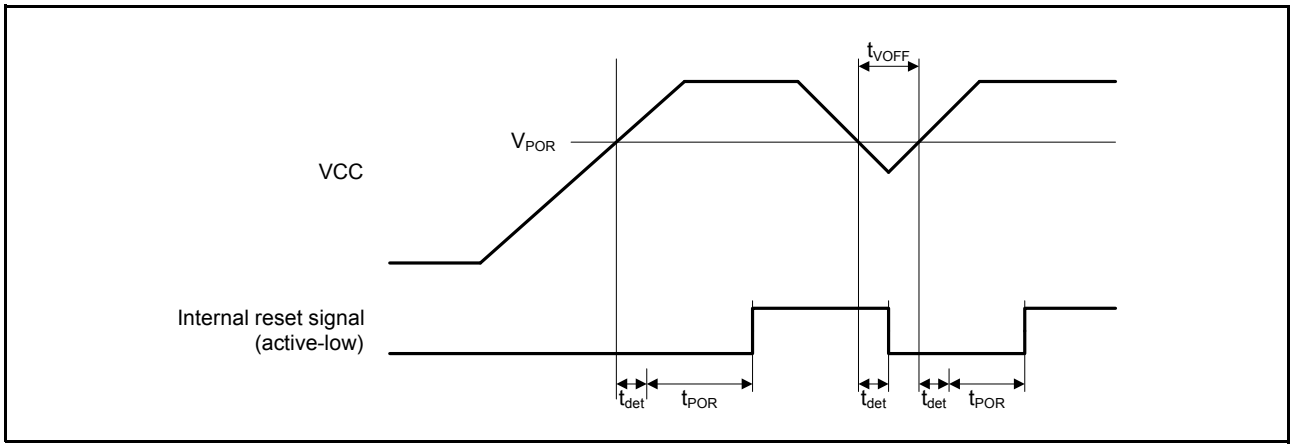


Figure 2.93 Power-on reset timing

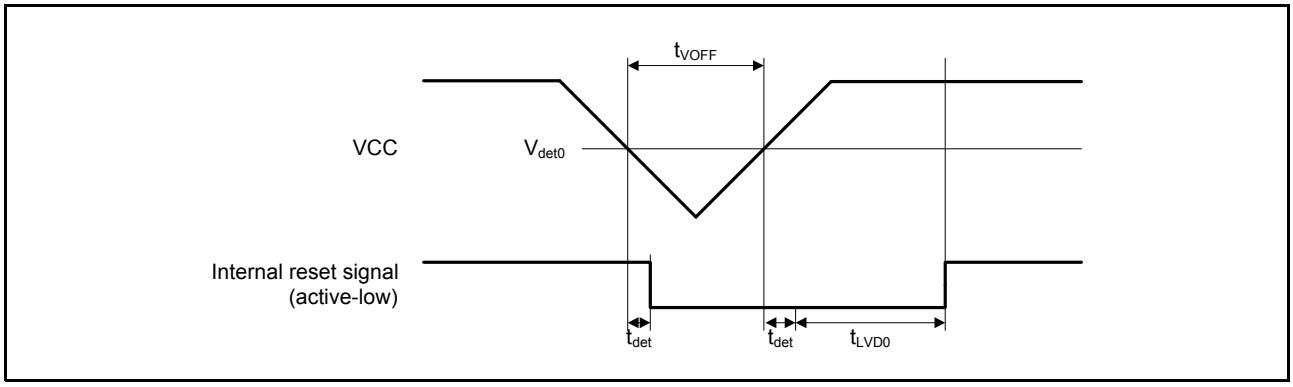


Figure 2.94 Voltage detection circuit timing (V_{det0})

2.10 VBATT Characteristics

Table 2.48 Battery backup function characteristics
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 2.97
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	-	-	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

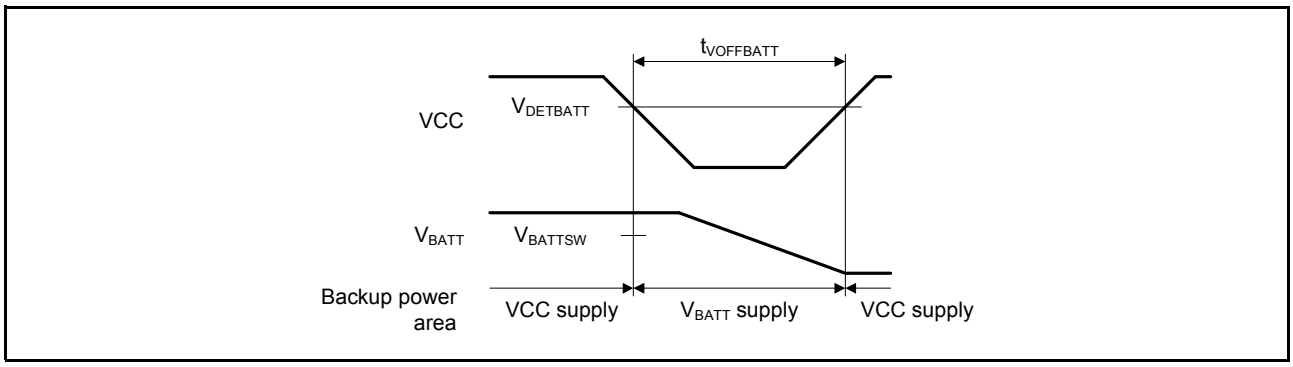


Figure 2.97 Battery backup function characteristics

2.11 CTSU Characteristics

Table 2.49 CTSU characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{oH}	-	-	-40	mA	When the mutual capacitance method is applied

2.12 ACMPHS Characteristics

Table 2.50 ACMPHS characteristics

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
Internal reference voltage	Vref	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

Table 2.52 PGA characteristics in differential mode (2 of 2)

Item		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	–1.0	-	1.0	%
	G = 2.333		–1.0	-	1.0	
	G = 4.000		–1.0	-	1.0	
	G = 5.667		–1.0	-	1.0	

2.14 Flash Memory Characteristics

2.14.1 Code Flash Memory Characteristics

Table 2.53 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time $N_{PEC} \leq 100$ times	128-byte	t_{P128}	-	1.1	13.2	-	0.52	6.0	ms	
	8-KB	t_{P8K}	-	75	176	-	34	80	ms	
	32-KB	t_{P32K}	-	299	704	-	136	320	ms	
Programming time $N_{PEC} > 100$ times	128-byte	t_{P128}	-	1.4	15.8	-	0.62	7.2	ms	
	8-KB	t_{P8K}	-	90	212	-	41	96	ms	
	32-KB	t_{P32K}	-	359	848	-	163	384	ms	
Erasure time $N_{PEC} \leq 100$ times	8-KB	t_{E8K}	-	92	216	-	51	120	ms	
	32-KB	t_{E32K}	-	329	864	-	183	480	ms	
Erasure time $N_{PEC} > 100$ times	8-KB	t_{E8K}	-	110	260	-	61	144	ms	
	32-KB	t_{E32K}	-	396	1040	-	220	576	ms	
Reprogramming/erasure cycle*Note:		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note: The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

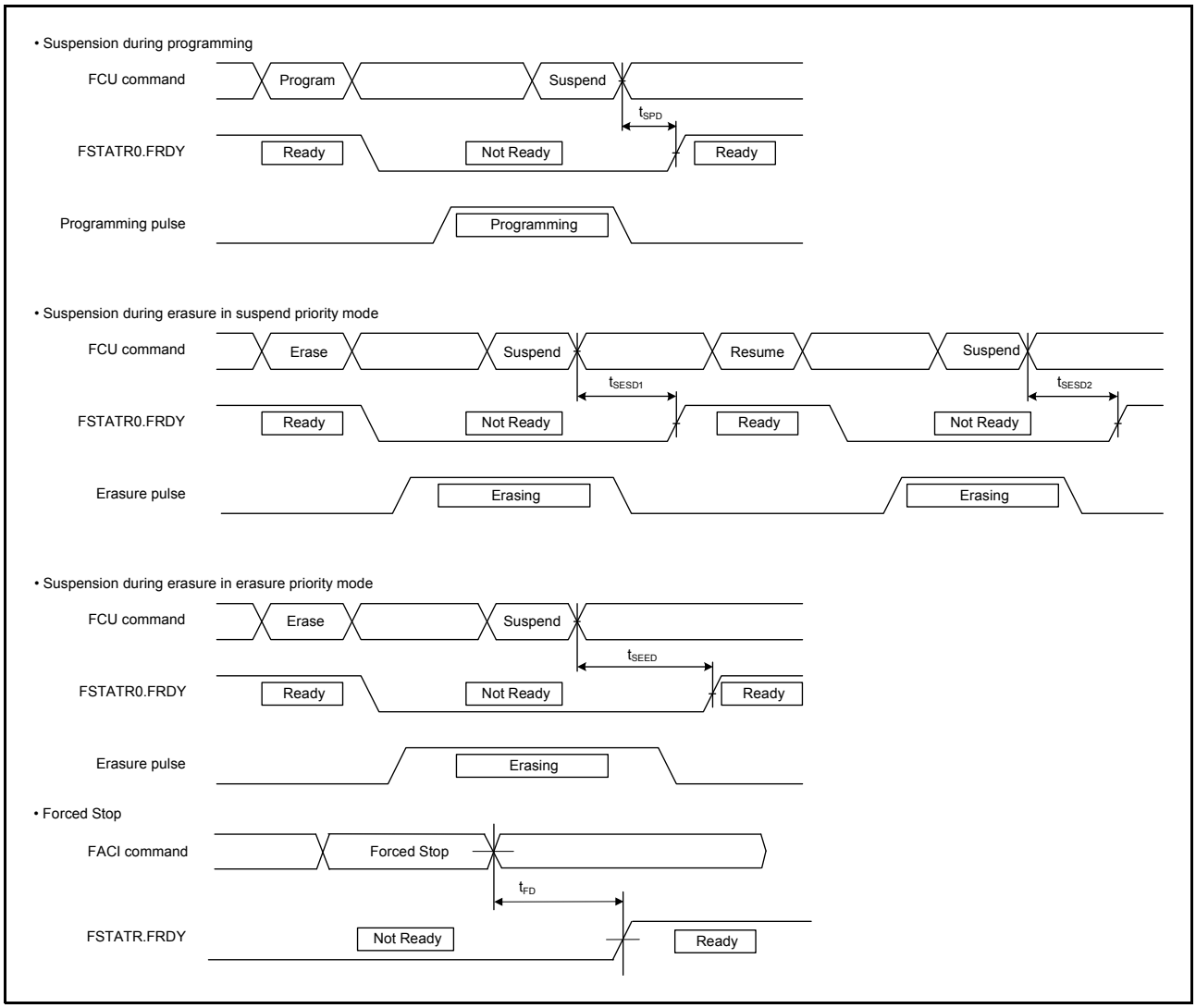


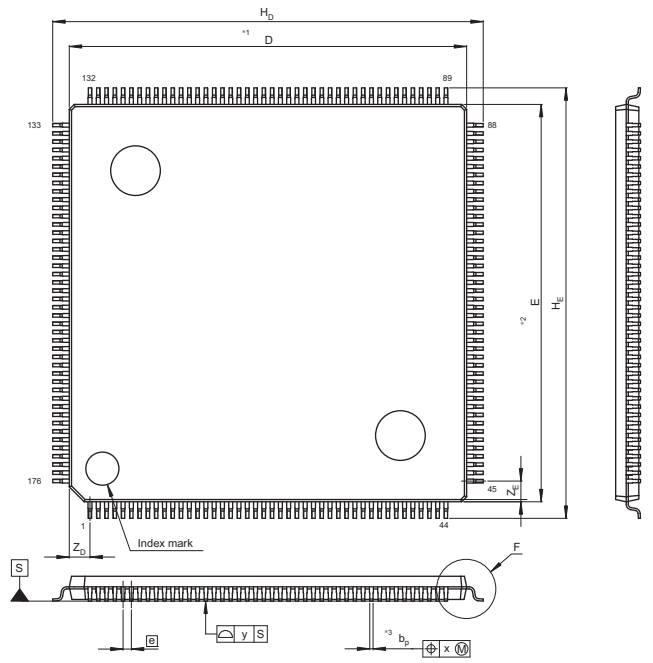
Figure 2.98 Suspension and forced stop timing for flash memory programming and erasure

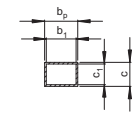
2.14.2 Data Flash Memory Characteristics

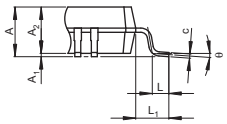
Table 2.54 Data flash memory characteristics (1 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Item		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.46	3.8	-	0.21	1.7	ms	
	8-byte	t_{DP8}	-	0.48	4.0	-	0.22	1.8		
	16-byte	t_{DP16}	-	0.53	4.5	-	0.24	2.0		
Erasure time	64-byte	t_{DE64}	-	4.03	18	-	2.24	10	ms	
	128-byte	t_{DE128}	-	6.2	27	-	3.4	15		
	256-byte	t_{DE256}	-	11.6	50	-	6.4	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





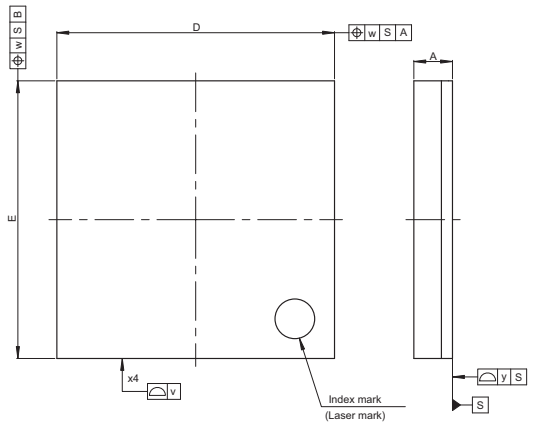


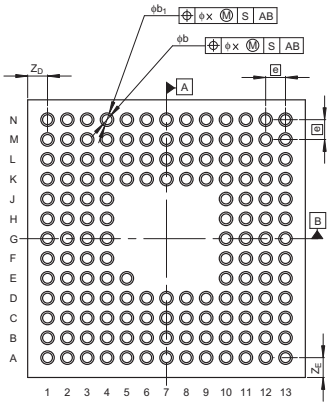
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 1.2 176-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g





Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 1.3 145-pin LGA

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