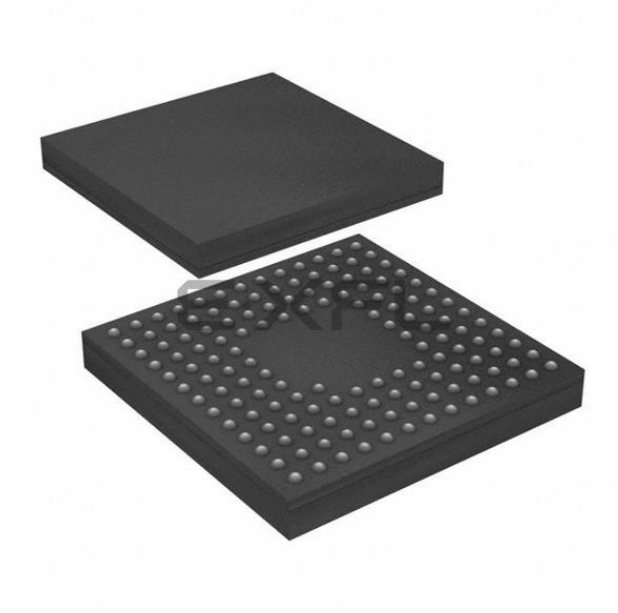
# Renesas Electronics America Inc - R7FS5D97E2A01CLK#AC0 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M4 |
| Core Size | 32-Bit Single-Core |
| Speed | 120MHz |
| Connectivity | CANbus, EBI/EMI, Ethernet, I²C, IrDA, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 110 |
| Program Memory Size | 2MB (2M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 640K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 145-TFLGA |
| Supplier Device Package | 145-TFLGA (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs5d97e2a01clk-ac0 |

Leading performance 120-MHz ARM Cortex-M4 microcontroller, up to 2-MB code flash memory, 640-KB SRAM, Graphics LCD Controller, 2D Drawing Engine, Capacitive Touch Sensing Unit, Ethernet MAC Controller with IEEE 1588 PTP, USB 2.0 High-Speed, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

# Features

### ■ ARM Cortex-M4 Core with Floating Point Unit (FPU)
- ARMv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and ARM Memory Protection Unit (MPU)

### ■ Memory
- Up to 2-MB code flash memory (40 MHz zero wait states)
- 64-KB data flash memory (up to 100,000 erase/write cycles)
- Up to 640-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

### ■ Connectivity
- Ethernet MAC Controller (ETHERC)
- Ethernet DMA Controller (EDMAC)
- Ethernet PTP Controller (EPTPC)
- USB 2.0 High-Speed Module (USBHS)
  - On-chip transceiver
  - USB battery charge version 1.2 supported
- USB 2.0 Full-Speed Module (USBFS)
  - On-chip transceiver
- Serial Communications Interface (SCI) with FIFO × 10
- Serial Peripheral Interface (SPI) × 2
- $I^2C$ Bus Interface (IIC) × 3
- CAN module (CAN) × 2
- Serial Sound Interface Enhanced (SSIE) × 2
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8- or 16-bit bus space is selectable per area
  - SDRAM support

### ■ Analog
- 12-Bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-Bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature sensor (TSN)

### ■ Timers
- General PWM Timer 32-Bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-Bit Enhanced (GPT32E) × 4
- General PWM Timer 32-Bit (GPT32) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

### ■ Safety
- ECC in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

### ■ System and Power Management
- Low-power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key interrupt function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

### ■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256
- GHASH
- RSA/DSA
- True Random Number Generator (TRNG)

### ■ Human Machine Interface (HMI)
- Graphics LCD Controller (GLCDC)
- JPEG Codec
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Parallel Data Capture Unit (PDC)

### ■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- Independent Watchdog Timer OCO (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

### ■ General-Purpose I/O Ports
- Up to 133 input/output pins
  - Up to 9 CMOS input
  - Up to 124 CMOS input/output
    - Up to 21 5-V tolerant input/output
    - Up to 18 high current (20 mA)

### ■ Operating Voltage
- VCC: 2.7 to 3.6 V

### ■ Operating Temperature and Packages
- Ta = –40°C to +85°C
  - 176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)
  - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
- Ta = –40°C to +105°C
  - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

**Table 1.3 System (3 of 3)**

| Feature | Functional description |
|---|---|
| Independent Watchdog Timer (IWDT) | The IWDT consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. The IWDT provides functionality to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, or refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT) in User's Manual. |

**Table 1.4 Event link**

| Feature | Functional description |
|---|---|
| Event Link Controller (ELC) | The ELC uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC) in User's Manual. |

**Table 1.5 Direct memory access**

| Feature | Functional description |
|---|---|
| Data Transfer Controller (DTC) | A DTC module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC) in User's Manual. |
| DMA Controller (DMAC) | An 8-channel DMAC module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC) in User's Manual. |

**Table 1.6 External bus interface**

| Feature | Functional description |
|---|---|
| External buses | • CS area (EXBIU): Connected to the external devices (external memory interface)<br>• SDRAM area (EXBIU): Connected to the SDRAM (external memory interface)<br>• QSPI area (EXBIUT2): Connected to the QSPI (external device interface). |

**Table 1.7 Timers**

| Feature | Functional description |
|---|---|
| General PWM Timer (GPT) | The GPT is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT) in User's Manual. |
| Port Output Enable for GPT (POEG) | Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG) in User's Manual. |
| Asynchronous General-Purpose Timer (AGT) | The AGT is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events.<br>This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT) in User's Manual. |
| Realtime Clock (RTC) | The RTC has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings.<br>For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years.<br>For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC) in User's Manual. |

**Table 1.13 Security**

| Feature | Functional description |
|---|---|
| Secure Crypto Engine 7 (SCE7) | • Security algorithms:<br>- Symmetric algorithms: AES, 3DES, and ARC4<br>- Asymmetric algorithms: RSA and DSA.<br>• Other support features:<br>- TRNG (True Random Number Generator)<br>- Hash-value generation: SHA1, SHA224, SHA256, GHASH<br>- 128-bit unique ID. |

## 1.2 Block Diagram

Figure 1.1 shows the block diagram of the MCU superset. Some individual devices within the group have a subset of the features.

## 1.3 Part Numbering

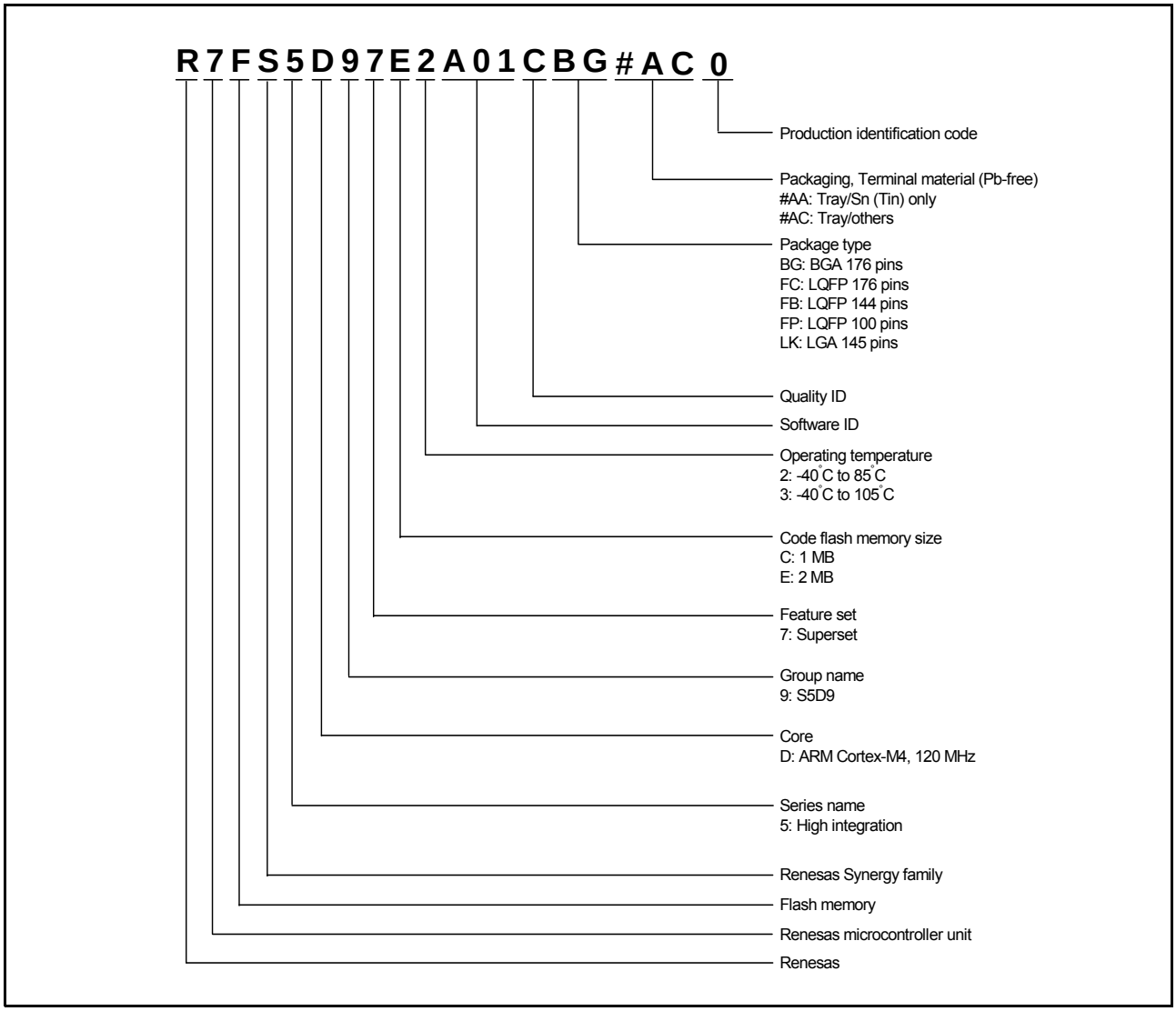


**Figure 1.2 Part numbering scheme**

**Table 1.14 List of Products**

| Part Number | Orderable Part Number | Package | Code flash | Data flash | SRAM | Operating Temperature |
|---|---|---|---|---|---|---|
| R7FS5D97E2A01CBG | R7FS5D97E2A01CBG#AC0 | PLBG0176GE-A | 2 MB | 64 KB | 640 KB | -40 to +85°C |
| R7FS5D97E3A01CFC | R7FS5D97E3A01CFC#AA0 | PLQP0176KB-A | | | | -40 to +105°C |
| R7FS5D97E2A01CLK | R7FS5D97E2A01CLK#AC0 | PTLG0145KA-A | | | | -40 to +85°C |
| R7FS5D97E3A01CFB | R7FS5D97E3A01CFB#AA0 | PLQP0144KA-B | | | | -40 to +105°C |
| R7FS5D97E3A01CFP | R7FS5D97E3A01CFP#AA0 | PLQP0100KB-B | | | | -40 to +105°C |
| R7FS5D97C2A01CBG | R7FS5D97C2A01CBG#AC0 | PLBG0176GE-A | 1 MB | | | -40 to +85°C |
| R7FS5D97C3A01CFC | R7FS5D97C3A01CFC#AA0 | PLQP0176KB-A | | | | -40 to +105°C |
| R7FS5D97C2A01CLK | R7FS5D97C2A01CLK#AC0 | PTLG0145KA-A | | | | -40 to +85°C |
| R7FS5D97C3A01CFB | R7FS5D97C3A01CFB#AA0 | PLQP0144KA-B | | | | -40 to +105°C |
| R7FS5D97C3A01CFP | R7FS5D97C3A01CFP#AA0 | PLQP0100KB-B | | | | -40 to +105°C |

**Table 1.16 Pin functions (3 of 5)**

| Function | Signal | I/O | Description |
|---|---|---|---|
| SPI | RSPCKA, RSPCKB | I/O | Clock input/output pin. |
| | MOSIA, MOSIB | I/O | Input or output pins for data output from the master. |
| | MISOA, MISOB | I/O | Input or output pins for data output from the slave. |
| | SSLA0, SSLB0 | I/O | Input or output pin for slave selection. |
| | SSLA1 to SSLA3, SSLB1 to SSLB3 | Output | Output pins for slave selection. |
| QSPI | QSPCLK | Output | QSPI clock output pin. |
| | QSSL | Output | QSPI slave output pin. |
| | QIO0 to QIO3 | I/O | Data0 to Data3. |
| CAN | CRX0, CRX1 | Input | Receive data. |
| | CTX0, CTX1 | Output | Transmit data. |
| USBFS | VCC_USB | Input | Power supply pins. |
| | VSS_USB | Input | Ground pins. |
| | USB_DP | I/O | D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus. |
| | USB_DM | I/O | D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus. |
| | USB_VBUS | Input | USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller. |
| | USB_EXICEN | Output | Low-power control signal for external power supply (OTG) chip. |
| | USB_VBUSEN | Output | VBUS (5 V) supply enable signal for external power supply chip. |
| | USB_OVRCURA, USB_OVRCURB | Input | Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected. |
| | USB_ID | Input | Connect the MicroAB connector ID input signal to this pin during operation in OTG mode. |
| USBHS | VCC_USBHS | Input | Power supply pin. |
| | VSS1_USBHS | Input | Ground pin. |
| | VSS2_USBHS | Input | Ground pin. |
| | AVCC_USBHS | Input | Analog power supply pin for the USBHS. |
| | AVSS_USBHS | Input | Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin. |
| | PVSS_USBHS | Input | PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin. |
| | USBHS_RREF | I/O | USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor (±1%). |
| | USBHS_DP | I/O | USB bus D+ data pin. |
| | USBHS_DM | I/O | USB bus D- data pin. |
| | USBHS_EXICEN | Output | Connect this pin to the OTG power supply IC. |
| | USBHS_ID | Input | Connect this pin to the OTG power supply IC. |
| | USBHS_VBUSEN | Output | VBUS power enable signal for USB. |
| | USBHS_OVRCURA, USBHS_OVRCURB | Input | Overcurrent pin for USB. |
| | USBHS_VBUS | Input | USB cable connection monitor input pin. |

| Pin number | | | | | | | | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | Power, System, Clock, Debug, CAC | Interrupt | I/O port | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSIE | ETHERC (MII) (25 MHz) | ETHERC (RMII) (50 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| A8 | 66 | A6 | 54 | 37 | TRDATA3 | - | P208 | - | - | - | GTOVLO | - | - | - | - | - | - | QIO3 | - | ET0_LINKSTA | ET0_LINKSTA | - | SD0DAT0_B | - | - | - | LCD_DATA18_B |
| C9 | 67 | C7 | 55 | 38 | RES | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| B8 | 68 | B6 | 56 | 39 | MD | - | P201 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| C8 | 69 | C8 | 57 | 40 | - | NMI | P200 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| D8 | 70 | - | - | - | - | - | P908 | CS7 | - | - | - | GTIOC2A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA14_B |
| D7 | 71 | - | - | - | - | - | P907 | CS6 | - | - | - | GTIOC2B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA13_B |
| A7 | 72 | - | - | - | - | - | P906 | CS5 | - | - | - | GTIOC3A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA12_B |
| B7 | 73 | - | - | - | - | - | P905 | CS4 | - | - | - | GTIOC3B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA11_B |
| C7 | 74 | C6 | 58 | - | - | - | P312 | CS3 | CAS | AGTOA1 | - | - | - | - | - | CTS3_RTS3/SS3 | - | - | - | - | - | - | - | - | - | - | - |
| D6 | 75 | B5 | 59 | - | - | - | P311 | CS2 | RAS | AGTOB1 | - | - | - | - | - | SCK3 | - | - | - | - | - | - | - | - | - | - | LCD_DATA23_A |
| A6 | 76 | D7 | 60 | - | - | - | P310 | A15 | A15 | AGTEE1 | - | - | - | - | - | TXD3 | - | QIO3 | - | - | - | - | - | - | - | - | LCD_DATA22_A |
| B6 | 77 | A5 | 61 | - | - | - | P309 | A14 | A14 | - | - | - | - | - | - | RXD3 | - | QIO2 | - | - | - | - | - | - | - | - | LCD_DATA21_A |
| A5 | 78 | C5 | 62 | - | - | - | P308 | A13 | A13 | - | - | - | - | - | - | - | - | QIO1 | - | - | - | - | - | - | - | - | LCD_DATA20_A |
| C6 | 79 | A4 | 63 | 41 | - | - | P307 | A12 | A12 | - | GTOUUP | - | - | - | CTS6 | - | - | QIO0 | - | - | - | - | - | - | - | - | LCD_DATA19_A |
| A4 | 80 | B4 | 64 | 42 | - | - | P306 | A11 | A11 | - | GTOULO | - | - | - | SCK6 | - | - | QSSL | - | - | - | - | - | - | - | - | LCD_DATA18_A |
| B5 | 81 | D6 | 65 | 43 | - | IRQ8 | P305 | A10 | A10 | - | GTOWUP | - | - | - | TXD6/MOSI6/SDA6 | - | - | QSPCLK | - | - | - | - | - | - | - | - | LCD_DATA17_A |
| B4 | 82 | C4 | 66 | 44 | - | IRQ9 | P304 | A09 | A09 | - | GTOWLO | GTIOC7A | - | - | RXD6/MISO6/SCL6 | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA16_A |
| C5 | 83 | A3 | 67 | 45 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| D5 | 84 | B3 | 68 | 46 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| A3 | 85 | D5 | 69 | 47 | - | - | P303 | A08 | A08 | - | - | GTIOC7B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA15_A |
| B3 | 86 | A2 | 70 | 48 | - | IRQ5 | P302 | A07 | A07 | - | GTOUUP | GTIOC4A | - | - | TXD2/MOSI2/SDA2 | - | - | SSLB3_B | - | - | - | - | - | - | - | - | LCD_DATA14_A |
| A2 | 87 | C3 | 71 | 49 | - | IRQ6 | P301 | A06 | A06 | AGTIO0 | GTOULO | GTIOC4B | - | - | RXD2/MISO2/SCL2 | CTS9_RTS9/SS9 | - | SSLB2_B | - | - | - | - | - | - | - | - | LCD_DATA13_A |
| C4 | 88 | B2 | 72 | 50 | TCK/SWCLK | - | P300 | - | - | - | GTOUUP | GTIOC0A_A | - | - | - | - | - | SSLB1_B | - | - | - | - | - | - | - | - | - |
| C3 | 89 | A1 | 73 | 51 | TMS/SWDIO | - | P108 | - | - | - | GTOULO | GTIOC0B_A | - | - | - | CTS9_RTS9/SS9 | - | SSLB0_B | - | - | - | - | - | - | - | - | - |
| A1 | 90 | D4 | 74 | 52 | CLKOUT/TDO/SWO | - | P109 | - | - | - | GTOVUP | GTIOC1A_A | - | CTX1 | - | TXD9/MOSI9/SDA9 | - | MOSIB_B | - | - | - | - | - | - | - | - | - |
| D3 | 91 | B1 | 75 | 53 | TDI | IRQ3 | P110 | - | - | - | GTOVLO | GTIOC1B_A | - | CRX1 | CTS2_RTS2/SS2 | RXD9/MISO9/SCL9 | - | MISOB_B | - | - | - | - | - | - | VCOUT | - | - |
| D4 | 92 | C2 | 76 | 54 | - | IRQ4 | P111 | A05 | A05 | - | - | GTIOC3A_A | - | - | SCK2 | SCK9 | - | RSPCKB_B | - | - | - | - | - | - | - | - | LCD_DATA12_A |
| B2 | 93 | D3 | 77 | 55 | - | - | P112 | A04 | A04 | - | - | GTIOC3B_A | - | - | TXD2/MOSI2/SDA2 | SCK1 | - | SSLB0_B | SSIBCK0_B | - | - | - | - | - | - | - | LCD_DATA11_A |
| B1 | 94 | C1 | 78 | 56 | - | - | P113 | A03 | A03 | - | - | GTIOC2A | - | - | RXD2/MISO2/SCL2 | - | - | - | SSILRCK0/SSIFS0_B | - | - | - | - | - | - | - | LCD_DATA10_A |
| C2 | 95 | E4 | 79 | 57 | - | - | P114 | A02 | A02 | - | - | GTIOC2B | - | - | - | - | - | - | SSIRXD0_B | - | - | - | - | - | - | - | LCD_DATA09_A |
| C1 | 96 | E3 | 80 | 58 | - | - | P115 | A01 | A01 | - | - | GTIOC4A | - | - | - | - | - | - | SSITXD0_B | - | - | - | - | - | - | - | LCD_DATA08_A |
| E3 | 97 | D2 | 81 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| E4 | 98 | D1 | 82 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| D2 | 99 | F4 | 83 | 59 | - | - | P608 | A00/BC0 | A00/DQM1 | - | - | GTIOC4B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA07_A |
| D1 | 100 | E2 | 84 | 60 | - | - | P609 | CS1 | CKE | - | - | GTIOC5A | - | CTX1 | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA06_A |
| F3 | 101 | F3 | 85 | 61 | - | - | P610 | CS0 | WE | - | - | GTIOC5B | - | CRX1 | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA05_A |
| E2 | 102 | E1 | 86 | - | CLKOUT/CACREF | - | P611 | - | SDCS | - | - | - | - | - | - | CTS7_RTS7/SS7 | - | - | - | - | - | - | - | - | - | - | - |
| E1 | 103 | F2 | 87 | - | - | - | P612 | D08[A08/D08] | DQ08 | - | - | - | - | - | - | SCK7 | - | - | - | - | - | - | - | - | - | - | - |
| F4 | 104 | F1 | 88 | - | - | - | P613 | D09[A09/D09] | DQ09 | - | - | - | - | - | - | TXD7 | - | - | - | - | - | - | - | - | - | - | - |
| F2 | 105 | G3 | 89 | - | - | - | P614 | D10[A10/D10] | DQ10 | - | - | - | - | - | - | RXD7 | - | - | - | - | - | - | - | - | - | - | - |
| F1 | 106 | - | - | - | - | - | P615 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA10_B |
| G1 | 107 | - | - | - | - | - | PA08 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA09_B |

| Pin number | | | | | Power, System, Clock, Debug, CAC | Interrupt | I/O port | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | | Analog | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | | | | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSIE | ETHERC (MII) (25 MHz) | ETHERC (RMII) (50 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| G4 | 108 | - | - | - | - | - | PA09 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA08_B |
| G2 | 109 | - | - | - | - | - | PA10 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA07_B |
| G3 | 110 | G1 | 90 | 62 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H3 | 111 | G2 | 91 | 63 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H1 | 112 | H1 | 92 | 64 | VCL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| H2 | 113 | - | - | - | - | - | PA01 | - | - | - | - | - | - | - | SCK8 | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA06_B |
| H4 | 114 | - | - | - | - | - | PA00 | - | - | - | - | - | - | - | TXD8 | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA05_B |
| J4 | 115 | - | - | - | - | - | P607 | - | - | - | - | - | - | - | RXD8 | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA04_B |
| J1 | 116 | - | - | - | - | - | P606 | - | - | - | - | - | RTCOUT | - | CTS8_RTS8/SS8 | - | - | - | - | - | - | - | - | - | - | - | LCD_DATA03_B |
| J2 | 117 | H2 | 93 | - | - | - | P605 | D11[A11/D11] | DQ11 | - | - | GTIOC8A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| J3 | 118 | G4 | 94 | - | - | - | P604 | D12[A12/D12] | DQ12 | - | - | GTIOC8B | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| K3 | 119 | H3 | 95 | - | - | - | P603 | D13[A13/D13] | DQ13 | - | - | GTIOC7A | - | - | - | CTS9_RTS9/SS9 | - | - | - | - | - | - | - | - | - | - | - |
| K1 | 120 | J1 | 96 | 65 | - | - | P602 | EBCLK | SDCLK | - | - | GTIOC7B | - | - | - | TXD9 | - | - | - | - | - | - | - | - | - | - | LCD_DATA04_A |
| K2 | 121 | J2 | 97 | 66 | - | - | P601 | WR/WR0 | DQM0 | - | - | GTIOC6A | - | - | - | RXD9 | - | - | - | - | - | - | - | - | - | - | LCD_DATA03_A |
| L1 | 122 | H4 | 98 | 67 | CLKOUT/CACREF | - | P600 | RD | - | - | - | GTIOC6B | - | - | - | SCK9 | - | - | - | - | - | - | - | - | - | - | LCD_DATA02_A |
| K4 | 123 | K2 | 99 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| L4 | 124 | K1 | 100 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| L2 | 125 | J3 | 101 | 68 | - | KR07 | P107 | D07[A07/D07] | DQ07 | AGTOA0 | - | GTIOC8A | - | - | CTS8_RTS8/SS8 | - | - | - | - | - | - | - | - | - | - | LCD_DATA01_A |
| M1 | 126 | K3 | 102 | 69 | - | KR06 | P106 | D06[A06/D06] | DQ06 | AGTOB0 | - | GTIOC8B | - | - | SCK8 | - | - | SSLA3_A | - | - | - | - | - | - | - | - | LCD_DATA00_A |
| L3 | 127 | J4 | 103 | 70 | - | IRQ0/KR05 | P105 | D05[A05/D05] | DQ05 | - | GTETRGA | GTIOC1A | - | - | TXD8/MOSI8/SDA8 | - | - | SSLA2_A | - | - | - | - | - | - | - | - | LCD_TCON3_A |
| M2 | 128 | L3 | 104 | 71 | - | IRQ1/KR04 | P104 | D04[A04/D04] | DQ04 | - | GTETRGB | GTIOC1B | - | - | RXD8/MISO8/SCL8 | - | - | SSLA1_A | - | - | - | - | - | - | - | - | LCD_TCON2_A |
| N1 | 129 | L1 | 105 | 72 | - | KR03 | P103 | D03[A03/D03] | DQ03 | - | GTOWUP | GTIOC2A_A | - | CTX0 | CTS0_RTS0/SS0 | - | - | SSLA0_A | - | - | - | - | - | - | - | - | LCD_TCON1_A |
| M3 | 130 | M1 | 106 | 73 | - | KR02 | P102 | D02[A02/D02] | DQ02 | AGTO0 | GTOWLO | GTIOC2B_A | - | CRX0 | SCK0 | - | - | RSPCKA_A | - | - | - | - | - | ADTRG0 | - | - | LCD_TCON0_A |
| N2 | 131 | M2 | 107 | 74 | - | IRQ1/KR01 | P101 | D01[A01/D01] | DQ01 | AGTEE0 | GTETRGB | GTIOC5A | - | - | TXD0/MOSI0/SDA0 | CTS1_RTS1/SS1 | SDA1_B | MOSIA_A | - | - | - | - | - | - | - | - | LCD_CLK_A |
| P1 | 132 | N1 | 108 | 75 | - | IRQ2/KR00 | P100 | D00[A00/D00] | DQ00 | AGTIO0 | GTETRGA | GTIOC5B | - | - | RXD0/MISO0/SCL0 | SCK1 | SCL1_B | MISOA_A | - | - | - | - | - | - | - | - | LCD_EXTCLK_A |
| N3 | 133 | L2 | 109 | - | - | - | P800 | D14[A14/D14] | DQ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R1 | 134 | N2 | 110 | - | - | - | P801 | D15[A15/D15] | DQ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | SD1DAT4_A | - | - | - | - |
| P2 | 135 | - | - | - | - | - | P802 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | SD1DAT5_A | - | - | - | LCD_DATA02_B |
| R2 | 136 | - | - | - | - | - | P803 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | SD1DAT6_A | - | - | - | LCD_DATA01_B |
| P3 | 137 | - | - | - | | - | P804 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | SD1DAT7_A | - | - | - | LCD_DATA00_B |
| N4 | 138 | N3 | 111 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| M4 | 139 | M3 | 112 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R3 | 140 | K4 | 113 | 76 | - | - | P500 | - | - | AGTOA0 | GTIU | GTIOC11A | - | USB_VBUSEN | - | - | - | QSPCLK | - | - | - | - | SD1CLK_A | AN016 | IVREF0 | - | - |
| P4 | 141 | M4 | 114 | 77 | - | IRQ11 | P501 | - | - | AGTOB0 | GTIV | GTIOC11B | - | USB_OVRCURA | - | TXD5/MOSI5/SDA5 | - | QSSL | - | - | - | - | SD1CMD_A | AN116 | IVREF1 | - | - |
| R4 | 142 | L4 | 115 | 78 | - | IRQ12 | P502 | - | - | - | GTIW | GTIOC12A | - | USB_OVRCURB | - | RXD5/MISO5/SCL5 | - | QIO0 | - | - | - | - | SD1DAT0_A | AN017 | IVCMP0 | - | - |
| N5 | 143 | K5 | 116 | 79 | - | - | P503 | - | - | - | GTETRGC | GTIOC12B | - | USB_EXICEN | CTS6_RTS6/SS6 | SCK5 | - | QIO1 | - | - | - | - | SD1DAT1_A | AN117 | - | - | - |
| P5 | 144 | L5 | 117 | 80 | - | - | P504 | ALE | - | - | GTETRGD | GTIOC13A | - | USB_ID | SCK6 | CTS5_RTS5/SS5 | - | QIO2 | - | - | - | - | SD1DAT2_A | AN018 | - | - | - |
| P6 | 145 | K6 | 118 | - | - | IRQ14 | P505 | - | - | - | - | GTIOC13B | - | - | RXD6/MISO6/SCL6 | - | - | QIO3 | - | - | - | - | SD1DAT3_A | AN118 | - | - | - |

| Pin number | | | | | | | | Extbus | | Timers | | | | Communication interfaces | | | | | | | | | | Analog | | HMI | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BGA176 | LQFP176 | LGA145 | LQFP144 | LQFP100 | Power, System, Clock, Debug, CAC | Interrupt | I/O port | External bus | SDRAM | AGT | GPT | GPT | RTC | USBFS, CAN | SCI0,2,4,6,8 (30 MHz) | SCI1,3,5,7,9 (30 MHz) | IIC | SPI, QSPI | SSIE | ETHERC (MII) (25 MHz) | ETHERC (RMII) (50 MHz) | USBHS | SDHI | ADC12 | DAC12, ACMPHS | CTSU | GLCDC, PDC |
| R5 | 146 | L6 | 119 | - | - | IRQ15 | P506 | - | - | - | - | - | - | - | TXD6/ MOSI6 /SDA6 | - | - | - | - | - | - | - | SD1 CD_ A | AN019 | - | - | - |
| N6 | 147 | - | - | - | - | - | P507 | - | - | - | - | - | - | - | - | CTS5_ RTS5/ SS5 | - | - | - | - | - | - | SD1 WP_ A | AN119 | - | - | - |
| R6 | 148 | N4 | 120 | 81 | - | - | P508 | - | - | - | - | - | - | - | SCK6 | SCK5 | - | - | - | - | - | - | - | AN020 | - | - | - |
| M7 | 149 | N5 | 121 | 82 | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| N7 | 150 | M5 | 122 | 83 | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| P7 | 151 | M6 | 123 | 84 | - | IRQ13 | P015 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN006/ AN106 | DA1/ IVCMP1 | - | - |
| R7 | 152 | N6 | 124 | 85 | - | - | P014 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN005/ AN105 | DA0/ IVREF3 | - | - |
| P8 | 153 | M7 | 125 | 86 | VREFL | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R8 | 154 | N7 | 126 | 87 | VREFH | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| N8 | 155 | L7 | 127 | 88 | AVCC0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| N9 | 156 | L8 | 128 | 89 | AVSS0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| P9 | 157 | M8 | 129 | 90 | VREFL0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| R9 | 158 | N8 | 130 | 91 | VREFH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| M8 | 159 | - | - | - | - | IRQ14 -DS | P010 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN103 | - | - | - |
| M9 | 160 | M9 | 131 | - | - | IRQ13 -DS | P009 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN004 | - | - | - |
| P10 | 161 | N9 | 132 | 92 | - | IRQ12 -DS | P008 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN003 | - | - | - |
| M6 | 162 | K7 | 133 | 93 | - | - | P007 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PGAVS S100/A N107 | - | - | - |
| N10 | 163 | L9 | 134 | 94 | - | IRQ11-DS | P006 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN102 | IVCMP2 | - | - |
| R10 | 164 | K8 | 135 | 95 | - | IRQ10 -DS | P005 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN101 | IVCMP2 | - | - |
| P11 | 165 | K9 | 136 | 96 | - | IRQ9-DS | P004 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN100 | IVCMP2 | - | - |
| M5 | 166 | K10 | 137 | 97 | - | - | P003 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PGAVS S000/A N007 | - | - | - |
| R11 | 167 | M10 | 138 | 98 | - | IRQ8-DS | P002 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN002 | IVCMP2 | - | - |
| N11 | 168 | N10 | 139 | 99 | - | IRQ7-DS | P001 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN001 | IVCMP2 | - | - |
| R12 | 169 | L10 | 140 | 100 | - | IRQ6-DS | P000 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | AN000 | IVCMP2 | - | - |
| M10 | 170 | N11 | 141 | - | VSS | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| M11 | 171 | N12 | 142 | - | VCC | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| P12 | 172 | - | - | - | - | - | P806 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_EXT CLK_B |
| R13 | 173 | - | - | - | - | - | P805 | - | - | - | - | - | - | - | - | TXD5 | - | - | - | - | - | - | - | - | - | - | LCD_DATA 17_B |
| N12 | 174 | - | - | - | - | - | P513 | - | - | - | - | - | - | - | - | RXD5 | - | - | - | - | - | - | - | - | - | - | LCD_DATA 16_B |
| R14 | 175 | M11 | 143 | - | - | IRQ14 | P512 | - | - | - | - | GTIOC 0A | - | CTX1 | TXD4/ MOSI4 /SDA4 | - | SCL2 | - | - | - | - | - | - | - | - | - | VSYNC |
| P13 | 176 | M12 | 144 | - | - | IRQ15 | P511 | - | - | - | - | GTIOC 0B | - | CRX1 | RXD4/ MISO4 /SCL4 | - | SDA2 | - | - | - | - | - | - | - | - | - | PCKO |

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix.

# 2. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr

Figure 2.1 shows the timing conditions.

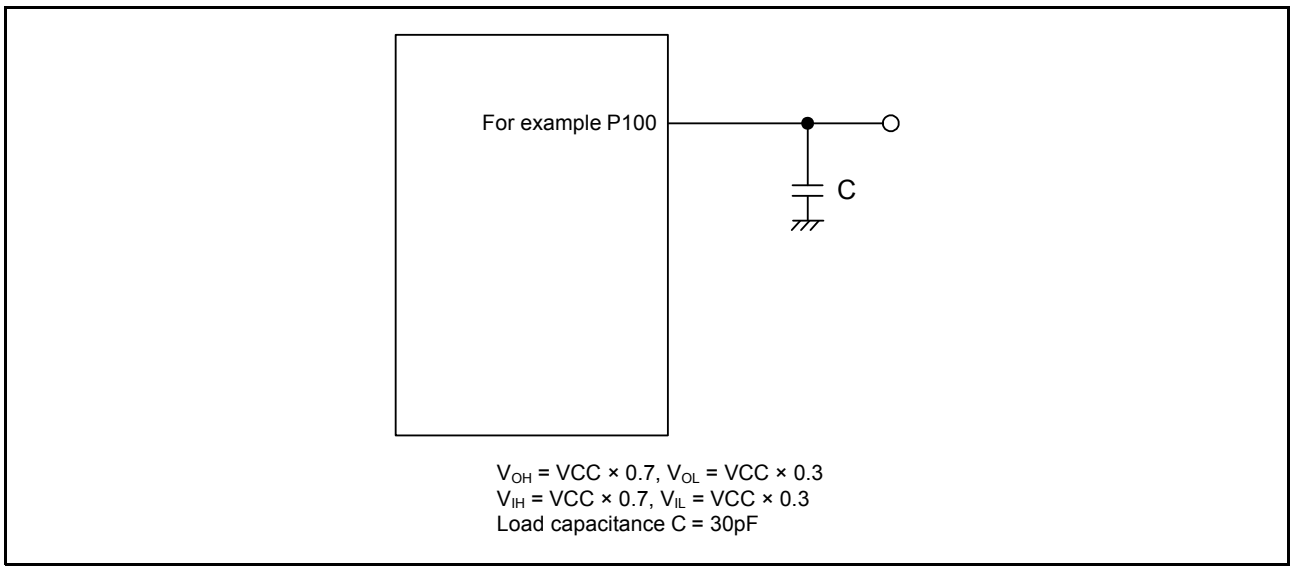


**Figure 2.1 Input or output timing measurement conditions**

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

## 2.1 Absolute Maximum Ratings

**Table 2.1 Absolute maximum ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | VCC, VCC_USB *2 | –0.3 to +4.0 | V |
| VBATT power supply voltage | VBATT | –0.3 to +4.0 | V |
| Input voltage (except for 5V-tolerant ports*1) | $V_{in}$ | –0.3 to VCC + 0.3 | V |
| Input voltage (5V-tolerant ports*1) | $V_{in}$ | –0.3 to + VCC + 4.0 (max 5.8) | V |
| Reference power supply voltage | VREFH/VREFH0 | –0.3 to VCC + 0.3 | V |
| Analog power supply voltage | AVCC0 *2 | –0.3 to +4.0 | V |
| USBHS power supply voltage | VCC_USBHS | –0.3 to +4.0 | V |
| USBHS analog power supply voltage | AVCC_USBHS | –0.3 to +4.0 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to AVCC0 + 0.3 | V |
| Operating temperature*3,*4,*5 | $T_{opr}$ | –40 to +85<br>–40 to +105 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

**Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.**

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 2.2.1, $T_j/T_a$ Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when $T_a$ = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.

**Table 2.7 Operating and standby current (2 of 2)**

| Item | | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|
| USB operating current | Low speed | USB | $I_{CCUSBLS}$ | - | 3.5 | 6.5 | mA | VCC_USB |
| | | USBHS | | - | 10.5 | 13.5 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0) |
| | | USBHS | | - | 2.8 | 3.6 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1) |
| | Full speed | USB | $I_{CCUSBFS}$ | - | 4.0 | 10.0 | mA | VCC_USB |
| | | USBHS | | - | 14 | 22 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0) |
| | | USBHS | | - | 6.5 | 13.0 | mA | VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1) |
| | High speed | USBHS | $I_{CCUSBHS}$ | - | 50 | 65 | mA | VCC_USBHS = AVCC_USBHS |
| | Standby mode (direct power down) | USBHS | $I_{CCUSBSBY}$ | - | 0.5 | 4.5 | µA | VCC_USBHS = AVCC_USBHS |

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. ICC depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)
ICC Max. = 0.84 × f + 37 (max. operation in High-speed mode)
ICC Typ. = 0.09 × f + 3.7 (normal operation in High-speed mode)
ICC Typ. = 0.6 × f + 1.8 (Low-speed mode 1)
ICC Max. = 0.08 × f + 37 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When using ETHERC, GLCDC, DRW, and JPEG, PCLKA frequency is such that PCLKA = ICLK.
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 module stop bit) and MSTPCRD.MSTPD15 (ADC121 module stop bit) are in the module stop state.

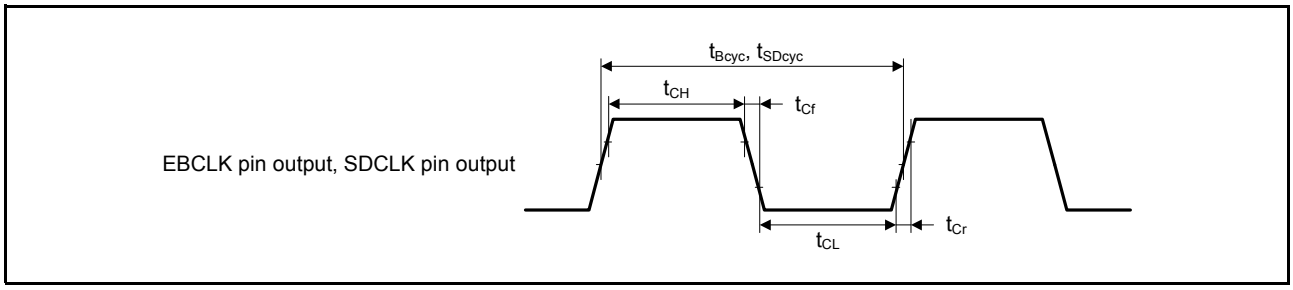


**Figure 2.3 EBCLK and SDCLK output timing**

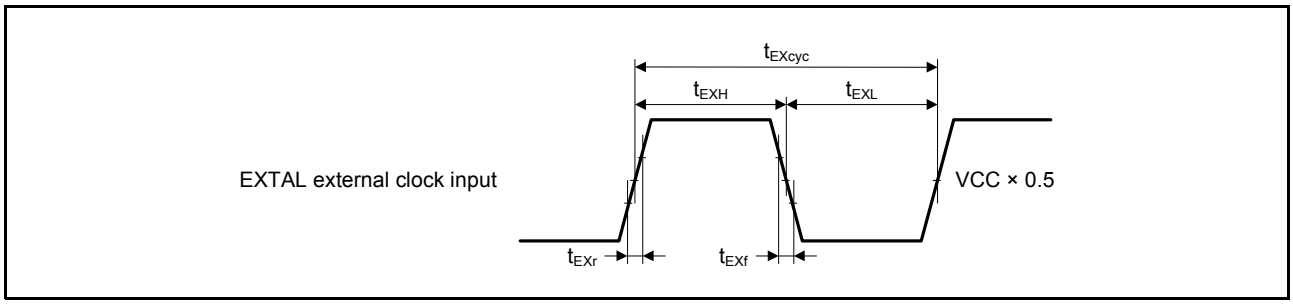


**Figure 2.4 EXTAL external clock input timing**

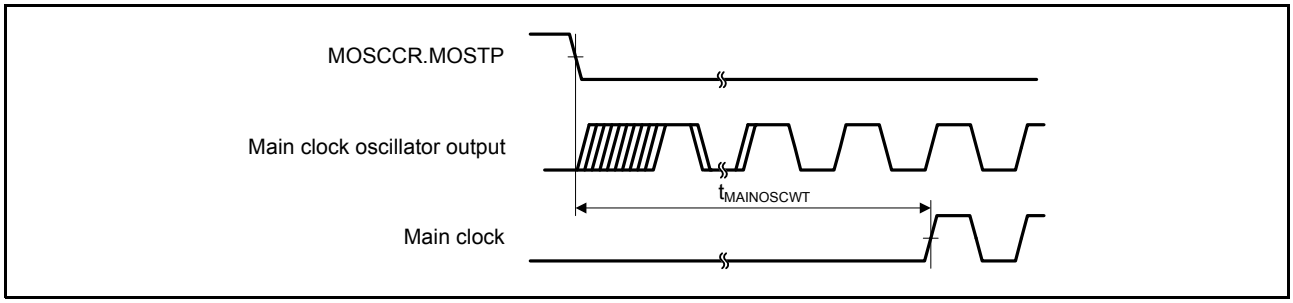


**Figure 2.5 Main clock oscillation start timing**

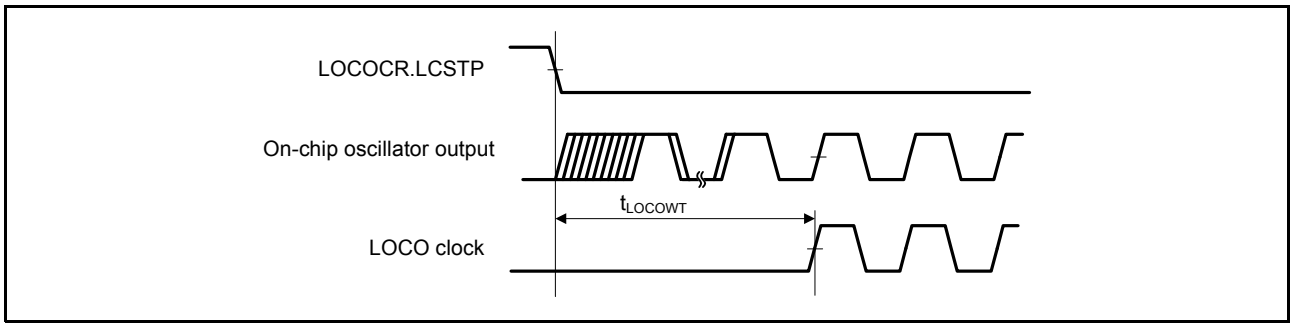


**Figure 2.6 LOCO clock oscillation start timing**

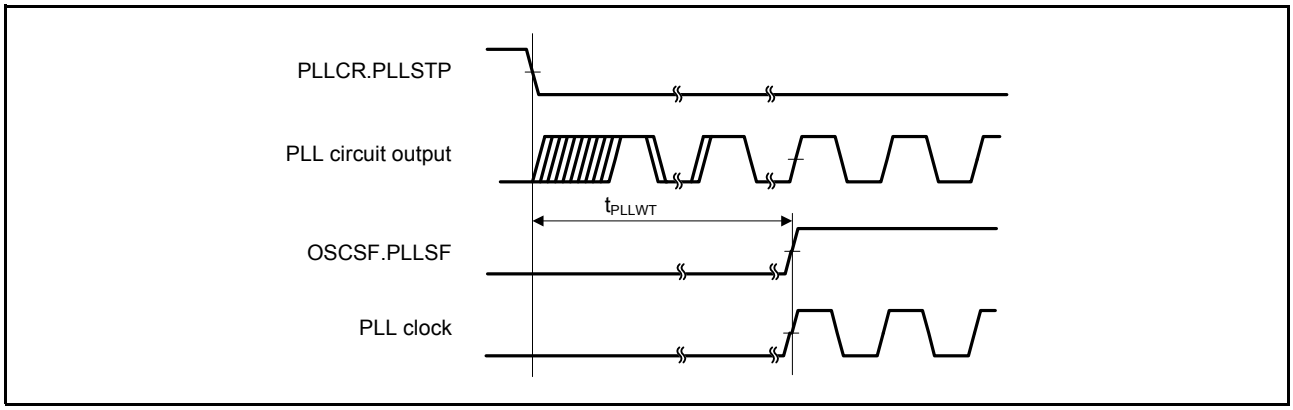


**Figure 2.7 PLL clock oscillation start timing**

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

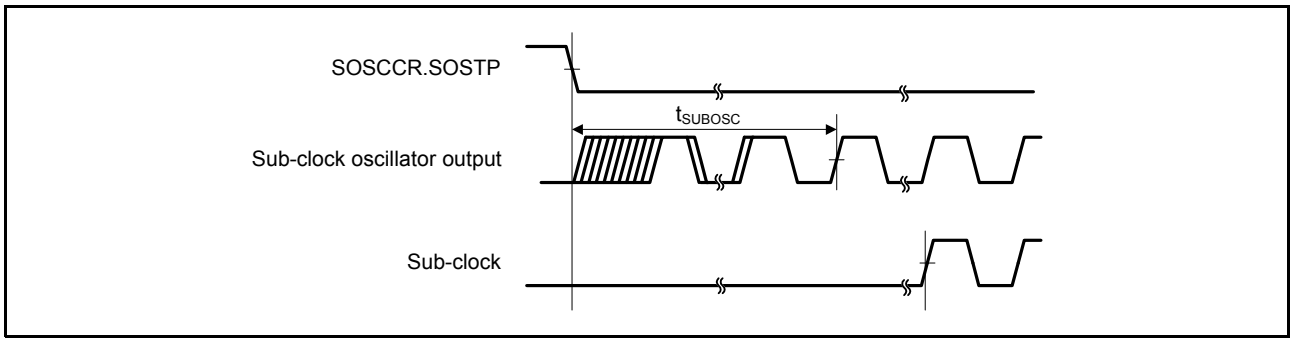


**Figure 2.8 Sub-clock oscillation start timing**

### 2.3.3 Reset Timing

**Table 2.15 Reset timing**

| Item | | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|---|
| RES pulse width | Power-on | $t_{RESWP}$ | 1 | - | - | ms | Figure 2.9 |
| | Deep Software Standby mode | $t_{RESWD}$ | 0.6 | - | - | ms | Figure 2.10 |
| | Software Standby mode, Subosc-speed mode | $t_{RESWS}$ | 0.3 | - | - | ms | |
| | All other | $t_{RESW}$ | 200 | - | - | µs | |
| Wait time after RES cancellation | | $t_{RESWT}$ | - | 29 | 33 | µs | Figure 2.9 |
| Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset) | | $t_{RESW2}$ | - | 320 | 408 | µs | - |

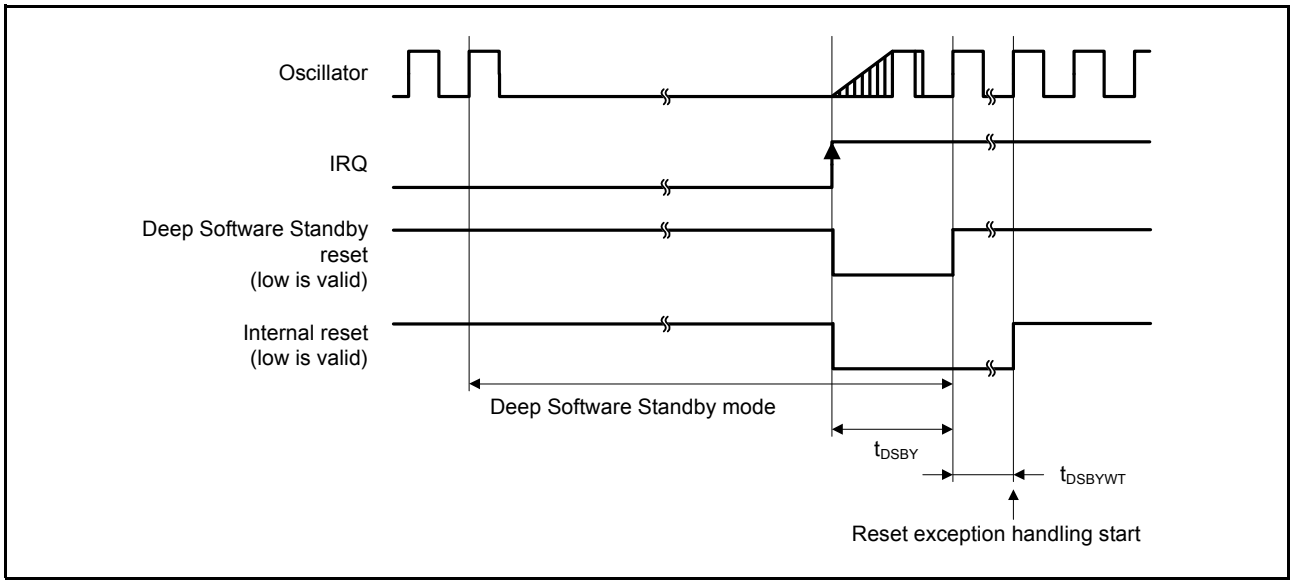


**Figure 2.12 Deep Software Standby mode cancellation timing**

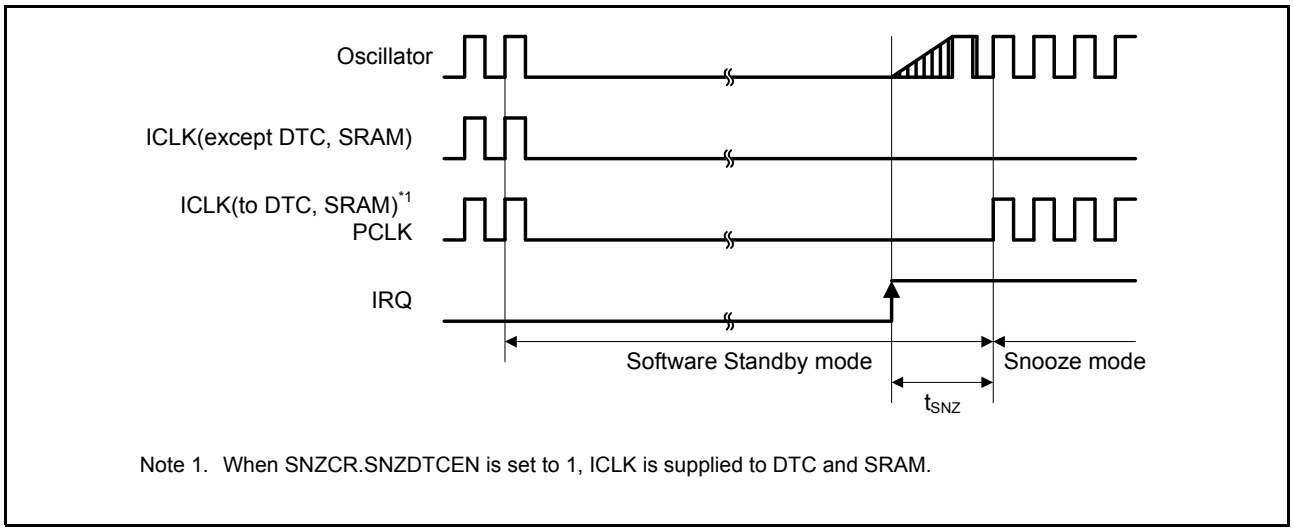


**Figure 2.13 Recovery timing from Software Standby mode to Snooze mode**

## 2.3.5 NMI and IRQ Noise Filter

**Table 2.17 NMI and IRQ noise filter**

| Item | Symbol | Min | Typ | Max | Unit | Test conditions | |
|---|---|---|---|---|---|---|---|
| NMI pulse width | $t_{NMIW}$ | 200 | - | - | ns | NMI digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | NMI digital filter enabled | $t_{NMICK} \times 3 \leq 200$ ns |
| | | $t_{NMICK} \times 3.5$*2 | - | - | | | $t_{NMICK} \times 3 > 200$ ns |
| IRQ pulse width | $t_{IRQW}$ | 200 | - | - | ns | IRQ digital filter disabled | $t_{Pcyc} \times 2 \leq 200$ ns |
| | | $t_{Pcyc} \times 2$*1 | - | - | | | $t_{Pcyc} \times 2 > 200$ ns |
| | | 200 | - | - | | IRQ digital filter enabled | $t_{IRQCK} \times 3 \leq 200$ ns |
| | | $t_{IRQCK} \times 3.5$*3 | - | - | | | $t_{IRQCK} \times 3 > 200$ ns |

Note: 200 ns minimum in Software Standby mode.
Note 1. $t_{Pcyc}$ indicates the PCLKB cycle.

Note 2. $t_{NMICK}$ indicates the cycle of the NMI digital filter sampling clock.
Note 3. $t_{IRQCK}$ indicates the cycle of the IRQi digital filter sampling clock.

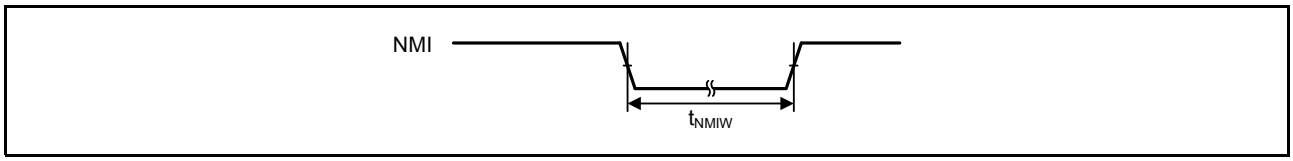


**Figure 2.14 NMI interrupt input timing**

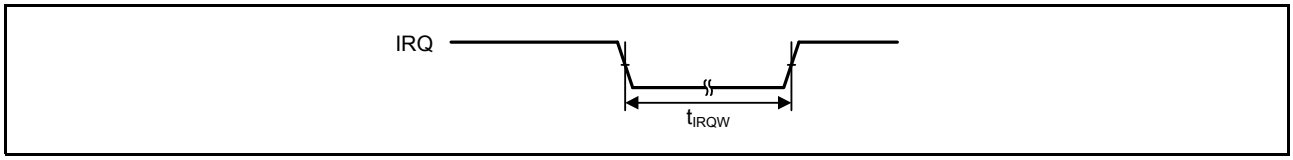


**Figure 2.15 IRQ interrupt input timing**

## 2.3.6 Bus Timing

**Table 2.18 Bus timing (1 of 2)**
Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | Symbol | Min | Max | Unit | Test conditions |
|---|---|---|---|---|---|
| Address delay | $t_{AD}$ | - | 12.5 | ns | Figure 2.18 to Figure 2.21 |
| Byte control delay | $t_{BCD}$ | - | 12.5 | ns | |
| CS delay | $t_{CSD}$ | - | 12.5 | ns | |
| ALE delay time | $t_{ALED}$ | - | 12.5 | ns | |
| RD delay | $t_{RSD}$ | - | 12.5 | ns | |
| Read data setup time | $t_{RDS}$ | 12.5 | - | ns | |
| Read data hold time | $t_{RDH}$ | 0 | - | ns | |
| WR/WRn delay | $t_{WRD}$ | - | 12.5 | ns | |
| Write data delay | $t_{WDD}$ | - | 12.5 | ns | |
| Write data hold time | $t_{WDH}$ | 0 | - | ns | |
| WAIT setup time | $t_{WTS}$ | 12.5 | - | ns | Figure 2.22 |
| WAIT hold time | $t_{WTH}$ | 0 | - | ns | |

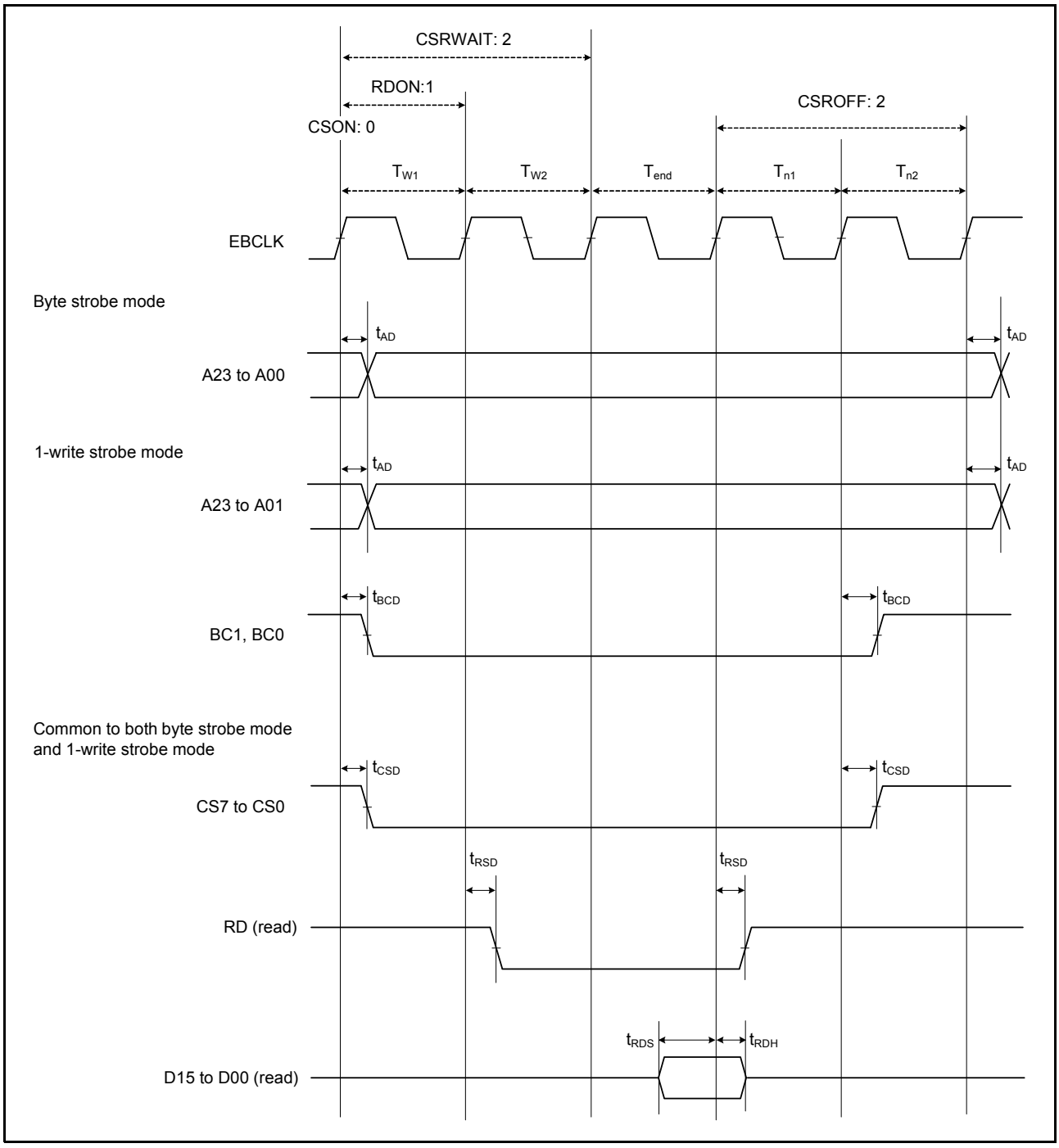


**Figure 2.18 External bus timing for normal read cycle with bus clock synchronized**

Note 1. $t_{PBcyc}$: PCLKB cycle.
Note 2. $t_{cac}$: CAC count clock source cycle.

## 2.3.10 SCI Timing

**Table 2.22 SCI timing (1)**
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

| Item | | | Symbol | Min | Max | Unit*1 | Test conditions |
|---|---|---|---|---|---|---|---|
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | - | $t_{Pcyc}$ | Figure 2.39 |
| | | Clock synchronous | | 6 | - | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | - | 5 | ns | |
| | Input clock fall time | | $t_{SCKf}$ | - | 5 | ns | |
| | Output clock cycle | Asynchronous | $t_{Scyc}$ | 6 | - | $t_{Pcyc}$ | |
| | | Clock synchronous | | 4 | - | | |
| | Output clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Output clock rise time | | $t_{SCKr}$ | - | 5 | ns | |
| | Output clock fall time | | $t_{SCKf}$ | - | 5 | ns | |
| | Transmit data delay | Clock synchronous | $t_{TXD}$ | - | 25 | ns | Figure 2.40 |
| | Receive data setup time | Clock synchronous | $t_{RXS}$ | 15 | - | ns | |
| | Receive data hold time | Clock synchronous | $t_{RXH}$ | 5 | - | ns | |

Note 1. $t_{Pcyc}$: PCLKA cycle.

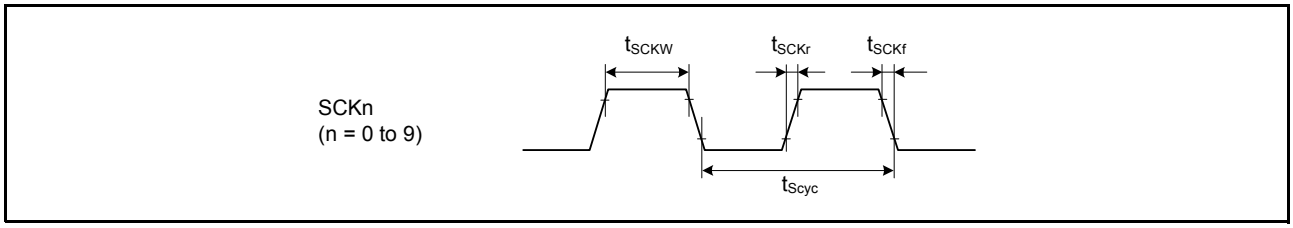


**Figure 2.39 SCK clock input/output timing**

**Table 2.27 IIC timing (1) (2 of 2)**

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

| Item | | Symbol | Min*1 | Max | Unit | Test conditions*3 |
|---|---|---|---|---|---|---|
| IIC (Fast mode) | SCL input cycle time | $t_{SCL}$ | 6 (12) × $t_{IICcyc}$ + 600 | - | ns | Figure 2.56 |
| | SCL input high pulse width | $t_{SCLH}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL input low pulse width | $t_{SCLL}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SCL, SDA input rise time | $t_{Sr}$ | 20 × (external pullup voltage/5.5V)*2 | 300 | ns | |
| | SCL, SDA input fall time | $t_{Sf}$ | 20 × (external pullup voltage/5.5V)*2 | 300 | ns | |
| | SCL, SDA input spike pulse removal time | $t_{SP}$ | 0 | 1 (4) × $t_{IICcyc}$ | ns | |
| | SDA input bus free time when wakeup function is disabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 300 | - | ns | |
| | SDA input bus free time when wakeup function is enabled | $t_{BUF}$ | 3 (6) × $t_{IICcyc}$ + 4 × $t_{Pcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is disabled | $t_{STAH}$ | $t_{IICcyc}$ + 300 | - | ns | |
| | START condition input hold time when wakeup function is enabled | $t_{STAH}$ | 1 (5) × $t_{IICcyc}$ + $t_{Pcyc}$ + 300 | - | ns | |
| | Repeated START condition input setup time | $t_{STAS}$ | 300 | - | ns | |
| | STOP condition input setup time | $t_{STOS}$ | 300 | - | ns | |
| | Data input setup time | $t_{SDAS}$ | $t_{IICcyc}$ + 50 | - | ns | |
| | Data input hold time | $t_{SDAH}$ | 0 | - | ns | |
| | SCL, SDA capacitive load | $C_b$ | - | 400 | pF | |

Note: $t_{IICcyc}$: IIC internal reference clock (IICφ) cycle, $t_{Pcyc}$: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.
Note 3. Must use pins that have a letter ("_A", "_B") to indicate group membership appended to their name as groups. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

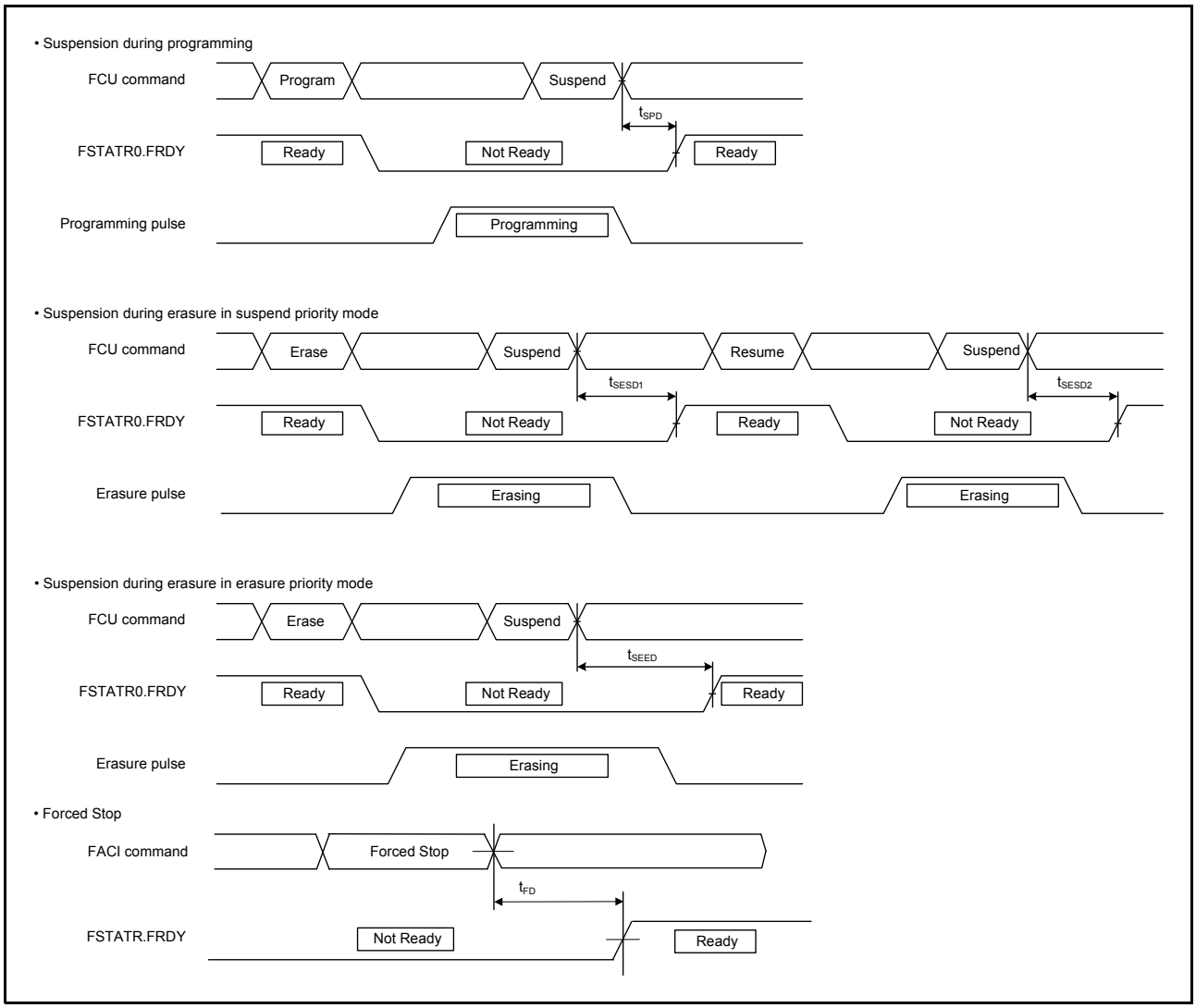


**Figure 2.98 Suspension and forced stop timing for flash memory programming and erasure**

## 2.14.2 Data Flash Memory Characteristics

**Table 2.54 Data flash memory characteristics (1 of 2)**
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

| Item | | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | Test conditions |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | | |
| Programming time | 4-byte | $t_{DP4}$ | - | 0.46 | 3.8 | - | 0.21 | 1.7 | ms | |
| | 8-byte | $t_{DP8}$ | - | 0.48 | 4.0 | - | 0.22 | 1.8 | | |
| | 16-byte | $t_{DP16}$ | - | 0.53 | 4.5 | - | 0.24 | 2.0 | | |
| Erasure time | 64-byte | $t_{DE64}$ | - | 4.03 | 18 | - | 2.24 | 10 | ms | |
| | 128-byte | $t_{DE128}$ | - | 6.2 | 27 | - | 3.4 | 15 | | |
| | 256-byte | $t_{DE256}$ | - | 11.6 | 50 | - | 6.4 | 28 | | |
| Blank check time | 4-byte | $t_{DBC4}$ | - | - | 84 | - | - | 30 | µs | |
| Reprogramming/erasure cycle*1 | | $N_{DPEC}$ | 125000 *2 | - | - | 125000 *2 | - | - | - | |

## 2.17 Serial Wire Debug (SWD)

**Table 2.57 SWD**

| Item | Symbol | Min | Typ | Max | Unit | Test conditions |
|---|---|---|---|---|---|---|
| SWCLK clock cycle time | $t_{SWCKcyc}$ | 40 | - | - | ns | Figure 2.104 |
| SWCLK clock high pulse width | $t_{SWCKH}$ | 15 | - | - | ns | |
| SWCLK clock low pulse width | $t_{SWCKL}$ | 15 | - | - | ns | |
| SWCLK clock rise time | $t_{SWCKr}$ | - | - | 5 | ns | |
| SWCLK clock fall time | $t_{SWCKf}$ | - | - | 5 | ns | |
| SWDIO setup time | $t_{SWDS}$ | 8 | - | - | ns | Figure 2.105 |
| SWDIO hold time | $t_{SWDH}$ | 8 | - | - | ns | |
| SWDIO data delay time | $t_{SWDD}$ | 2 | - | 28 | ns | |

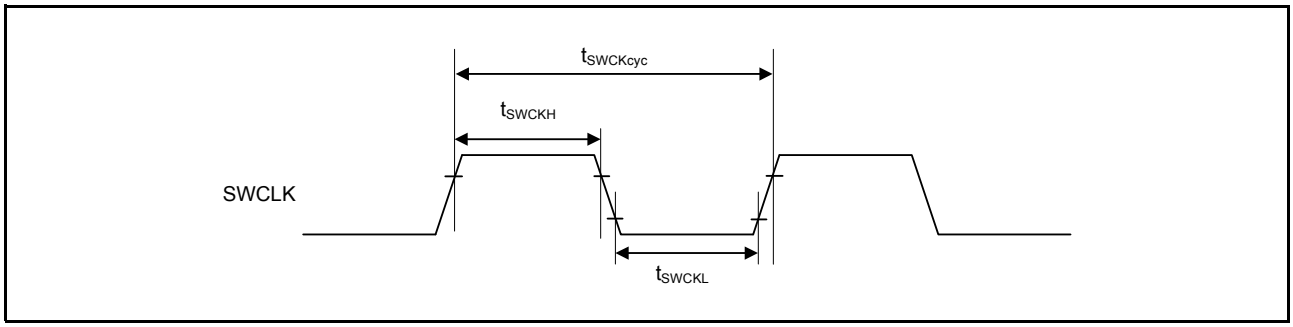


**Figure 2.104 SWD SWCLK timing**

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