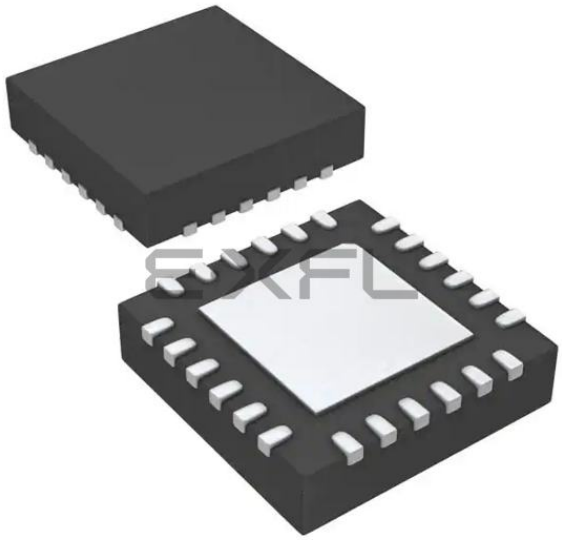

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke04z8vfk4r

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **freescale.com** and perform a part number search for the following device numbers: KE04Z.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE04
A	Key attribute	• Z = M0+ core
FFF	Program flash memory size	• 8 = 8 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• TG = 16 TSSOP (4.5 mm x 5 mm)

Table continues on the next page...

circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 2. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3[1]	V
	Input voltage of true open drain pins	–0.3	6	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum rating of V_{DD} also applies to V_{IN}.

5 General

5.1 Nonswitching electrical specifications

5.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 3. DC characteristics

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
—	—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	P	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, I_{load} = –5 mA	V_{DD} – 0.8	—	—	V
	C			3 V, I_{load} = –2.5 mA	V_{DD} – 0.8	—	—	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} = –20 mA	V_{DD} – 0.8	—	—	V
	C			3 V, I_{load} = –10 mA	V_{DD} – 0.8	—	—	V
I_{OHT}	D	Output high current	Max total I_{OH} for all ports	5 V	—	—	–100	mA
				3 V	—	—	–60	
V_{OL}	P	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
	C			3 V, I_{load} = 2.5 mA	—	—	0.8	V
	P		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
	C			3 V, I_{load} = 10 mA	—	—	0.8	V

Table continues on the next page...

Table 3. DC characteristics (continued)

Symbol	C	Descriptions			Min	Typical[1]	Max	Unit
I_{OLT}	D	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
				3 V	—	—	60	
V_{IH}	P	Input high voltage	All digital inputs	$4.5 \le V_{DD} < 5.5$ V	$0.65 \times V_{DD}$	—	—	V
				$2.7 \le V_{DD} < 4.5$ V	$0.70 \times V_{DD}$	—	—	
V_{IL}	P	Input low voltage	All digital inputs	$4.5 \le V_{DD} < 5.5$ V	—	—	$0.35 \times V_{DD}$	V
				$2.7 \le V_{DD} < 4.5$ V	—	—	$0.30 \times V_{DD}$	
V_{hys}	C	Input hysteresis	All digital inputs	—	$0.06 \times V_{DD}$	—	—	mV
$\lvert I_{In} \rvert$	P	Input leakage current	Per pin (pins in high impedance input mode)	$V_{IN} = V_{DD}$ or V_{SS}	—	0.1	1	µA
$\lvert I_{INTOT} \rvert$	C	Total leakage combined for all port pins	Pins in high impedance input mode	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	µA
R_{PU}	P	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	P	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	kΩ
I_{IC}	D	DC injection current[4, 5, 6]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
			Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	C	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	C	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB5, PTC1 and PTC5 support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

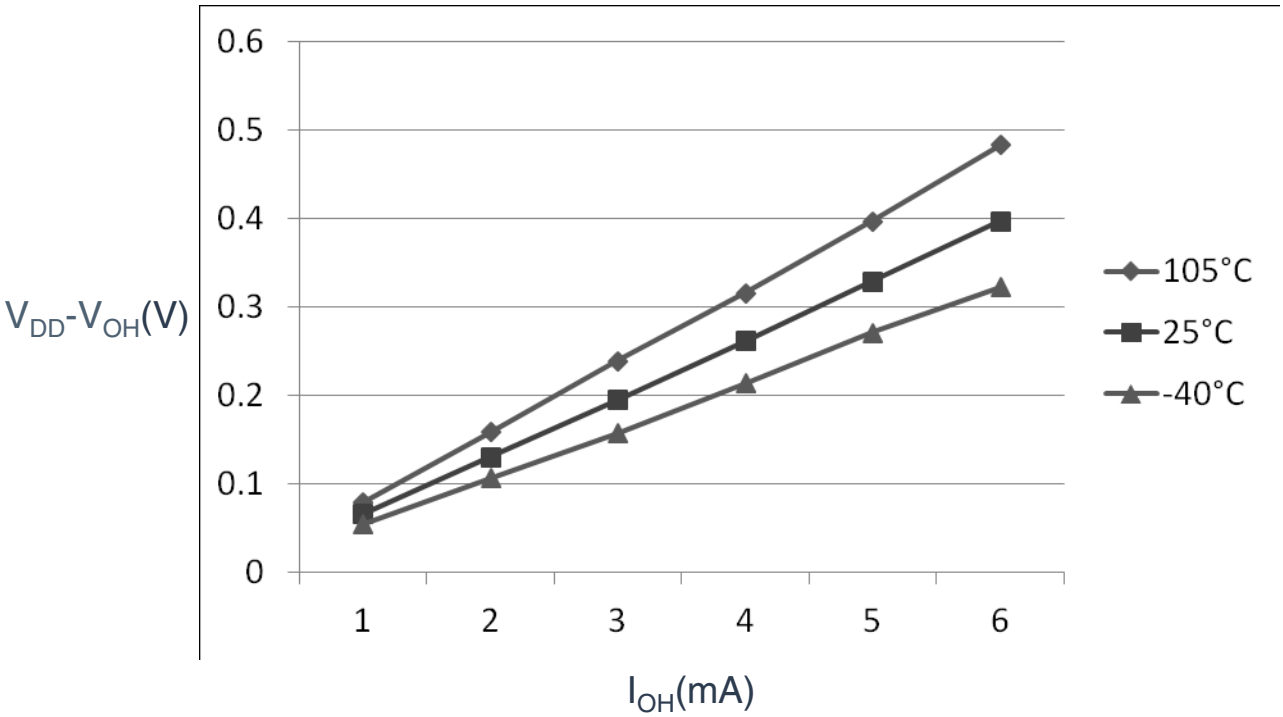

Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

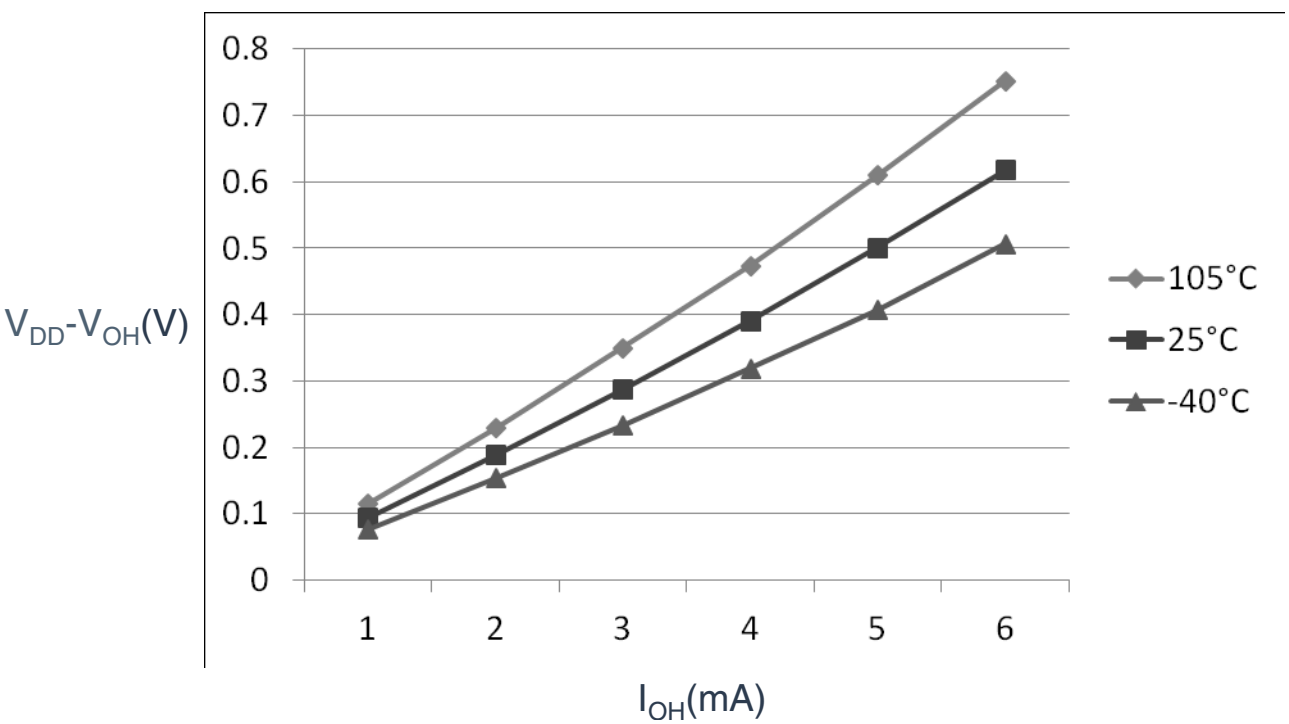

Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

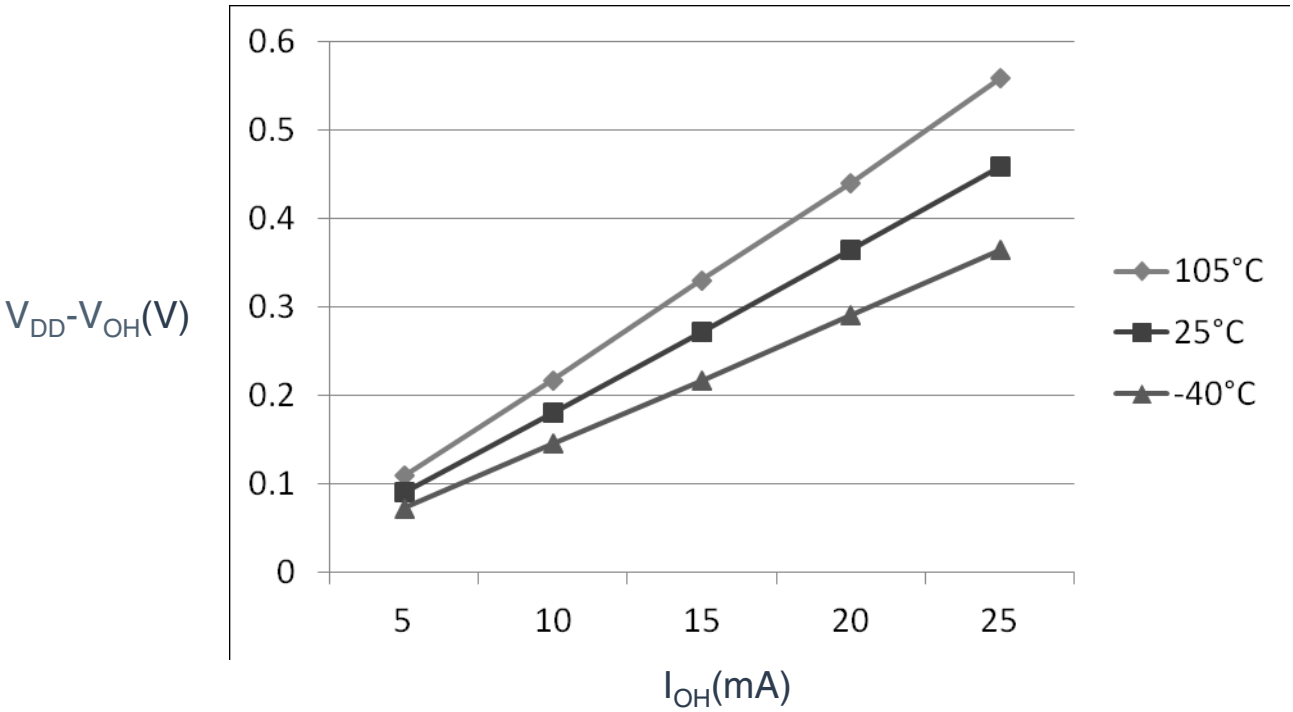

Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

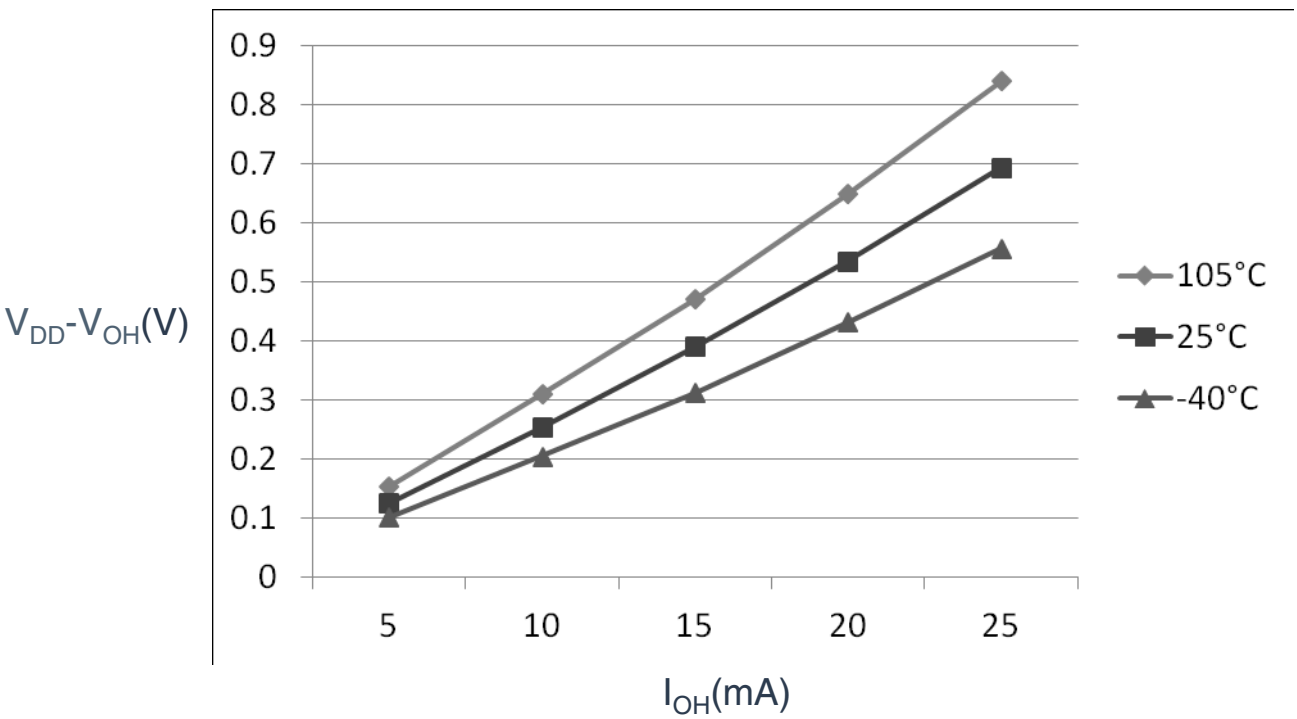

Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

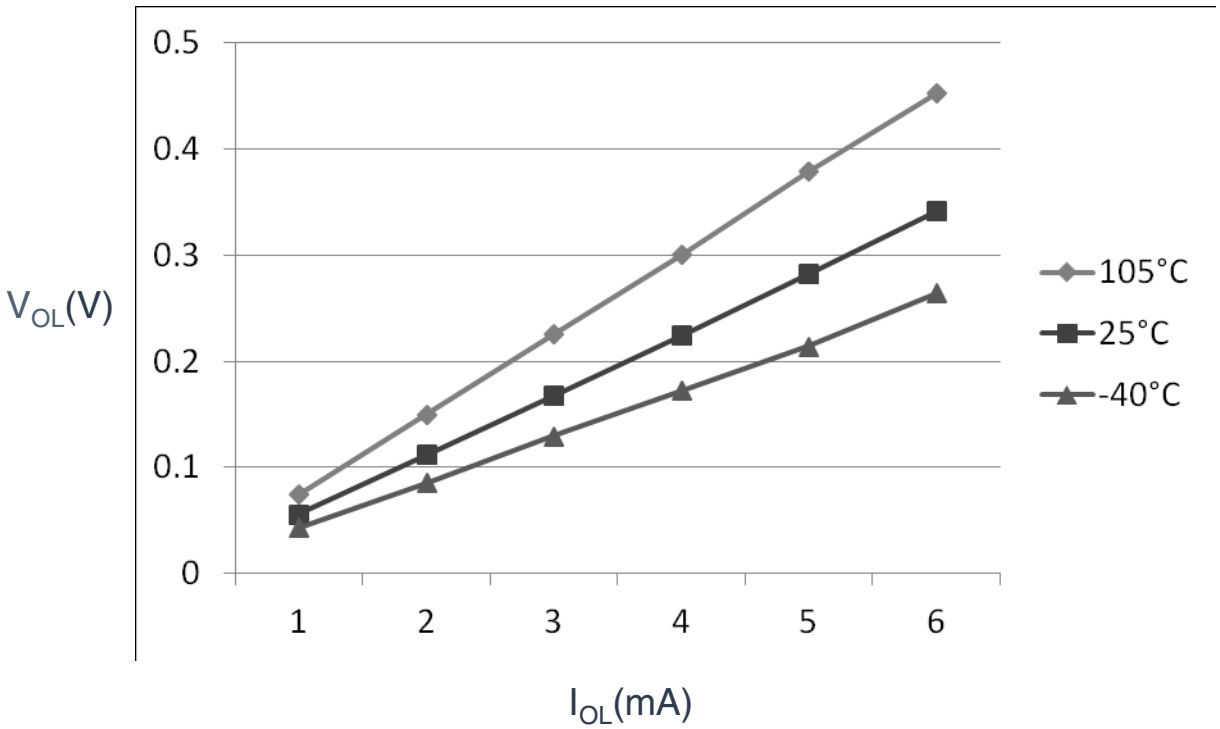

Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

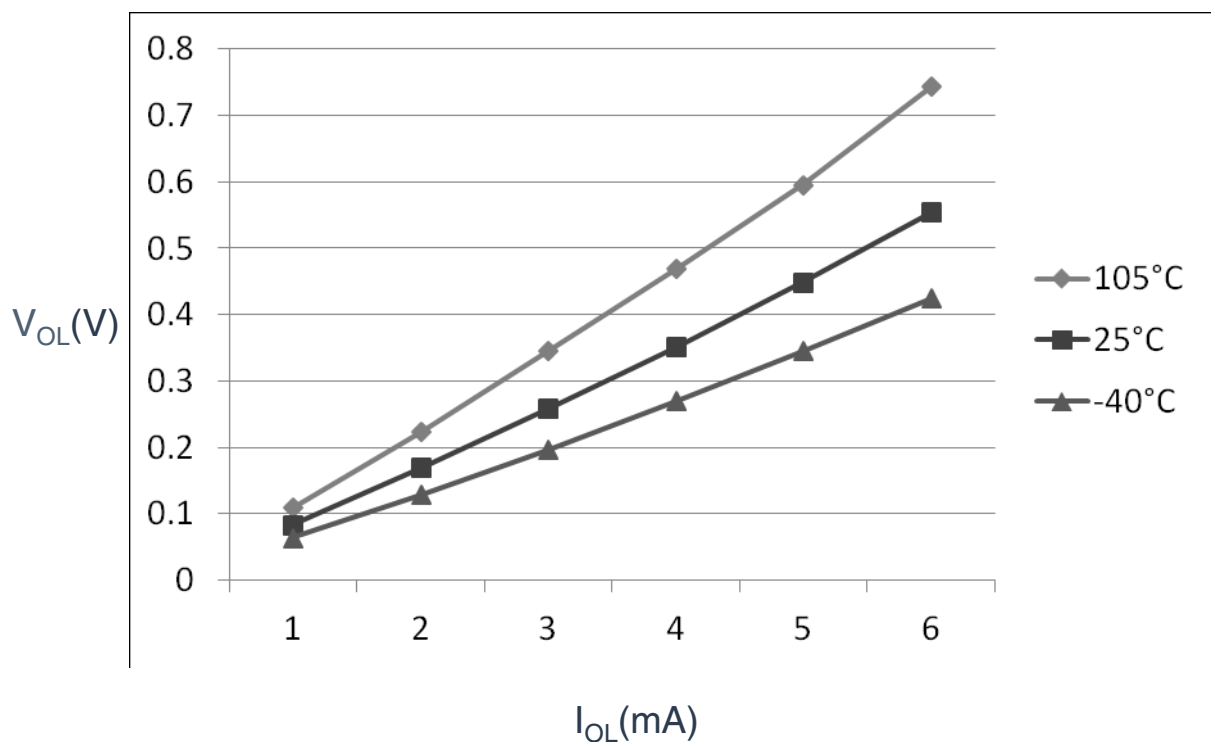

Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

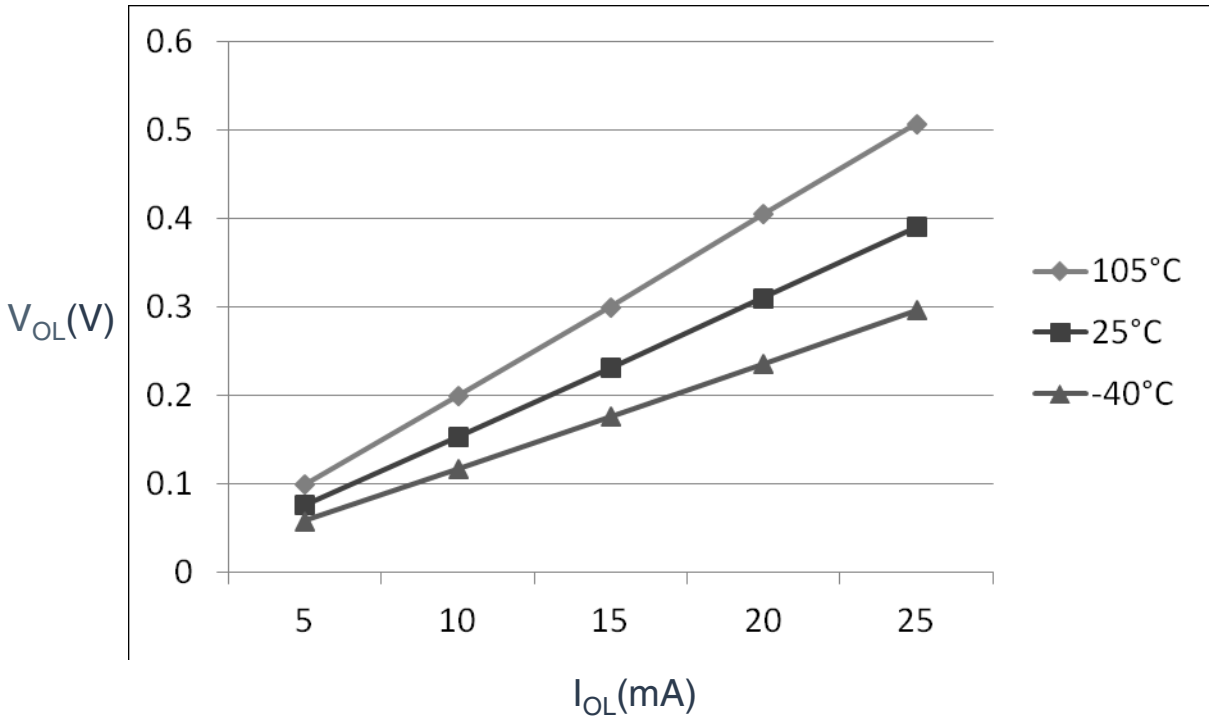

Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

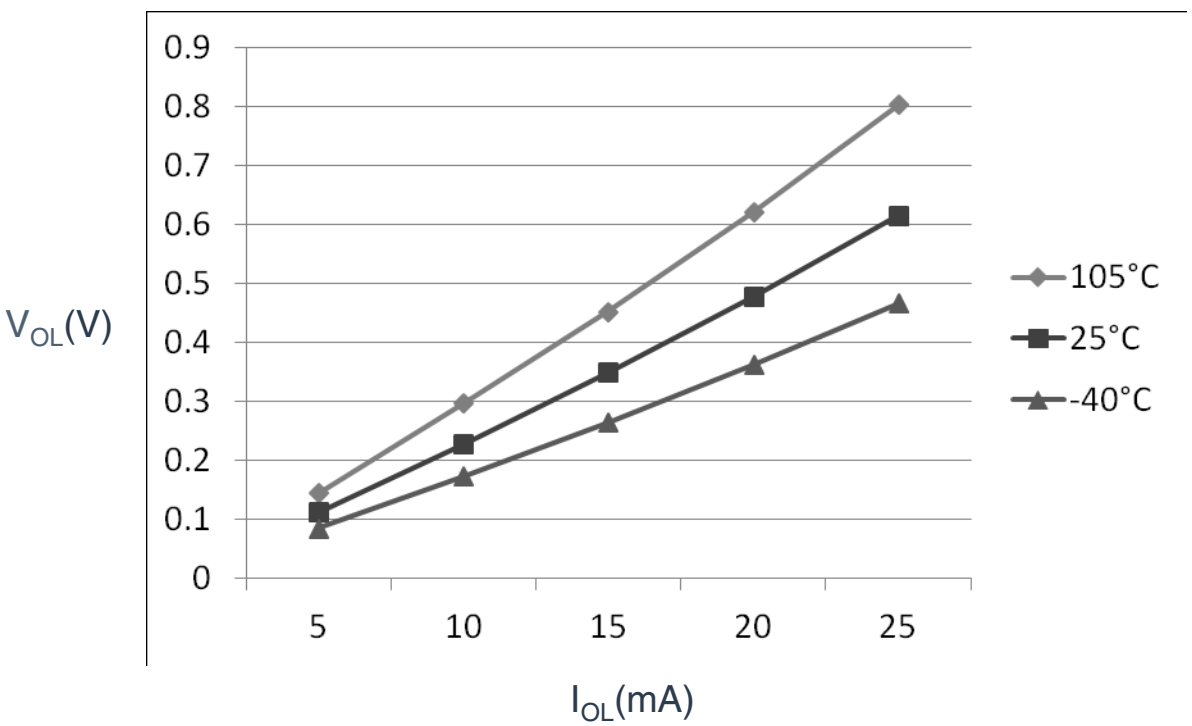

Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	48/24 MHz	5	10.1	—	mA	-40 to 105 °C
C			24/24 MHz		7.1	—		
C			12/12 MHz		4.4	—		
C			1/1 MHz		2.1	—		
C			48/24 MHz	3	9.9	—		
C			24/24 MHz		6.9	—		
C			12/12 MHz		4.2	—		
			1/1 MHz		1.9	—		
C	Run supply current FEI mode, all modules clocks disabled and gated; run from flash	RI_{DD}	48/24 MHz	5	7.4	—	mA	-40 to 105 °C
C			24/24 MHz		5.2	—		
C			12/12 MHz		3.5	—		
C			1/1 MHz		2	—		
C			48/24 MHz	3	7.2	—		
C			24/24 MHz		5	—		
C			12/12 MHz		3.3	—		
C			1/1 MHz		1.8	—		
C	Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	48/24 MHz	5	13.2	—	mA	-40 to 105 °C
P			24/24 MHz		9.1	9.5		
C			12/12 MHz		5.1	—		
C			1/1 MHz		1.8	—		
C			48/24 MHz	3	13	—		
P			24/24 MHz		9	9.4		
C			12/12 MHz		5	—		
C			1/1 MHz		1.7	—		
C	Run supply current FBE mode, all modules clocks disabled and gated; run from RAM	RI_{DD}	48/24 MHz	5	10.6	—	mA	-40 to 105 °C
P			24/24 MHz		7.6	7.8		
C			12/12 MHz		4.3	—		
C			1/1 MHz		1.7	—		
C			48/24 MHz	3	10.5	—		
P			24/24 MHz		7.5	7.7		
C			12/12 MHz		4.2	—		
			1/1 MHz		1.6	—		

Table continues on the next page...

Table 5. Supply current characteristics (continued)

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	48/24 MHz	5	7.2	—	mA	-40 to 105 °C
P			24/24 MHz		6.3	6.5		
C			12/12 MHz		3.6	—		
C			1/1 MHz		1.9	—		
C			48/24 MHz	3	7.1	—		
P			24/24 MHz		6.2	6.4		
C			12/12 MHz		3.5	—		
C			1/1 MHz		1.8	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	40	µA	-40 to 105 °C
P			—	3	1.9	39		-40 to 105 °C
C	ADC adder to Stop	—	—	5	86	—	µA	-40 to 105 °C
C	ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B			3	82	—		
C	ACMP adder to Stop	—	—	5	12	—	µA	-40 to 105 °C
C				3	12	—		
C	LVD adder to Stop[4]	—	—	5	130	—	µA	-40 to 105 °C
C				3	125	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. The Max current is observed at high temperature of 105 °C.
3. RTC adder cause <1 µA I_{DD} increase typically, RTC clock source is 1 kHz LPO clock.
4. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

5.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following Freescale applications notes, available on **freescale.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

Table 8. FTM input timing (continued)

C	Function	Symbol	Min	Max	Unit
D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

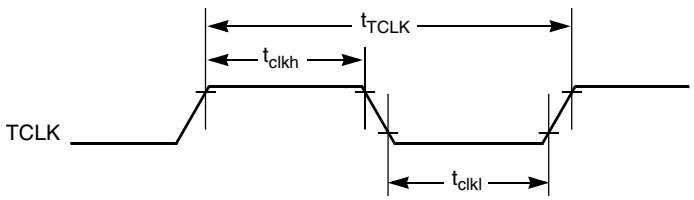

Figure 11. Timer external clock

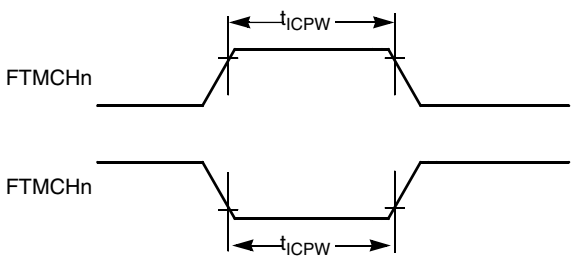

Figure 12. Timer input capture pulse

5.3 Thermal specifications

5.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 9. Thermal attributes

Board type	Symbol	Description	24 QFN	20 SOIC	16 TSSOP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	110	88	130	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42	61	87	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	92	74	109	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	36	55	80	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	18	34	48	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	3.7	37	33	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	10	20	10	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C)$$

Solving the equations above for K gives:

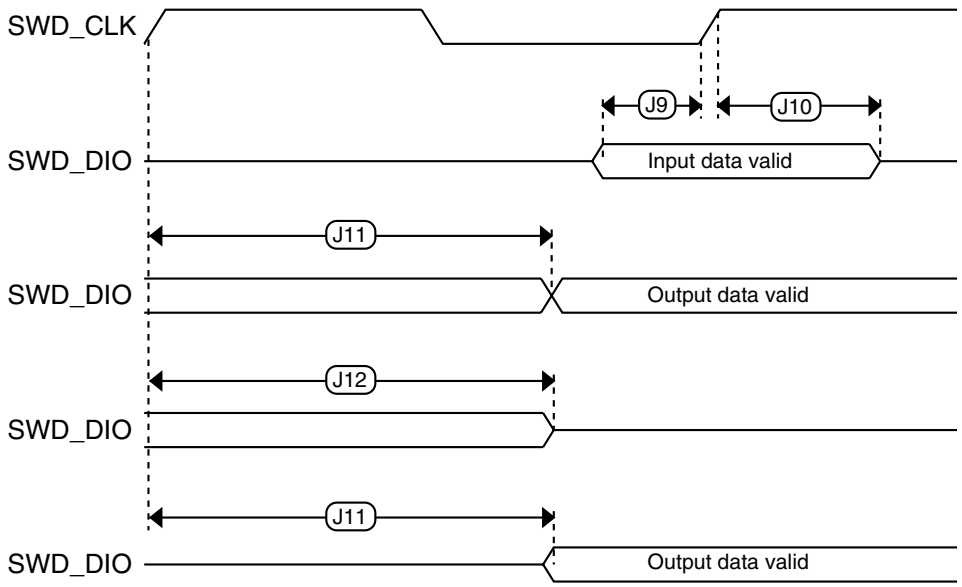

Figure 14. Serial wire data timing

6.2 External oscillator (OSC) and ICS characteristics

Table 11. OSC and ICS specifications (temperature range = -40 to 105 °C ambient)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	C	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
	C		High range (RANGE = 1)	f_{hi}	4	—	24	MHz
2	D	Load capacitors		C1, C2	See Note[2]			
3	D	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
			Low Frequency, High-Gain Mode		—	10	—	MΩ
			High Frequency, Low-Power Mode		—	1	—	MΩ
			High Frequency, High-Gain Mode		—	1	—	MΩ
4	D	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
			High-Gain Mode		—	200	—	kΩ
5	D	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ

Table continues on the next page...

Table 11. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	P	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	37.5	—	kHz
10	P	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	40	—	50	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 105°C	Δf_{int_t}	-1.2	—	1	%
			Over temperature range from 0 °C to 105°C	Δf_{int_t}	-0.5	—	1	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	Δf_{dco_ft}	-1.7	—	1.5	%
			Over temperature range from 0 °C to 105°C	Δf_{dco_ft}	-1	—	1.5	
14	C	FLL acquisition time[4,6]		$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

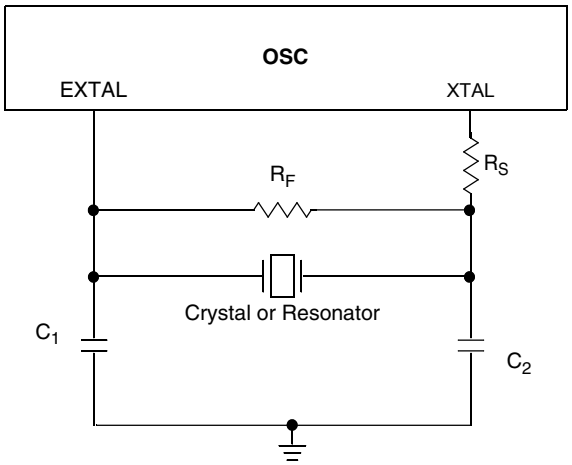

Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash memories.

Table 12. Flash characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase –40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f_{NVMBUS}	1	—	24	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	464	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
D	Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
D	Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
D	Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles

Table continues on the next page...

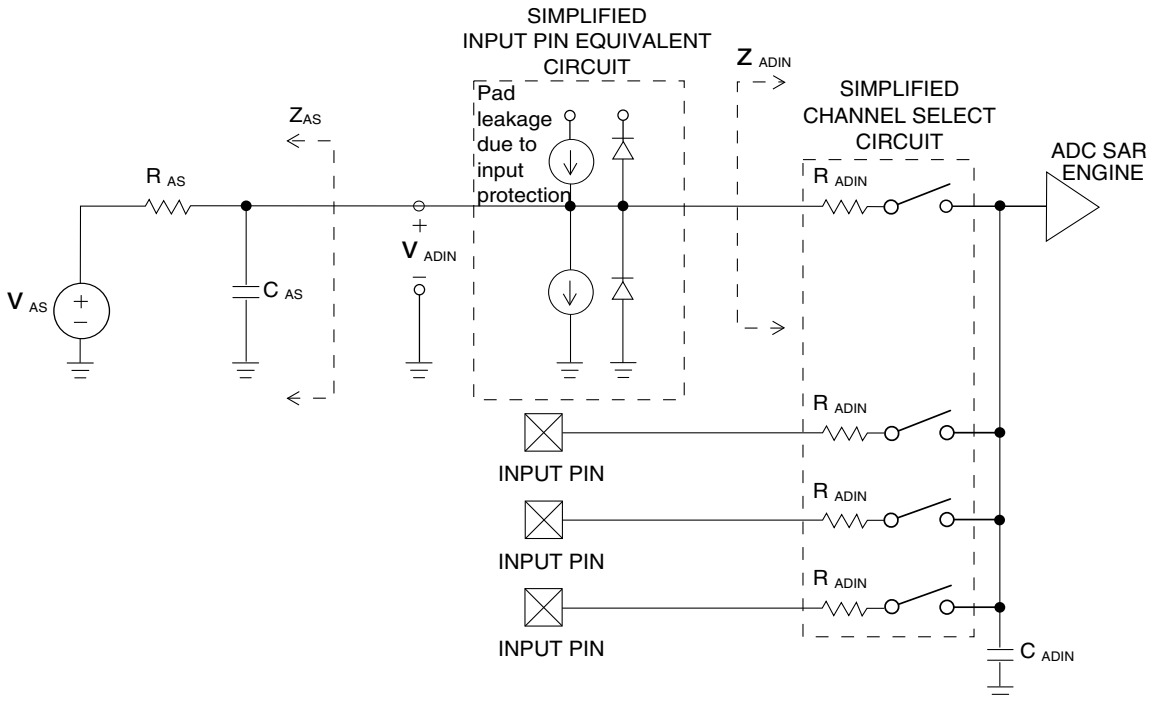

Figure 16. ADC input impedance equivalency diagram

Table 14. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
Supply current ADLPC = 1 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	133	—	µA
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz

Table continues on the next page...

Table 14. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode	T	E_{TUE}	—	±3.0	—	LSB[3]
	10-bit mode	C		—	±1.0	±2.0	
	8-bit mode	T		—	±0.8	—	
Differential Non-Liniarity	12-bit mode	T	DNL	—	±1.2	—	LSB[3]
	10-bit mode[4]	C		—	±0.3	±1.0	
	8-bit mode[4]	T		—	±0.15	—	
Integral Non-Linearity	12-bit mode	T	INL	—	±1.2	—	LSB[3]
	10-bit mode	C		—	±0.3	±1.0	
	8-bit mode	T		—	±0.15	—	
Zero-scale error[5]	12-bit mode	T	E_{ZS}	—	±1.2	—	LSB[3]
	10-bit mode	C		—	±0.15	±1.0	
	8-bit mode	T		—	±0.3	—	
Full-scale error[6]	12-bit mode	T	E_{FS}	—	±1.8	—	LSB[3]
	10-bit mode	C		—	±0.7	±1.0	
	8-bit mode	T		—	±0.5	—	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=2.5 MHz under FBE mode and alternate clock source (ALTCLK) is selected as ADC clock.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{In} = leakage current (refer to DC characteristics)

Table 17. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

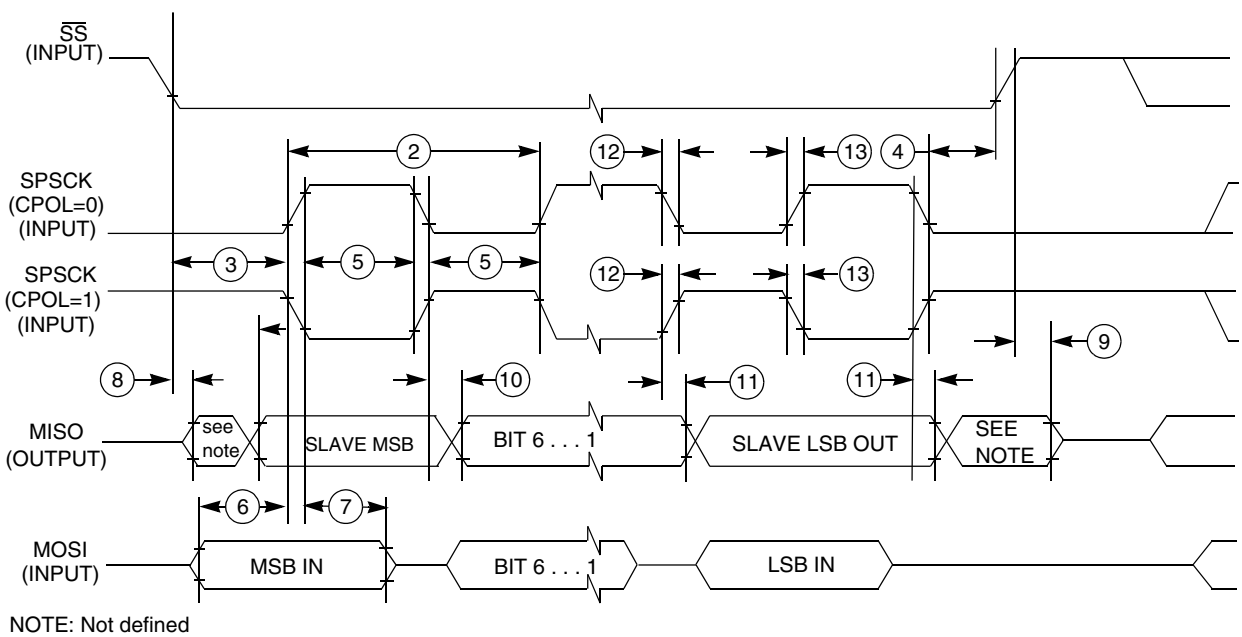

Figure 19. SPI slave mode timing (CPHA = 0)

NOTE

- PTB5, PTC1, and PTC5 pins support high-current drive output, refer to the PORT_HDRVE register in Port Control chapter for details.
- VDD and VREFH are internally connected. Only one pin (VDD or VREFH) is available on chip.
- VSS and VREFL are internally connected. Only one pin (VSS or VREFL) is available on chip.
- PTA2 and PTA3 are true open-drain pins when operated as output

24 QFN	20 SOIC	16 TSSOP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	—	—	PTC5	DISABLED	PTC5	KBI1_P1	FTM2_CH3	BUSOUT				
2	—	—	PTC4	DISABLED	PTC4	KBI1_P0	FTM2_CH2		PWT_IN0			
3	3	3	VDD	VDD							VDD	
3	3	3	VREFH	VDDA/ VREFH						VDDA	VREFH	
4	4	4	VREFL	VREFL							VREFL	
4	4	4	VSS	VSS/ VSSA						VSSA	VSS	
5	5	5	PTB7	EXTAL	PTB7		I2C0_SCL				EXTAL	
6	6	6	PTB6	XTAL	PTB6		I2C0_SDA				XTAL	
7	7	7	PTB5	ACMP1_OUT	PTB5	KBI1_P7	FTM2_CH5	SPI0_PCS	ACMP1_OUT			
8	8	8	PTB4	NMI_b	PTB4	KBI1_P6	FTM2_CH4	SPI0_MISO	ACMP1_IN2	NMI_b		
9	9	—	PTC3	ADC0_SE11	PTC3	KBI1_P5	FTM2_CH3				ADC0_SE11	
10	10	—	PTC2	ADC0_SE10	PTC2	KBI1_P4	FTM2_CH2				ADC0_SE10	
11	11	—	PTC1	ADC0_SE9	PTC1	KBI1_P3	FTM2_CH1				ADC0_SE9	
12	12	—	PTC0	ADC0_SE8	PTC0	KBI1_P2	FTM2_CH0				ADC0_SE8	
13	13	9	PTB3	ADC0_SE7	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1			ADC0_SE7	
14	14	10	PTB2	ADC0_SE6	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ACMP0_IN0		ADC0_SE6	
15	15	11	PTB1	ADC0_SE5	PTB1	KBI0_P5	UART0_TX	SPI0_MISO	TCLK2		ADC0_SE5	
16	16	12	PTB0	ADC0_SE4	PTB0	KBI0_P4	UART0_RX	SPI0_PCS	PWT_IN1		ADC0_SE4	
17	—	—	PTA7	ADC0_SE3	PTA7		FTM2_FLT2	SPI0_MOSI	ACMP1_IN1		ADC0_SE3	
18	—	—	PTA6	ADC0_SE2	PTA6		FTM2_FLT1	SPI0_SCK	ACMP1_IN0		ADC0_SE2	
19	17	13	PTA3	DISABLED	PTA3	KBI0_P3	UART0_TX	I2C0_SCL				
20	18	14	PTA2	DISABLED	PTA2	KBI0_P2	UART0_RX	I2C0_SDA				
21	19	15	PTA1	ADC0_SE1	PTA1	KBI0_P1	FTM0_CH1		ACMP0_IN1		ADC0_SE1	
22	20	16	PTA0	SWD_CLK	PTA0	KBI0_P0	FTM0_CH0	RTCO	ACMP0_IN2	ADC0_SE0	SWD_CLK	
23	1	1	PTA5	RESET_b	PTA5	IRQ	TCLK1				RESET_b	
24	2	2	PTA4	SWD_DIO	PTA4				ACMP0_OUT		SWD_DIO	

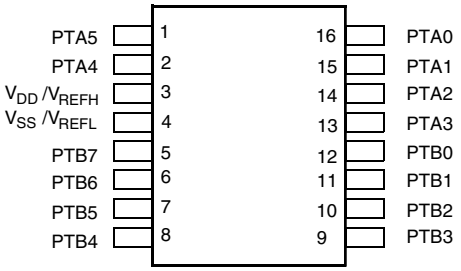

Figure 23. 16-pin TSSOP package

9 Revision history

The following table provides a revision history for this document.

Table 18. Revision history

Rev. No.	Date	Substantial Changes
3	3/2014	Initial public release

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Document Number MKE04P24M48SF0
Revision 3, 3/2014