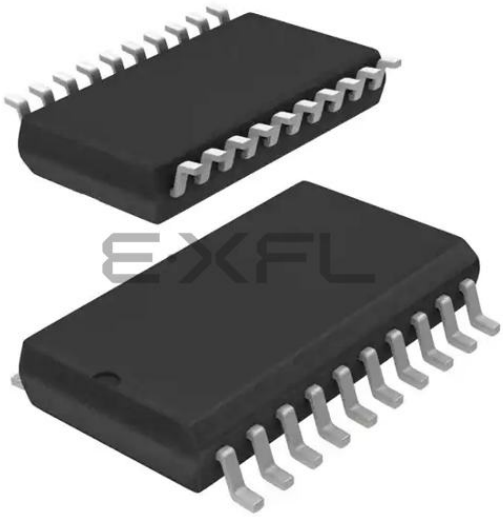


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f563hpf-g-sne2

1. Product Line-up

- MB95560H Series

Parameter \ Part number	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 16 • CMOS I/O : 15 • N-ch open drain: 1			• I/O ports (Max) : 17 • CMOS I/O : 15 • N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
LIN-UART	• A wide range of communication speed can be selected by a dedicated reload timer. • It has a full duplex double buffer. • Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled. • The LIN function can be used as a LIN master or a LIN slave.					
8/10-bit A/D converter	6 channels 8-bit or 10-bit resolution can be selected.					
8/16-bit composite timer	2 channels • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (7 types) and external clocks. • It can output square wave.					
External interrupt	6 channels • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					

3. Differences Among Products And Notes On Product Selection

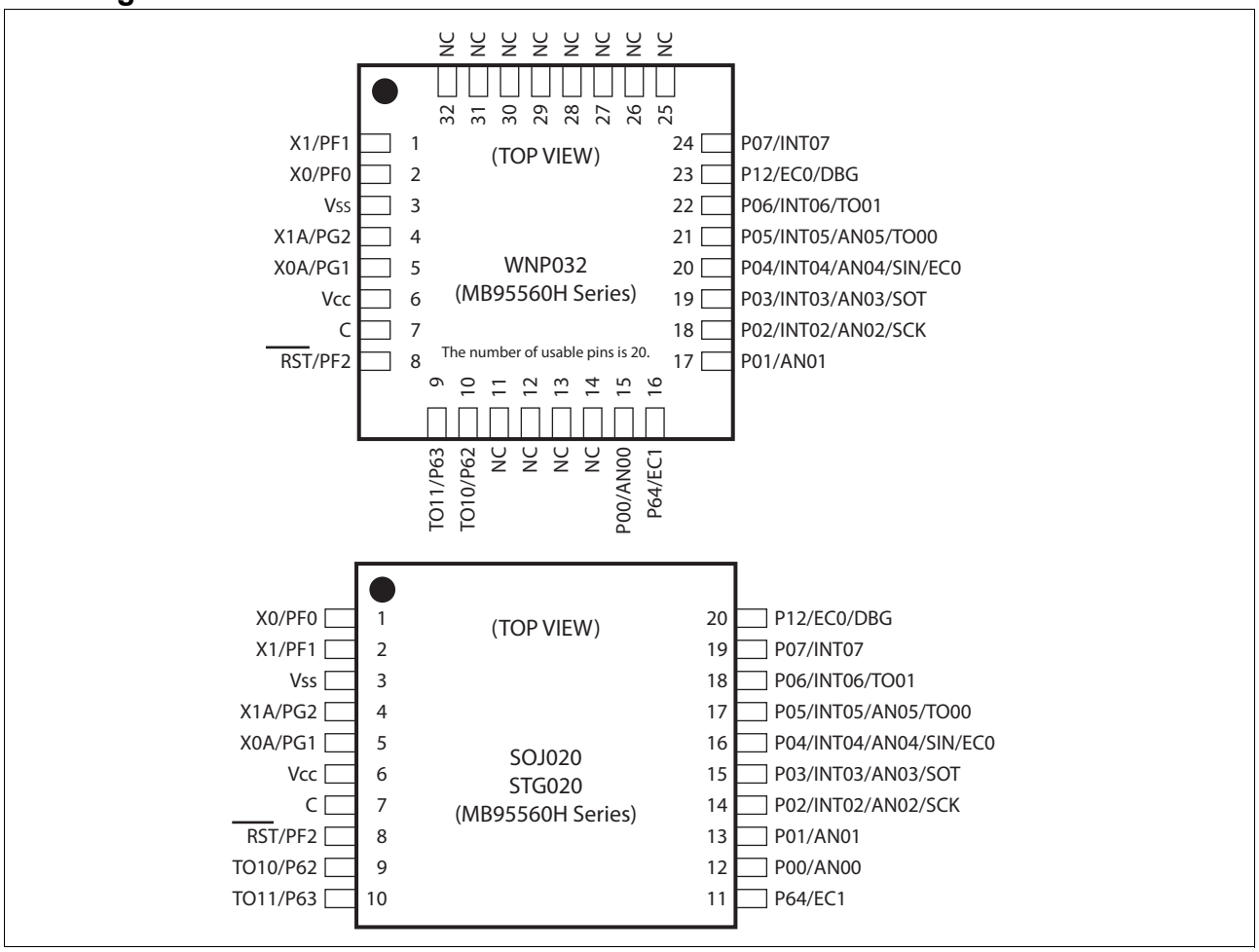
- Current consumption
  When using the on-chip debug function, take account of the current consumption of Flash memory program/erase.
  For details of current consumption, see “Electrical Characteristics”.

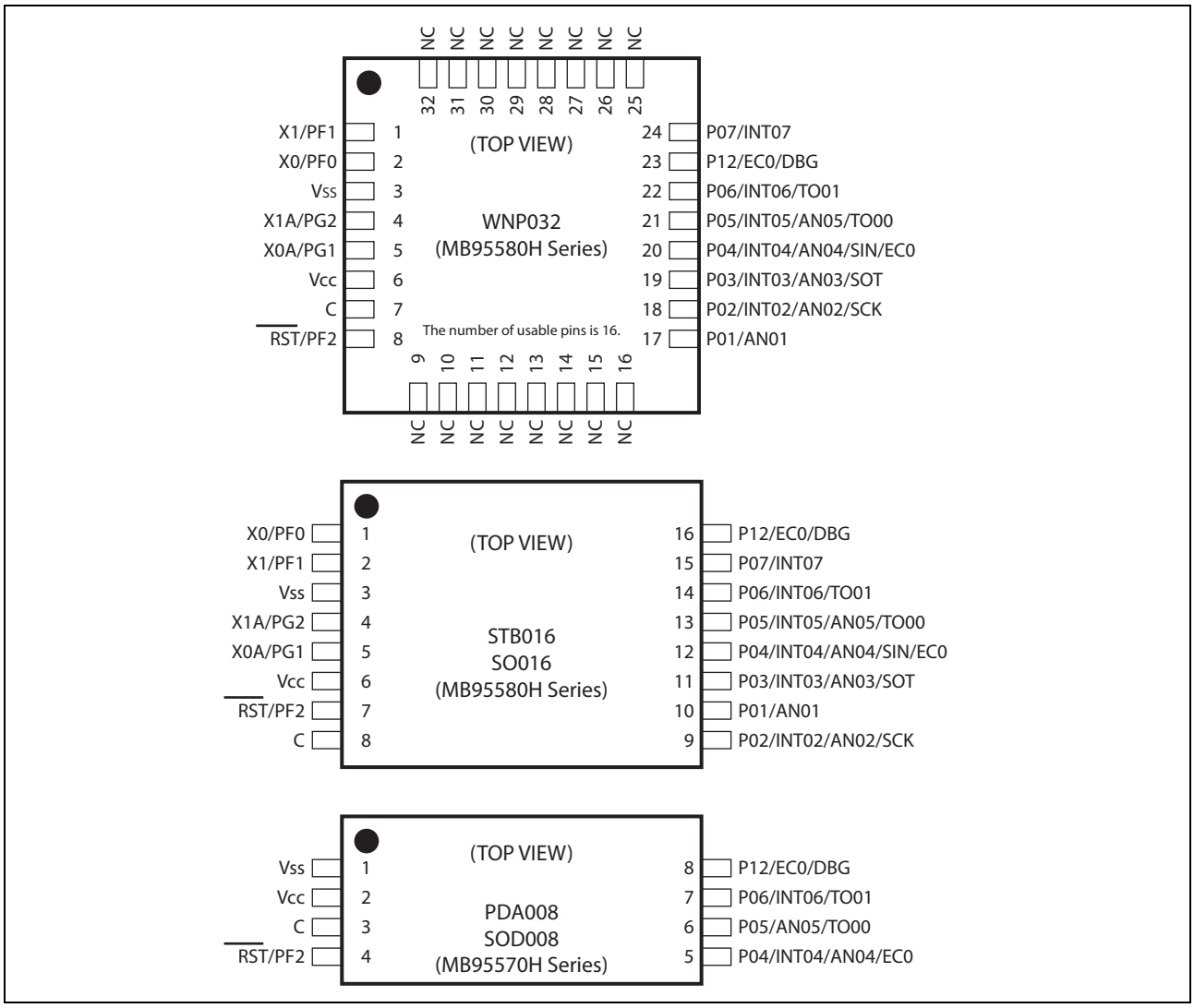
- Package
  For details of information on each package, see “Packages And Corresponding Products” and “Package Dimension”.

- Operating voltage
  The operating voltage varies, depending on whether the on-chip debug function is used or not.
  For details of the operating voltage, see “Electrical Characteristics”.

- On-chip debug function
  The on-chip debug function requires that V_{CC}, V_{SS} and one serial wire be connected to an evaluation tool. For details of the connection method, refer to “CHAPTER 21 EXAMPLE OF SERIAL PROGRAMMING CONNECTION” in “New 8FX MB95560H/570H/580H Hardware Manual”.

4. Pin Assignment



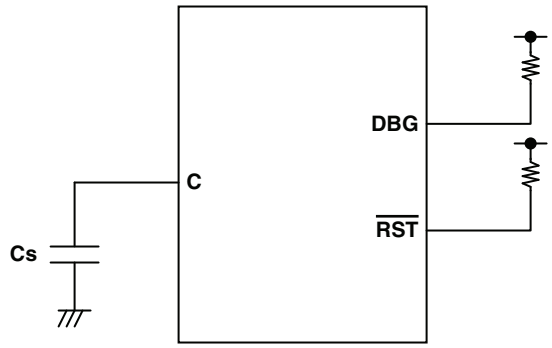

NC NC NC NC NC NC NC NC
32 31 30 29 28 27 26 25
X1/PF1 1
X0/PF0 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
C 7
RST/PF2 8
(TOP VIEW)
WNP032
(MB95580H Series)
The number of usable pins is 16.
24 P07/INT07
23 P12/EC0/DBG
22 P06/INT06/TO01
21 P05/INT05/AN05/TO00
20 P04/INT04/AN04/SIN/EC0
19 P03/INT03/AN03/SOT
18 P02/INT02/AN02/SCK
17 P01/AN01
9 10 11 12 13 14 15 16
NC NC NC NC NC NC NC NC
X0/PF0 1
X1/PF1 2
Vss 3
X1A/PG2 4
X0A/PG1 5
Vcc 6
RST/PF2 7
C 8
(TOP VIEW)
STB016
SO016
(MB95580H Series)
16 P12/EC0/DBG
15 P07/INT07
14 P06/INT06/TO01
13 P05/INT05/AN05/TO00
12 P04/INT04/AN04/SIN/EC0
11 P03/INT03/AN03/SOT
10 P01/AN01
9 P02/INT02/AN02/SCK
Vss 1
Vcc 2
C 3
RST/PF2 4
(TOP VIEW)
PDA008
SOD008
(MB95570H Series)
8 P12/EC0/DBG
7 P06/INT06/TO01
6 P05/AN05/TO00
5 P04/INT04/AN04/EC0

7. Pin Functions (MB95570H Series, 8 pins)

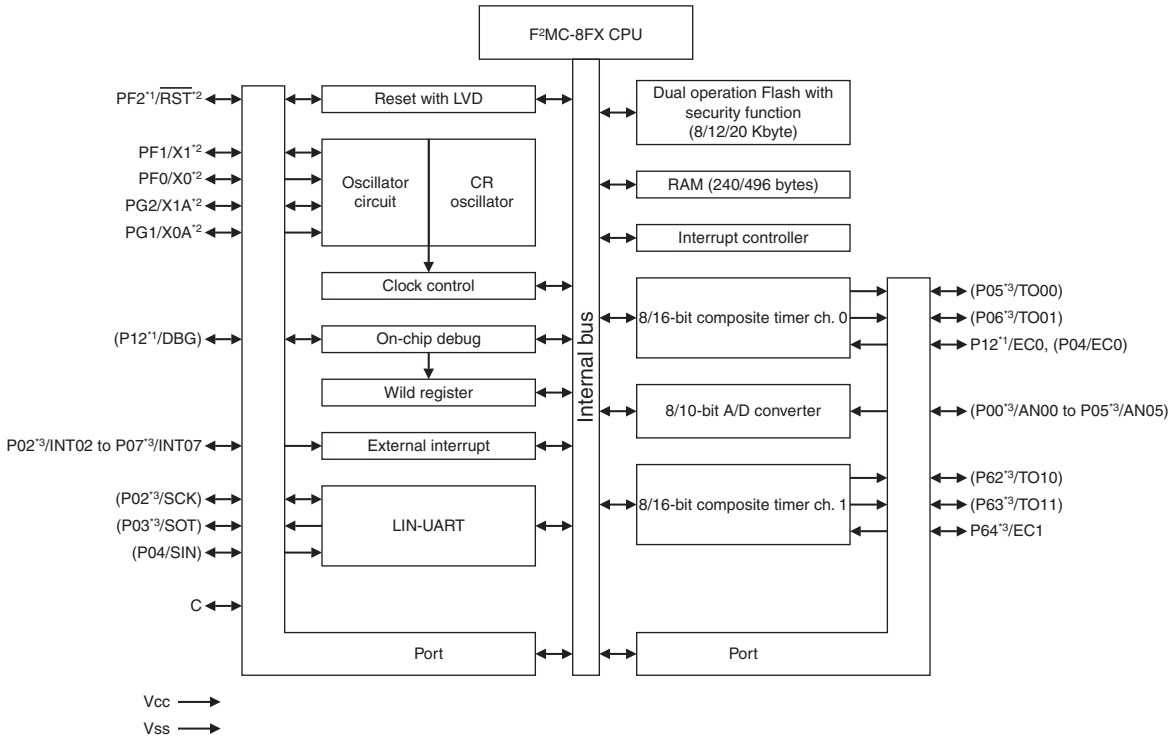
Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Decoupling capacitor connection pin
4	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F572H/F573H/F574H
5	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
6	P05	D	General-purpose I/O port High-current pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
7	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
8	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

*: For the I/O circuit types, see “I/O Circuit Type”.

- DBG/$\overline{\text{RST}}$/C pins connection diagram



14. Block Diagram (MB95560H Series)



*1: PF2 and P12 are N-ch open drain pins.
*2: Software option
*3: P00 to P03, P05 to P07 and P62 to P64 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

Address	Register abbreviation	Register name	R/W	Initial value
0F83H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B
0F89H to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register	R/W	00000000B
0F97H	T11CR0	8/16-bit composite timer 11 status control register 0	R/W	00000000B
0F98H	T10CR0	8/16-bit composite timer 10 status control register 0	R/W	00000000B
0F99H	T11DR	8/16-bit composite timer 11 data register	R/W	00000000B
0F9AH	T10DR	8/16-bit composite timer 10 data register	R/W	00000000B
0F9BH	TMCR1	8/16-bit composite timer 10/11 timer mode control register	R/W	00000000B
0F9CH to 0FBBH	—	(Disabled)	—	—
0FBCH	BGR1	LIN-UART baud rate generator register 1	R/W	00000000B
0FBDH	BGR0	LIN-UART baud rate generator register 0	R/W	00000000B
0FBEH to 0FC2H	—	(Disabled)	—	—
0FC3H	AIDRL	A/D input disable register (lower)	R/W	00000000B
0FC4H to 0FE3H	—	(Disabled)	—	—
0FE4H	CRTH	Main CR clock trimming register (upper)	R/W	000XXXXXB
0FE5H	CRTL	Main CR clock trimming register (lower)	R/W	000XXXXXB
0FE6H	—	(Disabled)	—	—
0FE7H	CRTDA	Main CR clock temperature dependent adjustment register	R/W	000XXXXXB
0FE8H	SYSC	System configuration register	R/W	11000011B
0FE9H	CMCR	Clock monitoring control register	R/W	00000000B
0FEAH	CMDR	Clock monitoring data register	R	00000000B

Address	Register abbreviation	Register name	R/W	Initial value
0050H	SCR	LIN-UART serial control register	R/W	00000000B
0051H	SMR	LIN-UART serial mode register	R/W	00000000B
0052H	SSR	LIN-UART serial status register	R/W	00001000B
0053H	RDR	LIN-UART receive data register	R/W	00000000B
	TDR	LIN-UART transmit data register	R/W	00000000B
0054H	ESCR	LIN-UART extended status control register	R/W	00000100B
0055H	ECCR	LIN-UART extended communication control register	R/W	000000XXB
0056H to 006BH	—	(Disabled)	—	—
006CH	ADC1	8/10-bit A/D converter control register 1	R/W	00000000B
006DH	ADC2	8/10-bit A/D converter control register 2	R/W	00000000B
006EH	ADDH	8/10-bit A/D converter data register (upper)	R/W	00000000B
006FH	ADDL	8/10-bit A/D converter data register (lower)	R/W	00000000B
0070H	—	(Disabled)	—	—
0071H	FSR2	Flash memory status register 2	R/W	00000000B
0072H	FSR	Flash memory status register	R/W	000X0000B
0073H	SWRE0	Flash memory sector write control register 0	R/W	00000000B
0074H	FSR3	Flash memory status register 3	R	000XXXXXB
0075H	FSR4	Flash memory status register 4	R/W	00000000B
0076H	WREN	Wild register address compare enable register	R/W	00000000B
0077H	WROR	Wild register data test setting register	R/W	00000000B
0078H	—	Mirror of register bank pointer (RP) and direct bank pointer (DP)	—	—
0079H	ILR0	Interrupt level setting register 0	R/W	11111111B
007AH	ILR1	Interrupt level setting register 1	R/W	11111111B
007BH	ILR2	Interrupt level setting register 2	R/W	11111111B
007CH	—	(Disabled)	—	—
007DH	ILR4	Interrupt level setting register 4	R/W	11111111B
007EH	ILR5	Interrupt level setting register 5	R/W	11111111B
007FH	—	(Disabled)	—	—
0F80H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch. 0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B

21. Interrupt Source Table (MB95560H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

22. Interrupt Source Table (MB95570H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
—	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
—	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
—	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
—					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
—	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
—	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

23. Interrupt Source Table (MB95580H Series)

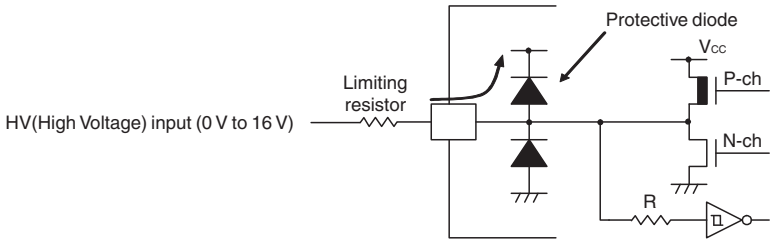
Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0. PF1, PG1, and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

  - Input/Output equivalent circuit



*4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

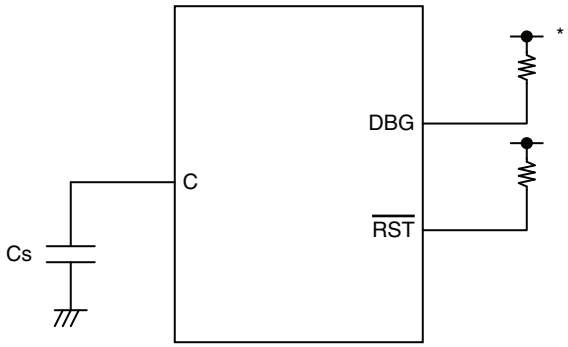
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1, *2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Decoupling capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{RST}$ / C pins connection diagram



*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

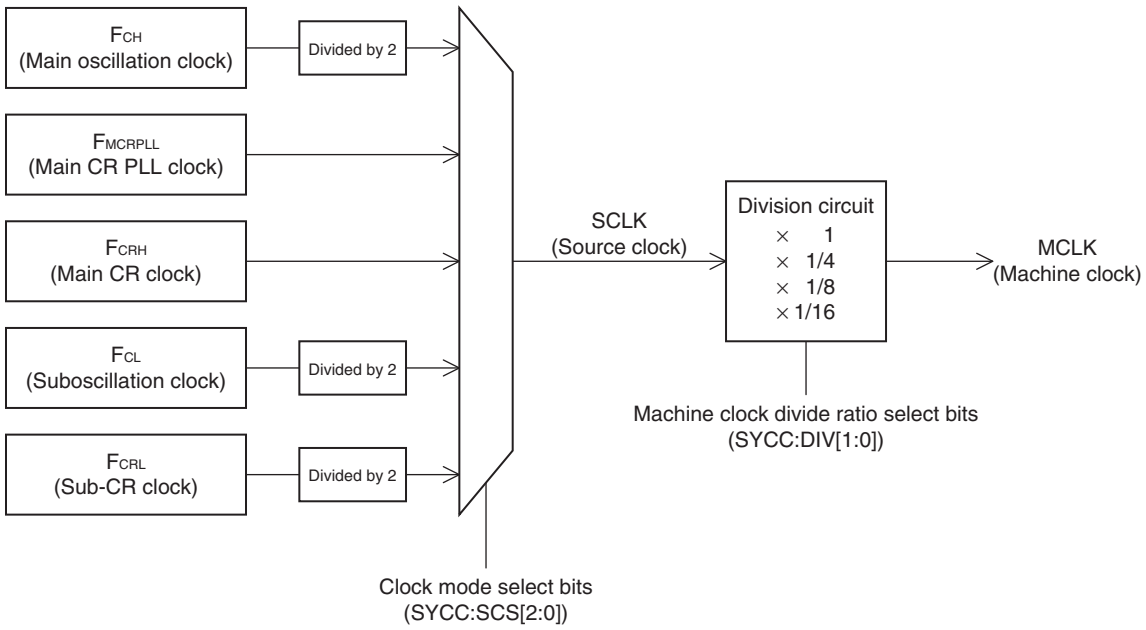
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

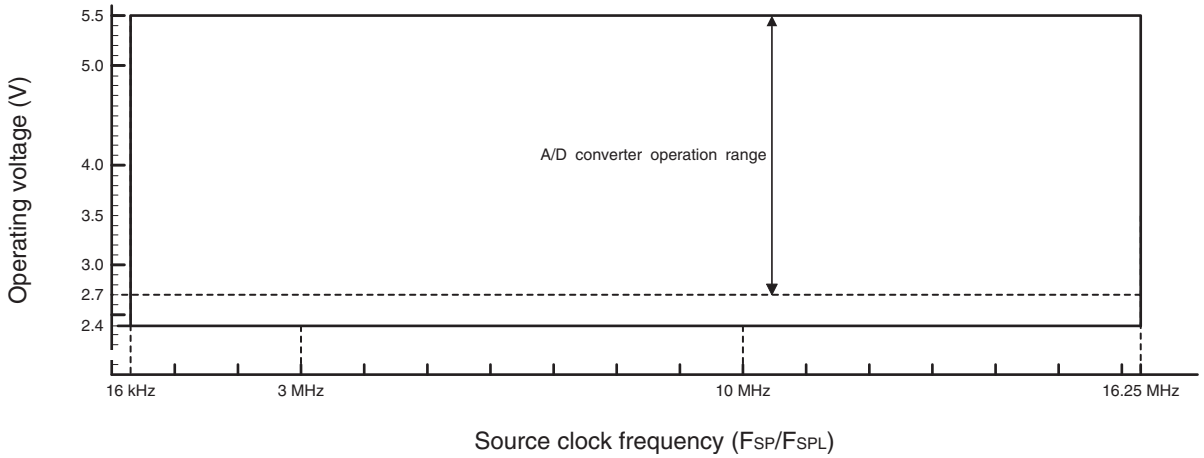
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ*1	Max*2		
Power supply current*5	I_{CC}	V_{CC} (External clock operation)	F_{CH} = 32 MHz F_{MP} = 16 MHz Main clock mode (divided by 2)	—	3.5	4.4	mA	Except during Flash memory programming and erasing
				—	7.4	9.8	mA	During Flash memory programming and erasing
				—	5.1	6.4	mA	At A/D conversion
	I_{CCS}		F_{CH} = 32 MHz F_{MP} = 16 MHz Main sleep mode (divided by 2)	—	1.2	1.5	mA	
	I_{CCL}		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subclock mode (divided by 2) T_A = +25 °C	—	65	71	µA	
	I_{CCLS}*6		F_{CL} = 32 kHz F_{MPL} = 16 kHz Subsleep mode (divided by 2) T_A = +25 °C	—	5.4	7	µA	In deep standby mode
	I_{CCT}*6		F_{CL} = 32 kHz Watch mode T_A = +25 °C	—	4.8	6.9	µA	In deep standby mode
	I_{CCMCR}	V_{CC}	F_{CRH} = 4 MHz F_{MP} = 4 MHz Main CR clock mode	—	1.1	1.4	mA	
	I_{CCSCR}		Sub-CR clock mode (divided by 2) T_A = +25 °C	—	58	64	µA	
	I_{CCTS}	V_{CC} (External clock operation)	F_{CH} = 32 MHz Time-base timer mode T_A = +25 °C	—	290	340	µA	In deep standby mode
	I_{CCH}		Main stop mode (single external clock product)/ Substop mode (dual external clock product) T_A = +25 °C	—	4.1	6.5	µA	In deep standby mode

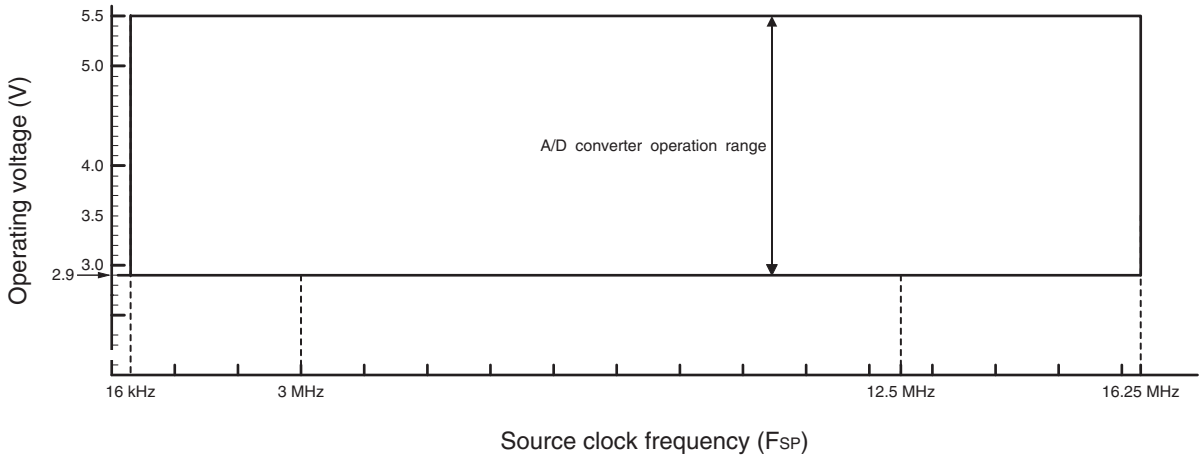
- Schematic diagram of the clock generation block



- Operating voltage - Operating frequency (T_A = –40°C to +85°C)
  Without the on-chip debug function



- Operating voltage - Operating frequency (T_A = –40 °C to +85 °C)
  With the on-chip debug function



24.4.6 LIN-UART Timing (only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K)

Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is disabled*2.
(ESCR register: SCES bit = 0, ECCR register: SCDE bit = 0)

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

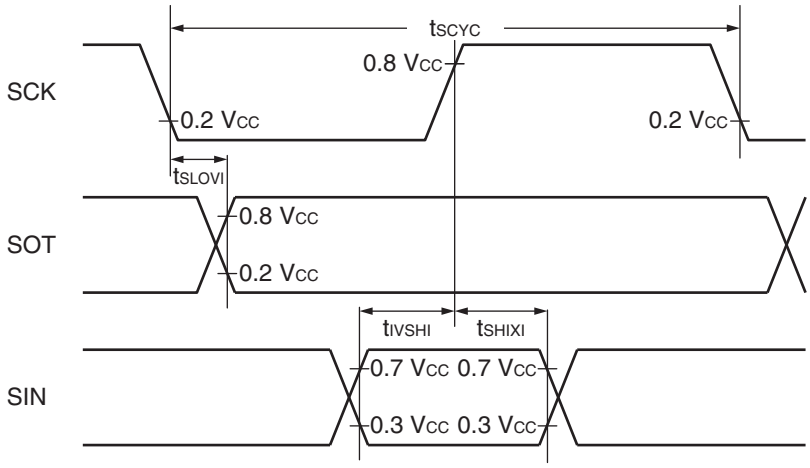
Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
Serial clock “L” pulse width	t_{SLSH}	SCK	External clock operation output pin: C_L = 80 pF + 1 TTL	3 t_{MCLK}*3 – t_R	—	ns
Serial clock “H” pulse width	t_{SHSL}	SCK		t_{MCLK}*3 + 10	—	ns
SCK ↓→ SOT delay time	t_{SLOVE}	SCK, SOT		—	2 t_{MCLK}*3 + 60	ns
Valid SIN → SCK ↑	t_{IVSHE}	SCK, SIN		30	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXE}	SCK, SIN		t_{MCLK}*3 + 30	—	ns
SCK fall time	t_F	SCK		—	10	ns
SCK rise time	t_R	SCK		—	10	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function used to delay the output signal of the serial clock for half the clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.

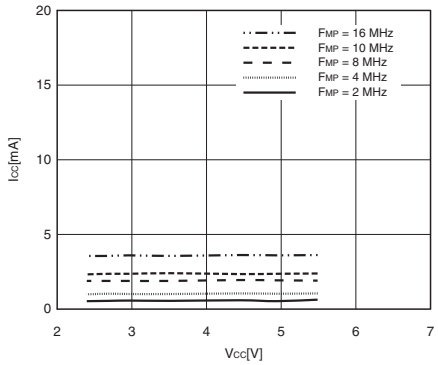
- Internal shift clock mode



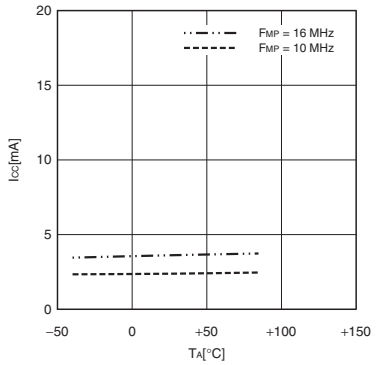
25. Sample Characteristics

- Power supply current temperature characteristics

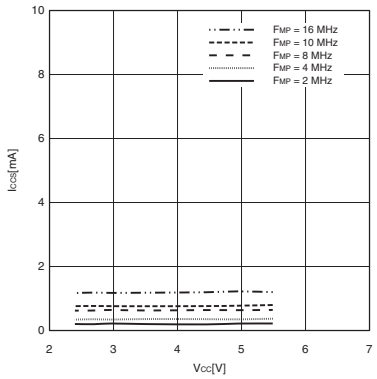
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



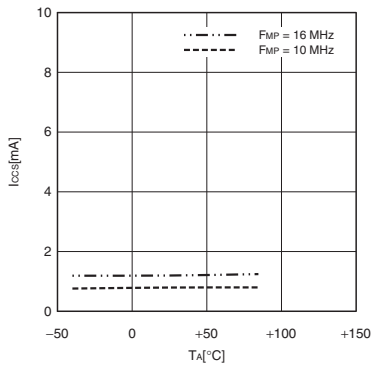
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



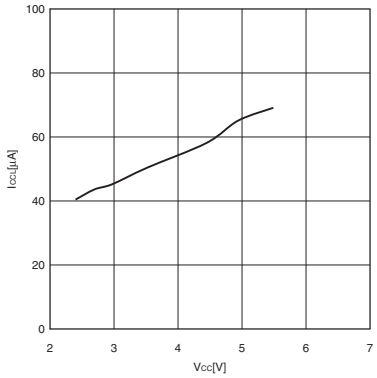
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



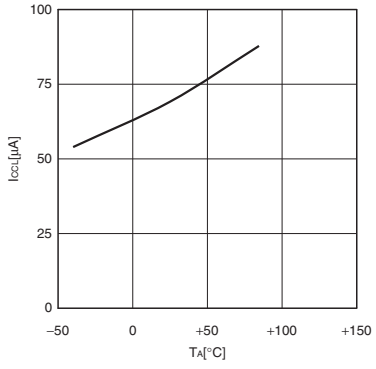
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



I_{CCL} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



Part number	Package	Packing
MB95F582HPF-G-SNE2 MB95F582KPF-G-SNE2 MB95F583HPF-G-SNE2 MB95F583KPF-G-SNE2 MB95F584HPF-G-SNE2 MB95F584KPF-G-SNE2	16-pin plastic SOP (SO016)	Tube
MB95F572HPH-G-SNE2 MB95F572KPH-G-SNE2 MB95F573HPH-G-SNE2 MB95F573KPH-G-SNE2 MB95F574HPH-G-SNE2 MB95F574KPH-G-SNE2	8-pin plastic DIP (PDA008)	Tube
MB95F572HPF-G-SNE2 MB95F572KPF-G-SNE2 MB95F573HPF-G-SNE2 MB95F573KPF-G-SNE2 MB95F574HPF-G-SNE2 MB95F574KPF-G-SNE2	8-pin plastic SOP (SOD008)	Tube

Document History Page

Document Title: MB95560H Series/MB95570H Series/MB95580H Series, New 8FX 8-bit Microcontrollers Document Number: 002-04629				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	AKIH	05/27/2013	Migrated to Cypress and assigned document number 002-04629. No change to document contents or format.
*A	5193921	AKIH	03/29/2016	Updated 24.4.3 External Reset Added MB95F564KPF-G-UNE2, MB95F564KPFT-G-UNE2 in “Ordering Information”. Updated to Cypress template.
*B	5420206	HTER	02/06/2017	Changed package code as the following in 1.Product Line-up (Page4, 6), 2.Packages And Corresponding Products (Page 7), 4.Pin Assignment (Page 9 to 10), 27.Ordering Information (Page 75 to 76) and 28.Package Dimensions (Page 77 to 83). “LCC-32P-M19” to “WNP032” “FPT-20P-M09” to “SOJ020” “FPT-20P-M10” to “STG020” “FPT-16P-M08” to “STB016” “FPT-16P-M23” to “SO016” “DIP-8P-M03” to “PDA008” “FPT-8P-M08” to “SOD008” Added Part number “MB95F564KPFT-G-UNERE2, MB95F562KPFT-G-UNERE2, MB95F563KPFT-G-UNERE2” in 27.Ordering Information (Page 75). Deleted Part number “MB95F564KPF-G-SNE2, MB95F564KPFT-G-SNE2” in 27.Ordering Information (Page 75).
*C	5761469	AESATP12	06/08/2017	Updated logo and copyright.
*D	5895915	HUAL	09/27/2017	Added Part number “MB95F563HPFT-G-UNERE2” and Packing information in 27.Ordering Information (Page 75).
*E	5972828	HUAL	11/21/2017	Updated Package Dimension: Updated Diagram corresponding to “SOP 20”.