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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f564kpft-g-sne2

Contents

<table>
<tr><th>Part number
Parameter</th><th>MB95F582H</th><th>MB95F583H</th><th>MB95F584H</th><th>MB95F582K</th><th>MB95F583K</th><th>MB95F584K</th></tr>
<tr><td>Time-base timer</td><td colspan="6">Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)</td></tr>
<tr><td>Hardware/ software watchdog timer</td><td colspan="6">• Reset generation cycle
Main oscillation clock at 10 MHz: 105 ms (Min)
• The sub-CR clock can be used as the source clock of the hardware watchdog timer.</td></tr>
<tr><td>Wild register</td><td colspan="6">It can be used to replace 3 bytes of data.</td></tr>
<tr><td>LIN-UART</td><td colspan="6">• A wide range of communication speed can be selected by a dedicated reload timer.
• It has a full duplex double buffer.
• Both clock synchronous serial data transfer and clock asynchronous serial data transfer are enabled.
• The LIN function can be used as a LIN master or a LIN slave.</td></tr>
<tr><td rowspan="2">8/10-bit A/D converter</td><td colspan="6">5 channels</td></tr>
<tr><td colspan="6">8-bit or 10-bit resolution can be selected.</td></tr>
<tr><td rowspan="2">8/16-bit composite timer</td><td colspan="6">1 channel</td></tr>
<tr><td colspan="6">• The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel".
• It has the following functions: interval timer function, PWC function, PWM function and input capture function.
• Count clock: it can be selected from internal clocks (7 types) and external clocks.
• It can output square wave.</td></tr>
<tr><td rowspan="2">External interrupt</td><td colspan="6">6 channels</td></tr>
<tr><td colspan="6">• Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.)
• It can be used to wake up the device from the standby mode.</td></tr>
<tr><td>On-chip debug</td><td colspan="6">• 1-wire serial control
• It supports serial writing (asynchronous mode).</td></tr>
<tr><td>Watch prescaler</td><td colspan="6">Eight different time intervals can be selected.</td></tr>
<tr><td>Flash memory</td><td colspan="6">• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands.
• It has a flag indicating the completion of the operation of Embedded Algorithm.
• Flash security feature for protecting the content of the Flash memory
<table><tr><td>Number of program/erase cycles</td><td>1000</td><td>10000</td><td>100000</td></tr><tr><td>Data retention time</td><td>20 years</td><td>10 years</td><td>5 years</td></tr></table></td></tr>
<tr><td>Standby mode</td><td colspan="6">Sleep mode, stop mode, watch mode, time-base timer mode</td></tr>
<tr><td>Package</td><td colspan="6">WNP032
STB016
SO016</td></tr>
</table>

8. Pin Functions (MB95580H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10			
11			
12			
13			
14			
15			
16			
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

11.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

- **Lead Insertion Type**

  Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

  Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

  If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

- **Surface Mount Type**

  Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

  You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

- **Lead-Free Packaging**

  CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

- **Storage of Semiconductor Devices**

  Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

  (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.

  (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
  When you open Dry Package that recommends humidity 40% to 70% relative humidity.

  (3) When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.

  (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

- **Baking**

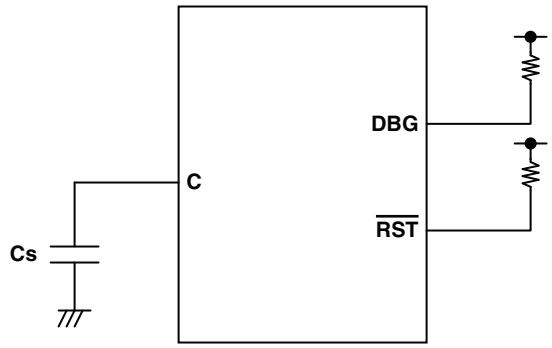
  Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

  Condition: 125°C/24 h

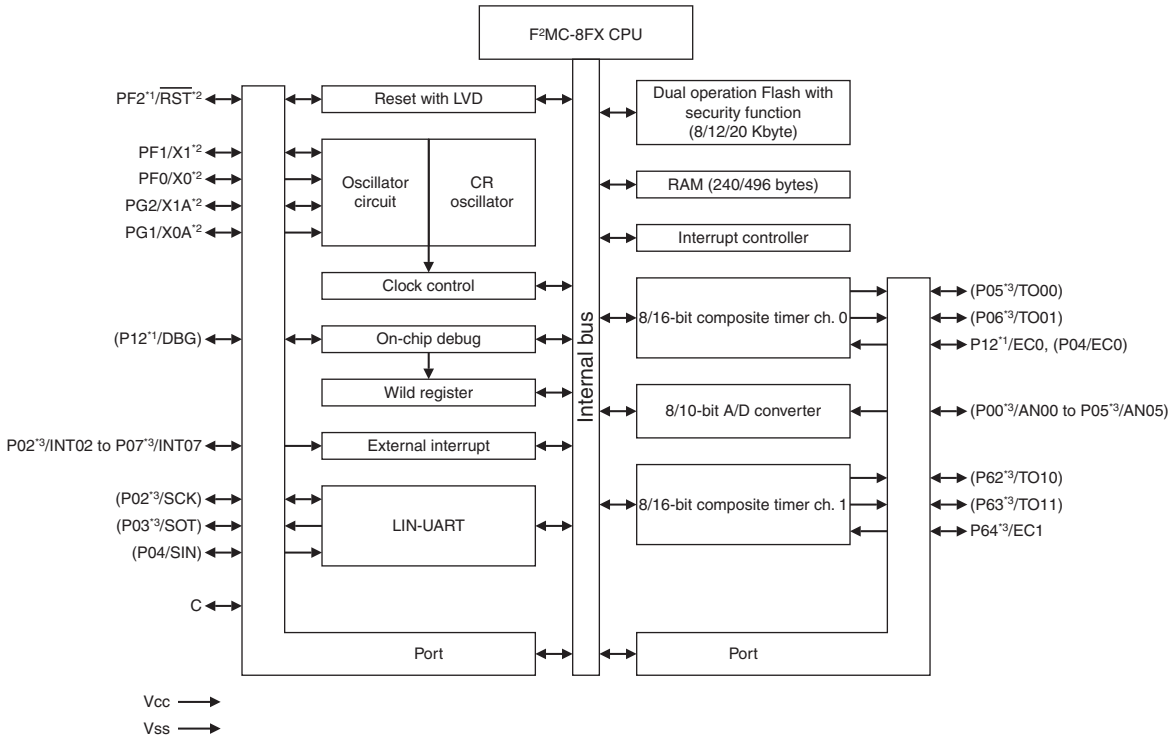
- **Static Electricity**

  Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- DBG/$\overline{\text{RST}}$/C pins connection diagram



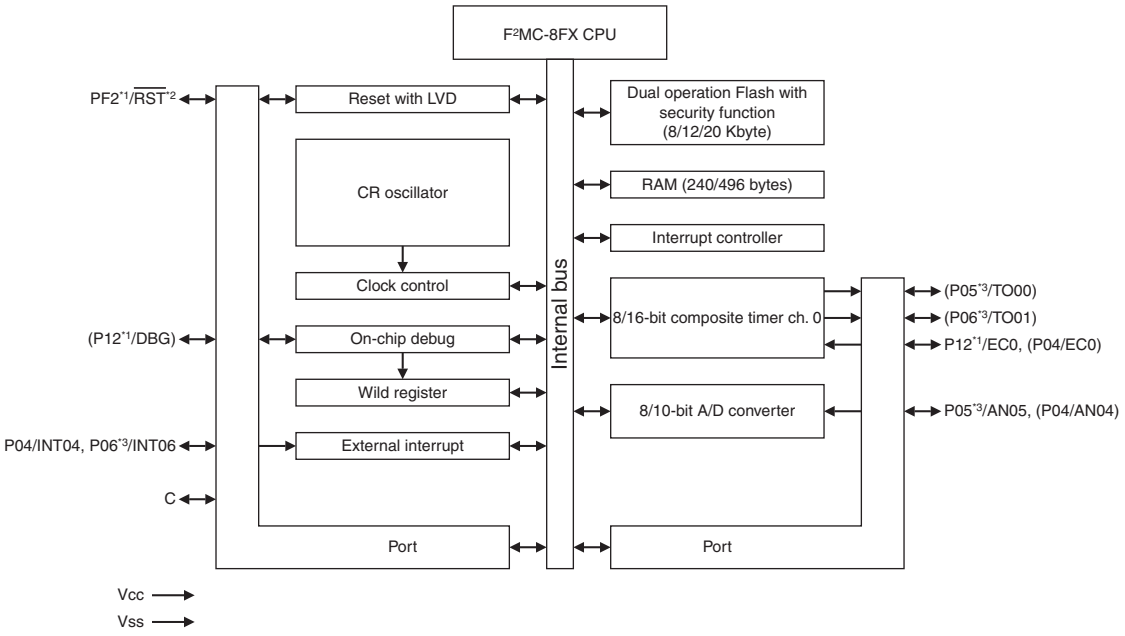
14. Block Diagram (MB95560H Series)



*1: PF2 and P12 are N-ch open drain pins.
*2: Software option
*3: P00 to P03, P05 to P07 and P62 to P64 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

15. Block Diagram (MB95570H Series)



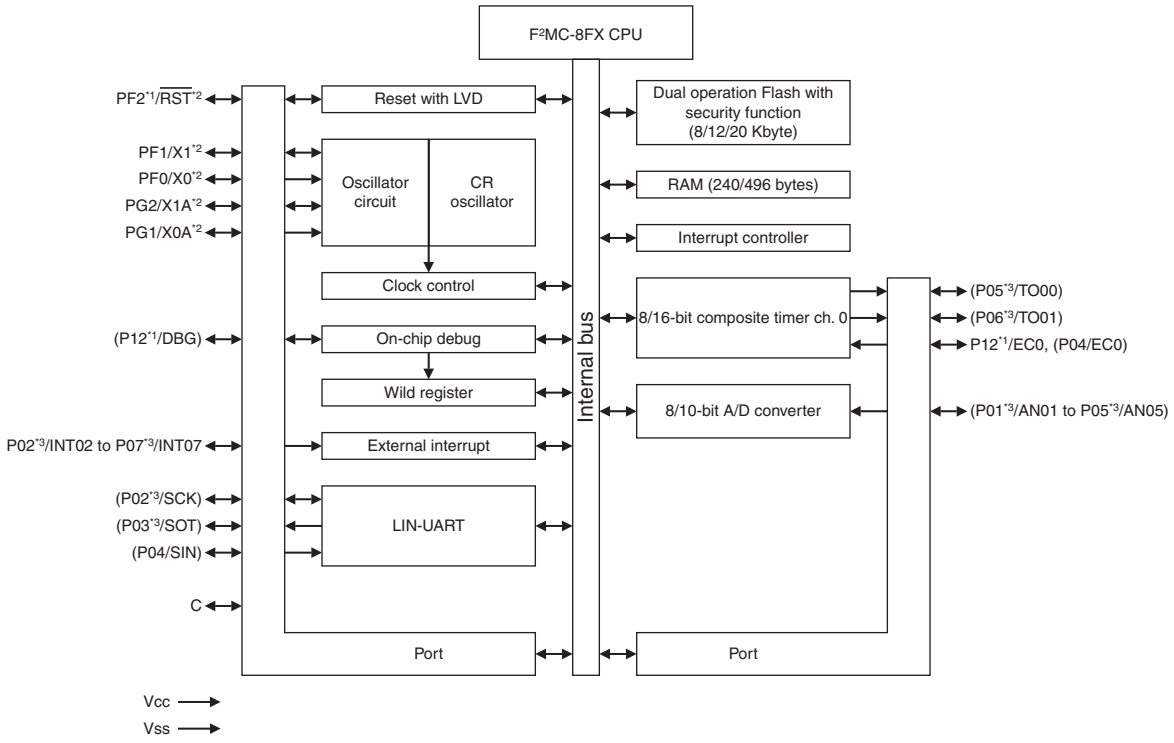
*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P05 and P06 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

16. Block Diagram (MB95580H Series)



*1: PF2 and P12 are N-ch open drain pins.

*2: Software option

*3: P01 to P03 and P05 to P07 are high-current pins.

Note: Pins in parentheses indicate that functions of those pins are shared among different resources.

20. I/O Map (MB95580H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	000X0000B
0007H	SYCC	System clock control register	R/W	XXX11011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R/W	000XXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00XX0000B
000DH	SYCC2	System clock control register 2	R/W	XXXX0011B
000EH	STBC2	Standby control register 2	R/W	00000000B
000FH to 0027H	—	(Disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH	PDRG	Port G data register	R/W	00000000B
002BH	DDRG	Port G direction register	R/W	00000000B
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0034H	—	(Disabled)	—	—
0035H	PULG	Port G pull-up register	R/W	00000000B
0036H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000B
0038H to 0048H	—	(Disabled)	—	—
0049H	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	00000000B
004AH	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000B
004CH, 004DH	—	(Disabled)	—	—
004EH	LVDR	LVDR reset voltage selection ID register	R/W	00000000B
004FH	—	(Disabled)	—	—

24.3 DC Characteristics

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	P04	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHS}	P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P04	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	Hysteresis input
	V_{ILS}	P00*3 to P03*4, P05 to P07*4, P12, P62 to P64*3, PF0*4, PF1*4, PG1*4, PG2*4	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P12, PF2	—	V_{SS} – 0.3	—	V_{SS} + 5.5	V	
"H" level output voltage	V_{OH1}	P04, PF0*4, PF1*4, PG1*4, PG2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P00*3 to P03*4, P05 to P07*4, P62 to P64*3	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	P04, P12, PF0 to PF2*4, PG1*4, PG2*4	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P00*3 to P03*4, P05 to P07*4, P62 to P64*3	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	P00*3 to P07*4, P62 to P64*3, PG1*4, PG2*4	V_I = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

24.4.2 Source Clock / Machine Clock

(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock cycle time*1	t_{SCLK}	—	61.5	—	2000	ns	When the main external clock is used Min: F_{CH} = 32.5 MHz, divided by 2 Max: F_{CH} = 1 MHz, divided by 2
			62.5	—	1000	ns	When the main CR clock is used Min: F_{CRH} = 4 MHz, multiplied by 4 Max: F_{CRH} = 4 MHz, divided by 4
			—	61	—	µs	When the suboscillation clock is used F_{CL} = 32.768 kHz, divided by 2
			—	20	—	µs	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Source clock frequency	F_{SP}	—	0.5	—	16.25	MHz	When the main oscillation clock is used
			—	4	—	MHz	When the main CR clock is used
	F_{SPL}		—	16.384	—	kHz	When the suboscillation clock is used
			—	50	—	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz, divided by 2
Machine clock cycle time*2 (minimum instruction execution time)	t_{MCLK}	—	61.5	—	32000	ns	When the main oscillation clock is used Min: F_{SP} = 16.25 MHz, no division Max: F_{SP} = 0.5 MHz, divided by 16
			250	—	1000	ns	When the main CR clock is used Min: F_{SP} = 4 MHz, no division Max: F_{SP} = 4 MHz, divided by 4
			61	—	976.5	µs	When the suboscillation clock is used Min: F_{SPL} = 16.384 kHz, no division Max: F_{SPL} = 16.384 kHz, divided by 16
			20	—	320	µs	When the sub-CR clock is used Min: F_{SPL} = 50 kHz, no division Max: F_{SPL} = 50 kHz, divided by 16
Machine clock frequency	F_{MP}	—	0.031	—	16.25	MHz	When the main oscillation clock is used
			0.25	—	16	MHz	When the main CR clock is used
	F_{MPL}		1.024	—	16.384	kHz	When the suboscillation clock is used
			3.125	—	50	kHz	When the sub-CR clock is used F_{CRL} = 100 kHz

*1: This is the clock before it is divided according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). This source clock is divided to become a machine clock according to the division ratio set by the machine clock division ratio select bits (SYCC:DIV[1:0]). In addition, a source clock can be selected from the following.
- Main clock divided by 2
- Main CR clock
- PLL multiplication of main CR clock (Select a multiplication rate from 2, 2.5, 3 and 4.)
- Subclock divided by 2
- Sub-CR clock divided by 2

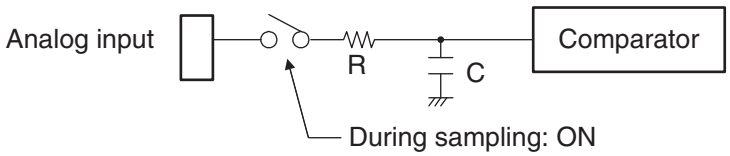
*2: This is the operating clock of the microcontroller. A machine clock can be selected from the following.
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

24.5.2 Notes on Using A/D Converter

- External impedance of analog input and its sampling time

  The A/D converter of the MB95560H/570H/580H has a sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the capacitor of the internal sample and hold circuit is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, considering the relationship between the external impedance and minimum sampling time, either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. In addition, if sufficient sampling time cannot be secured, connect a capacitor of about 0.1 µF to the analog input pin.

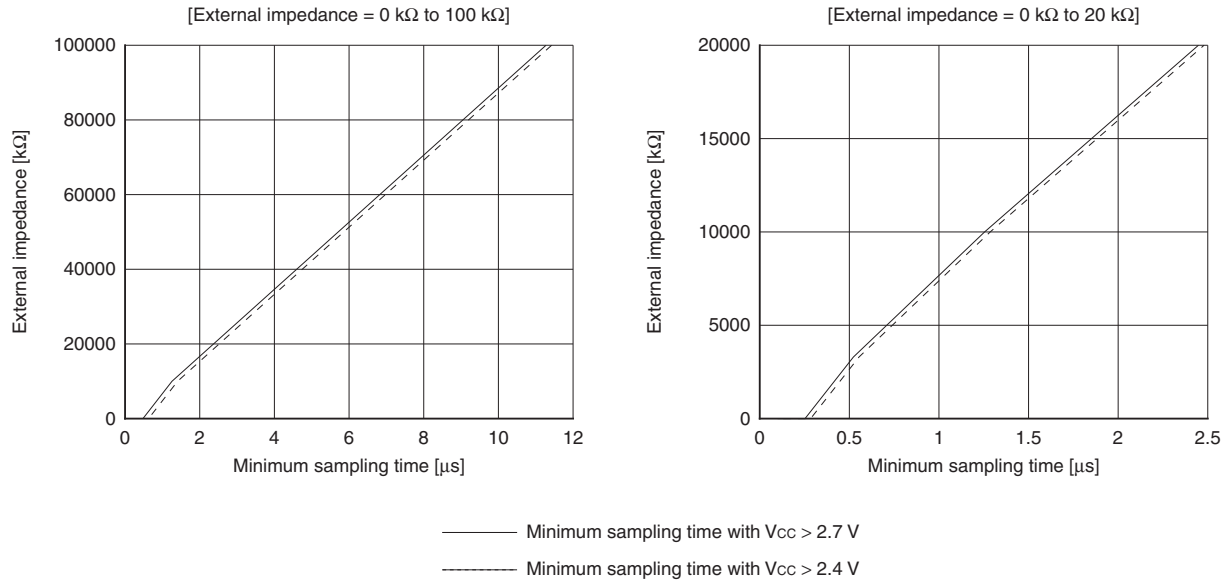
- Analog input equivalent circuit



V_{CC}	R	C
4.5 V ≤ V_{CC} ≤ 5.5 V	1.45 kΩ (Max)	14.89 pF (Max)
2.7 V ≤ V_{CC} < 4.5 V	2.7 kΩ (Max)	14.89 pF (Max)

Note: The values are reference values.

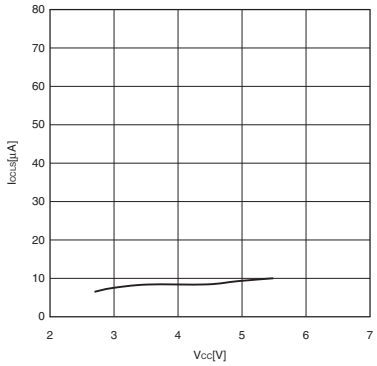
- Relationship between external impedance and minimum sampling time



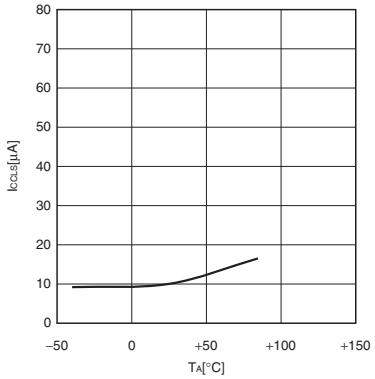
- A/D conversion error

  As |V_{CC} – V_{SS}| decreases, the A/D conversion error increases proportionately.

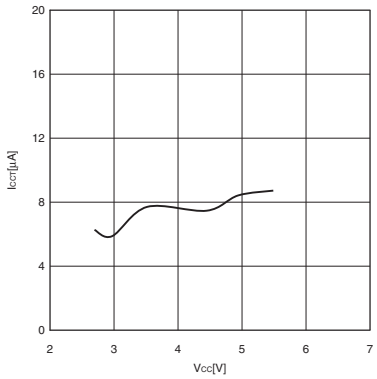
I_{CCLS} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



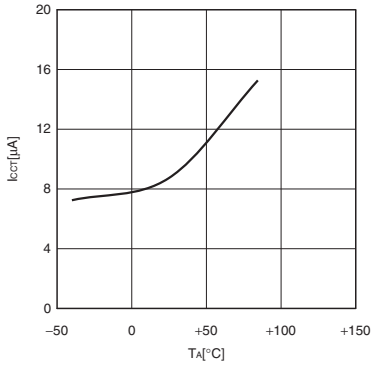
I_{CCLS} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subsleep mode with the external clock operating



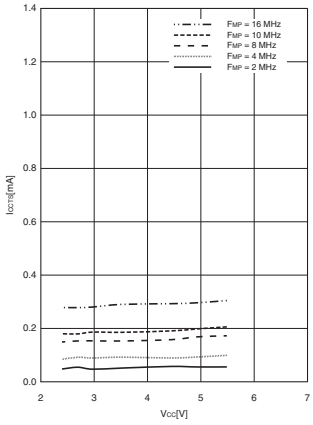
I_{CCT} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



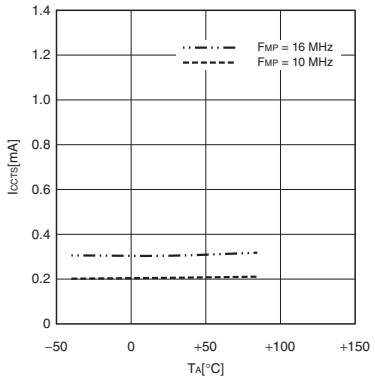
I_{CCT} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Watch mode with the external clock operating



I_{CCTS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

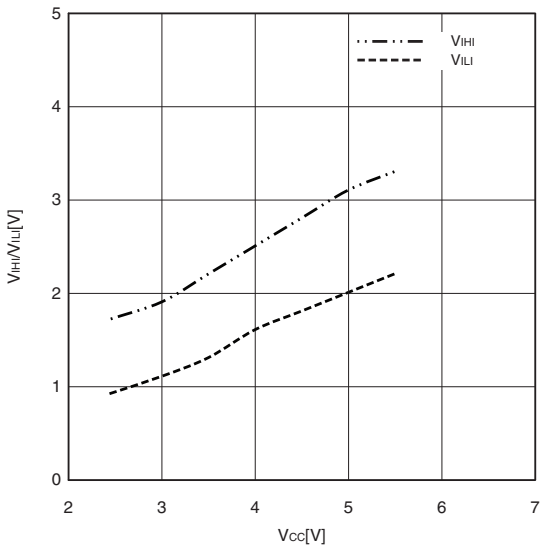


I_{CCTS} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Time-base timer mode with the external clock operating

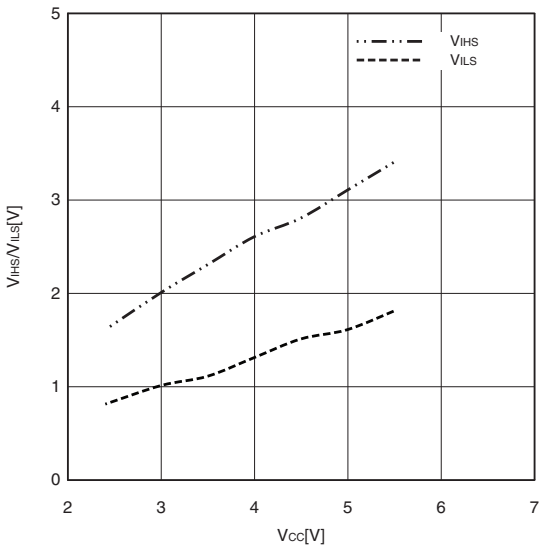


- Input voltage characteristics

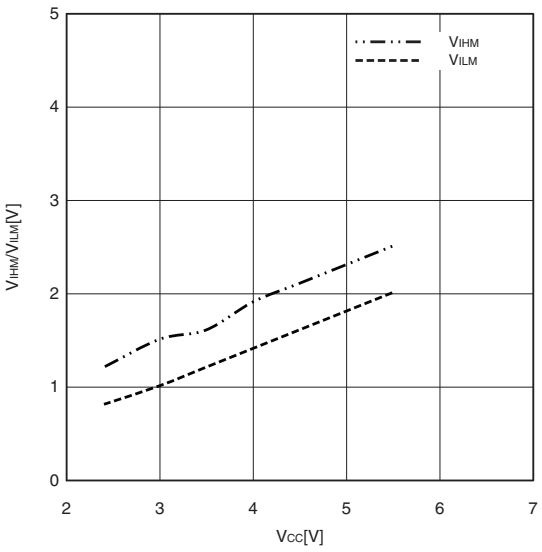
V_{IHI} – V_{CC} and V_{ILI} – V_{CC}
T_A = +25 °C



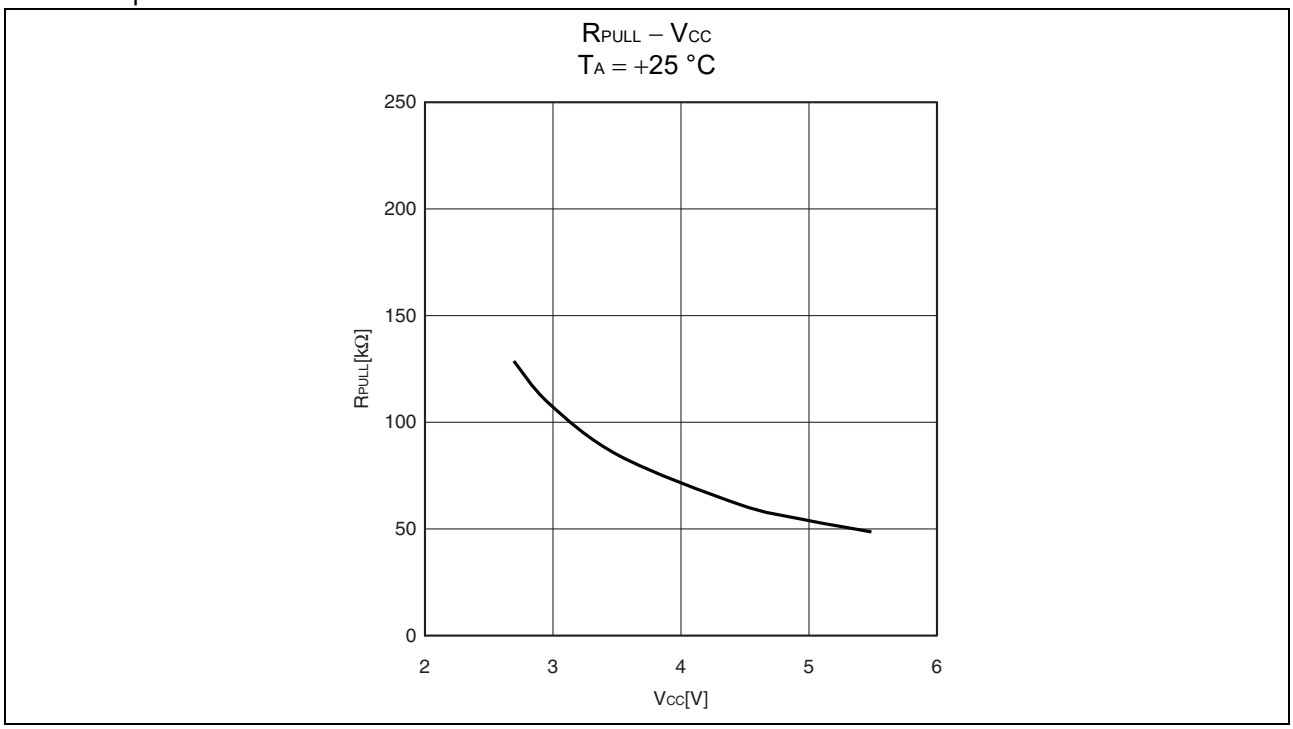
V_{IHS} – V_{CC} and V_{ILS} – V_{CC}
T_A = +25 °C



V_{IHM} – V_{CC} and V_{ILM} – V_{CC}
T_A = +25 °C



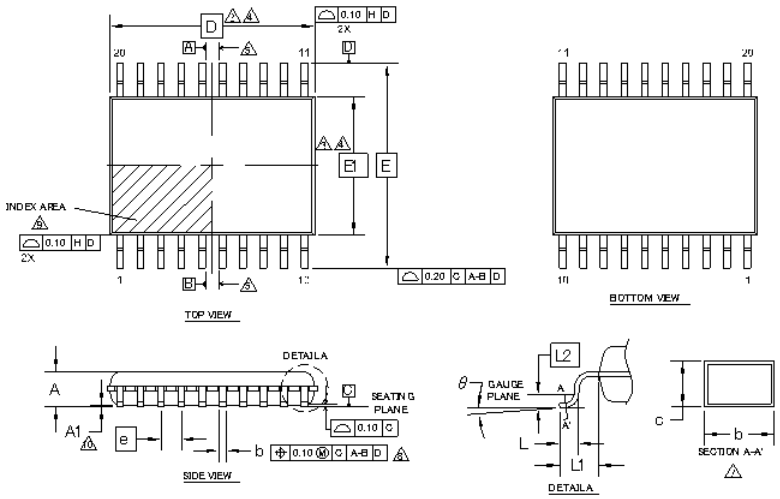
- Pull-up characteristics



27. Ordering Information

Part number	Package	Packing
MB95F562HWQN-G-SNE1 MB95F562KWQN-G-SNE1 MB95F563HWQN-G-SNE1 MB95F563KWQN-G-SNE1 MB95F564HWQN-G-SNE1 MB95F564KWQN-G-SNE1	32-pin plastic QFN (WNP032)	Tray
MB95F562HWQN-G-SNERE1 MB95F562KWQN-G-SNERE1 MB95F563HWQN-G-SNERE1 MB95F563KWQN-G-SNERE1 MB95F564HWQN-G-SNERE1 MB95F564KWQN-G-SNERE1		Reel
MB95F562HPF-G-SNE2 MB95F562KPF-G-SNE2 MB95F563HPF-G-SNE2 MB95F563KPF-G-SNE2 MB95F564HPF-G-SNE2 MB95F564KPF-G-UNE2	20-pin plastic SOP (SOJ020)	Tube
MB95F562HPFT-G-SNE2 MB95F562KPFT-G-SNE2 MB95F563HPFT-G-SNE2 MB95F563KPFT-G-SNE2 MB95F564HPFT-G-SNE2 MB95F564KPFT-G-UNE2	20-pin plastic TSSOP (STG020)	Tube
MB95F562KPFT-G-UNERE2 MB95F563HPFT-G-UNERE2 MB95F563KPFT-G-UNERE2 MB95F564KPFT-G-UNERE2		Reel
MB95F582HWQN-G-SNE1 MB95F582KWQN-G-SNE1 MB95F583HWQN-G-SNE1 MB95F583KWQN-G-SNE1 MB95F584HWQN-G-SNE1 MB95F584KWQN-G-SNE1	32-pin plastic QFN (WNP032)	Tray
MB95F582HWQN-G-SNERE1 MB95F582KWQN-G-SNERE1 MB95F583HWQN-G-SNERE1 MB95F583KWQN-G-SNERE1 MB95F584HWQN-G-SNERE1 MB95F584KWQN-G-SNERE1		Reel
MB95F582HPFT-G-SNE2 MB95F582KPFT-G-SNE2 MB95F583HPFT-G-SNE2 MB95F583KPFT-G-SNE2 MB95F584HPFT-G-SNE2 MB95F584KPFT-G-SNE2	16-pin plastic TSSOP (STB016)	Tube

Package Type	Package Code
TSSOP 20	STG020



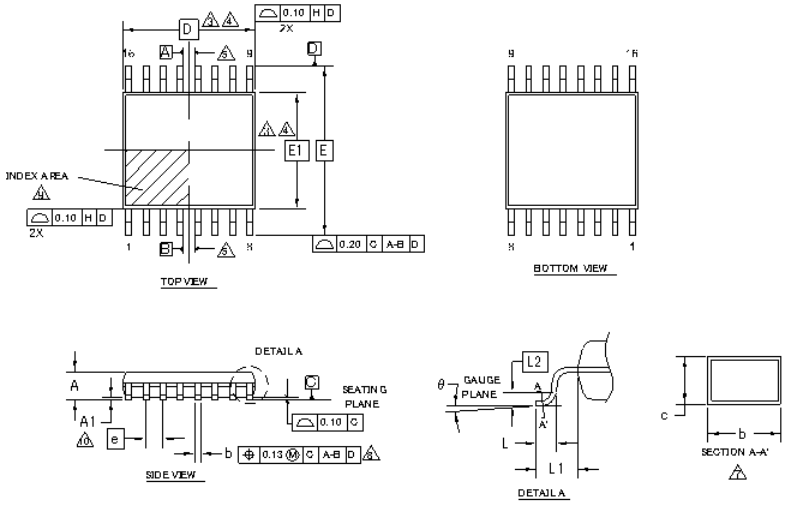
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	6.50 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.20	0.24	0.28
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
3. DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 20 LEAD TSSOP
6.50X6.40X1.20 MM STG020 REV**

002-15916 **

Package Type	Package Code
TSSOP 16	STB016



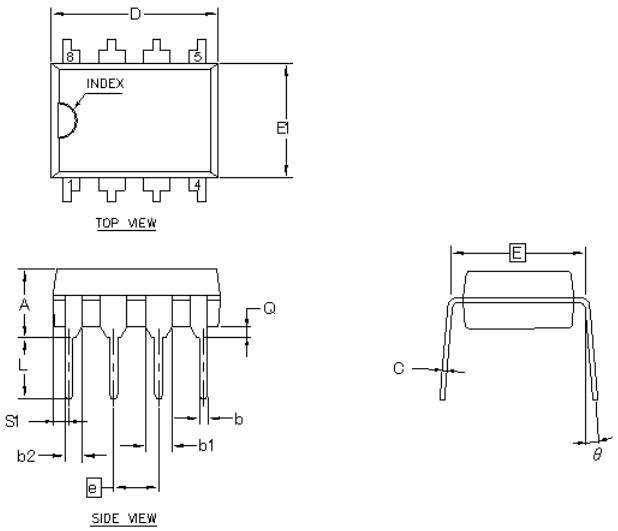
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	4.96 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.16	0.24	0.32
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
3. DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERFLAD FLASH OR PROTRUSION. INTERFLAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 16 LEAD TSSOP
4.96x6.40x1.20 mm STB016 REV**

002-15914 **

Package Type	Package Code
DIP 8	PDA008



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	4.36
L	3.00	——	——
D	9.10	9.40	9.80
E	7.62 TYP		
E1	6.10	6.35	6.60
θ	——	——	15°
c	0.20	0.25	0.30
b	0.38	0.46	0.54
b1	——	1.52	1.82
b2	——	0.99	1.29
e	2.54 TYP		
S1	0.59	0.89	1.24
Q	0.50	——	——

NOTES
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. JEDEC SPECIFICATION NO. REF : N/A

PACKAGE OUTLINE, 8 LEAD PDIP
9.40X6.35X3.86 MM PDA008 REV**

002-16909 **

Page	Section	Details
48	2. Recommended Operating Conditions	Revised note *2. The value is 2.88 V when the low-voltage detection reset is used. → The minimum power supply voltage becomes 2.18 V when a product with the low-voltage detection reset is used.
		Corrected the following statement in note *3. The decoupling capacitor for the V_{CC} pin must have a capacitance larger than C_S. → The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S.
		Revised the remark in "• DBG/$\overline{\text{RST}}$/C pins connection diagram".
49	3. DC Characteristics	Revised the remark of the parameter "Input leak current (Hi-Z output leak current)". When pull-up resistance is disabled → When the internal pull-up resistor is disabled
		Renamed the parameter "Pull-up resistance" to "Internal pull-up resistor".
		Revised the remark of the parameter "Internal pull-up resistor". When pull-up resistance is enabled → When the internal pull-up resistor is enabled
53	4. AC Characteristics (1) Clock Timing	Corrected the pin names of the parameter "Input clock rising time and falling time". X0 → X0, X0A X0, X1 → X0, X1, X0A, X1A

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