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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	LINbus, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	17
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f564kwqn-g-sne1

Contents

Part number / Parameter	MB95F562H	MB95F563H	MB95F564H	MB95F562K	MB95F563K	MB95F564K
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	WNP032 SOJ020 STG020					

- MB95570H Series

Part number / Parameter	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 4 • CMOS I/O : 3 • N-ch open drain: 1			• I/O ports (Max) : 5 • CMOS I/O : 3 • N-ch open drain: 2		
Time-base timer	Interval time: 0.256 ms to 8.3 s (external clock frequency = 4 MHz)					
Hardware/ software watchdog timer	• Reset generation cycle Main oscillation clock at 10 MHz: 105 ms (Min) • The sub-CR clock can be used as the source clock of the hardware watchdog timer.					
Wild register	It can be used to replace 3 bytes of data.					
LIN-UART	No LIN-UART					
8/10-bit A/D converter	2 channels					
	8-bit or 10-bit resolution can be selected.					

Part number / Parameter	MB95F572H	MB95F573H	MB95F574H	MB95F572K	MB95F573K	MB95F574K
8/16-bit composite timer	1 channel • The timer can be configured as an "8-bit timer × 2 channels" or a "16-bit timer × 1 channel". • It has the following functions: interval timer function, PWC function, PWM function and input capture function. • Count clock: it can be selected from internal clocks (7 types) and external clocks. • It can output square wave.					
External interrupt	2 channels • Interrupt by edge detection (The rising edge, falling edge, or both edges can be selected.) • It can be used to wake up the device from the standby mode.					
On-chip debug	• 1-wire serial control • It supports serial writing (asynchronous mode).					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming (Embedded Algorithm), and program/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Flash security feature for protecting the content of the Flash memory Number of program/erase cycles: 1000 / 10000 / 100000 Data retention time: 20 years / 10 years / 5 years					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	PDA008 SOD008					

• MB95580H Series

Part number / Parameter	MB95F582H	MB95F583H	MB95F584H	MB95F582K	MB95F583K	MB95F584K
Type	Flash memory product					
Clock supervisor counter	It supervises the main clock oscillation.					
Flash memory capacity	8 Kbyte	12 Kbyte	20 Kbyte	8 Kbyte	12 Kbyte	20 Kbyte
RAM capacity	240 bytes	496 bytes	496 bytes	240 bytes	496 bytes	496 bytes
Power-on reset	Yes					
Low-voltage detection reset	No			Yes		
Reset input	Dedicated			Selected through software		
CPU functions	• Number of basic instructions : 136 • Instruction bit length : 8 bits • Instruction length : 1 to 3 bytes • Data bit length : 1, 8 and 16 bits • Minimum instruction execution time : 61.5 ns (machine clock frequency = 16.25 MHz) • Interrupt processing time : 0.6 µs (machine clock frequency = 16.25 MHz)					
General-purpose I/O	• I/O ports (Max) : 12 • CMOS I/O : 11 • N-ch open drain: 1			• I/O ports (Max) : 13 • CMOS I/O : 11 • N-ch open drain: 2		

6. Pin Functions (MB95560H Series, 20 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
2	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F562H/F563H/F564H
9	P62	E	General-purpose I/O port High-current pin
	TO10		8/16-bit composite timer ch. 1 output pin
10	P63	E	General-purpose I/O port High-current pin
	TO11		8/16-bit composite timer ch. 1 output pin
11	P64	E	General-purpose I/O port High-current pin
	EC1		8/16-bit composite timer ch. 1 clock input pin
12	P00	D	General-purpose I/O port High-current pin
	AN00		A/D converter analog input pin
13	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
14	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
15	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

7. Pin Functions (MB95570H Series, 8 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	V_{SS}	—	Power supply pin (GND)
2	V_{CC}	—	Power supply pin
3	C	—	Decoupling capacitor connection pin
4	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F572H/F573H/F574H
5	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
6	P05	D	General-purpose I/O port High-current pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
7	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
8	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin

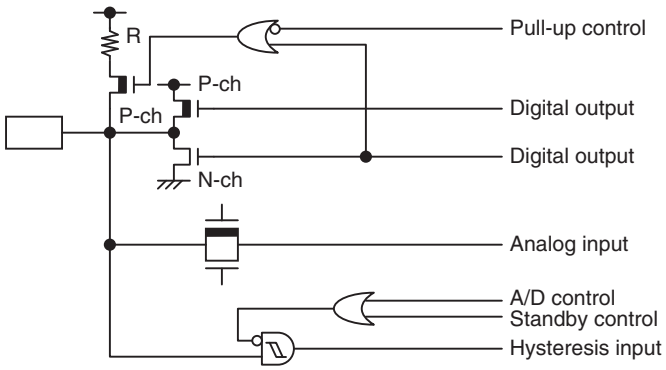
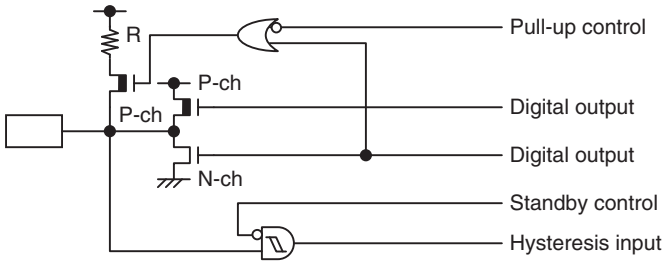
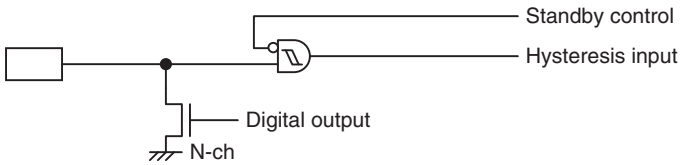
*: For the I/O circuit types, see “I/O Circuit Type”.

8. Pin Functions (MB95580H Series, 32 pins)

Pin no.	Pin name	I/O circuit type*	Function
1	PF1	B	General-purpose I/O port
	X1		Main clock I/O oscillation pin
2	PF0	B	General-purpose I/O port
	X0		Main clock input oscillation pin
3	V_{SS}	—	Power supply pin (GND)
4	PG2	C	General-purpose I/O port
	X1A		Subclock I/O oscillation pin
5	PG1	C	General-purpose I/O port
	X0A		Subclock input oscillation pin
6	V_{CC}	—	Power supply pin
7	C	—	Decoupling capacitor connection pin
8	PF2	A	General-purpose I/O port
	$\overline{RST}$		Reset pin Dedicated reset pin on MB95F582H/F583H/F584H
9	NC	—	It is an internally connected pin. Always leave it unconnected.
10			
11			
12			
13			
14			
15			
16			
17	P01	D	General-purpose I/O port High-current pin
	AN01		A/D converter analog input pin
18	P02	D	General-purpose I/O port High-current pin
	INT02		External interrupt input pin
	AN02		A/D converter analog input pin
	SCK		LIN-UART clock I/O pin
19	P03	D	General-purpose I/O port High-current pin
	INT03		External interrupt input pin
	AN03		A/D converter analog input pin
	SOT		LIN-UART data output pin

Pin no.	Pin name	I/O circuit type*	Function
20	P04	D	General-purpose I/O port
	INT04		External interrupt input pin
	AN04		A/D converter analog input pin
	SIN		LIN-UART data input pin
	EC0		8/16-bit composite timer ch. 0 clock input pin
21	P05	D	General-purpose I/O port High-current pin
	INT05		External interrupt input pin
	AN05		A/D converter analog input pin
	TO00		8/16-bit composite timer ch. 0 output pin
22	P06	E	General-purpose I/O port High-current pin
	INT06		External interrupt input pin
	TO01		8/16-bit composite timer ch. 0 output pin
23	P12	F	General-purpose I/O port
	EC0		8/16-bit composite timer ch. 0 clock input pin
	DBG		DBG input pin
24	P07	E	General-purpose I/O port High-current pin
	INT07		External interrupt input pin
25	NC	—	It is an internally connected pin. Always leave it unconnected.
26			
27			
28			
29			
30			
31			
32			

*: For the I/O circuit types, see “I/O Circuit Type”.

Type	Circuit	Remarks
D		• CMOS output • Hysteresis input • Pull-up control available • Analog input
E		• CMOS output • Hysteresis input • Pull-up control available
F		• N-ch open drain output • Hysteresis input

11. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

11.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- **Absolute Maximum Ratings**

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

- **Recommended Operating Conditions**

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

19. I/O Map (MB95570H Series)

Address	Register abbreviation	Register name	R/W	Initial value
0000H	PDR0	Port 0 data register	R/W	00000000B
0001H	DDR0	Port 0 direction register	R/W	00000000B
0002H	PDR1	Port 1 data register	R/W	00000000B
0003H	DDR1	Port 1 direction register	R/W	00000000B
0004H	—	(Disabled)	—	—
0005H	WATR	Oscillation stabilization wait time setting register	R/W	11111111B
0006H	PLLC	PLL control register	R/W	000X0000B
0007H	SYCC	System clock control register	R/W	XXX11011B
0008H	STBC	Standby control register	R/W	00000000B
0009H	RSRR	Reset source register	R/W	000XXXXXB
000AH	TBTC	Time-base timer control register	R/W	00000000B
000BH	WPCR	Watch prescaler control register	R/W	00000000B
000CH	WDTC	Watchdog timer control register	R/W	00XX0000B
000DH	SYCC2	System clock control register 2	R/W	XXXX0011B
000EH	STBC2	Standby control register 2	R/W	00000000B
000FH to 0027H	—	(Disabled)	—	—
0028H	PDRF	Port F data register	R/W	00000000B
0029H	DDRF	Port F direction register	R/W	00000000B
002AH, 002BH	—	(Disabled)	—	—
002CH	PUL0	Port 0 pull-up register	R/W	00000000B
002DH to 0035H	—	(Disabled)	—	—
0036H	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	00000000B
0037H	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	00000000B
0038H to 0049H	—	(Disabled)	—	—
004AH	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	00000000B
004BH	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	00000000B
004CH, 004DH	—	(Disabled)	—	—
004EH	LVDR	LVDR reset voltage selection ID register	R/W	00000000B
004FH to 006BH	—	(Disabled)	—	—

21. Interrupt Source Table (MB95560H Series)

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

23. Interrupt Source Table (MB95580H Series)

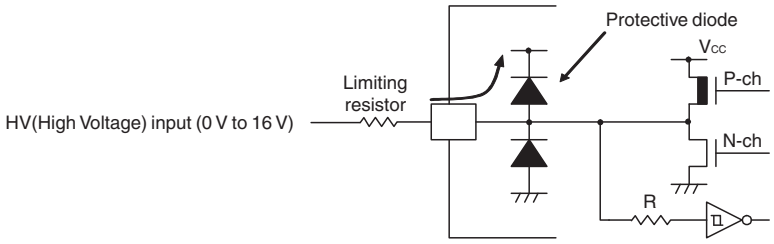
Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 4	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High
External interrupt ch. 5	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
—	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
LIN-UART (reception)	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
LIN-UART (transmission)	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
—	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
—	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
—	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
—	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
—	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
—	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
—	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

*3: Applicable to the following pins: P00 to P07, P62 to P64, PF0, PF1, PG1, PG2 (P00, and P62 to P64 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K. P01, P02, P03, P07, PF0. PF1, PG1, and PG2 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K/F582H/F582K/F583H/F583K/F584H/F584K.)

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit:

  - Input/Output equivalent circuit



*4: P62 and P63 are only available on MB95F562H/F562K/F563H/F563K/F564H/F564K.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

24.2 Recommended Operating Conditions

(V_{SS} = 0.0 V)

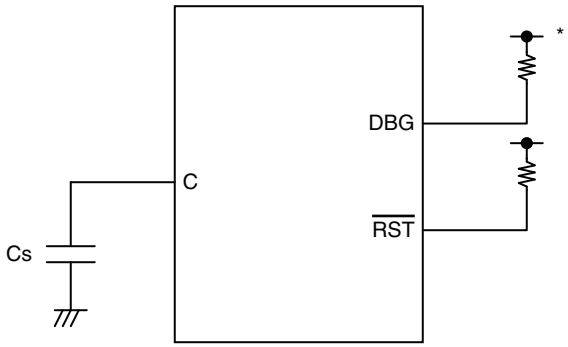
Parameter	Symbol	Value		Unit	Remarks	
		Min	Max			
Power supply voltage	V_{CC}	2.4*1, *2	5.5*1	V	In normal operation	Other than on-chip debug mode
		2.3	5.5		Hold condition in stop mode	
		2.9	5.5		In normal operation	On-chip debug mode
		2.3	5.5		Hold condition in stop mode	
Decoupling capacitor	C_S	0.022	1	µF	*3	
Operating temperature	T_A	−40	+85	°C	Other than on-chip debug mode	
		+5	+35		On-chip debug mode	

*1: The value varies depending on the operating frequency, the machine clock and the analog guaranteed range.

*2: The minimum power supply voltage becomes 2.88 V when a product with the low-voltage detection reset is used.

*3: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The decoupling capacitor for the V_{CC} pin must have a capacitance equal to or larger than the capacitance of C_S. For the connection to a decoupling capacitor C_S, see the diagram below. To prevent the device from unintentionally entering an unknown mode due to noise, minimize the distance between the C pin and C_S and the distance between C_S and the V_{SS} pin when designing the layout of a printed circuit board.

- DBG / $\overline{RST}$ / C pins connection diagram



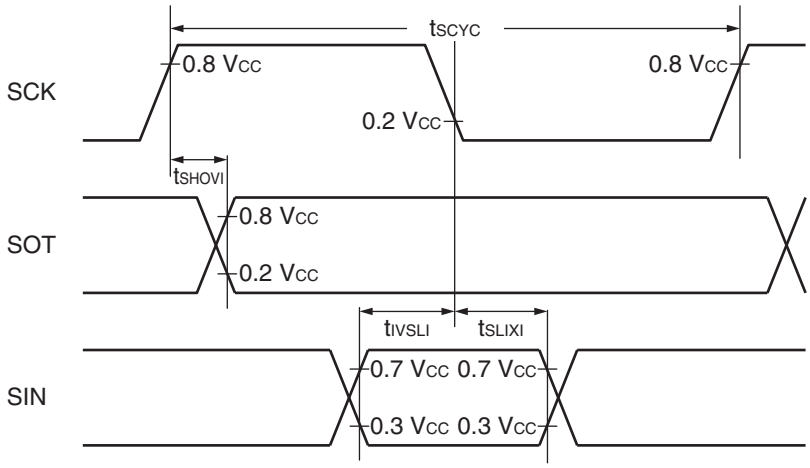
*: Connect the DBG pin to an external pull-up resistor of 2 kΩ or above. After power-on, ensure that the DBG pin does not stay at “L” level until the reset output is released. The DBG pin becomes a communication pin in debug mode. Since the actual pull-up resistance depends on the tool used and the interconnection length, refer to the tool document when selecting a pull-up resistor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

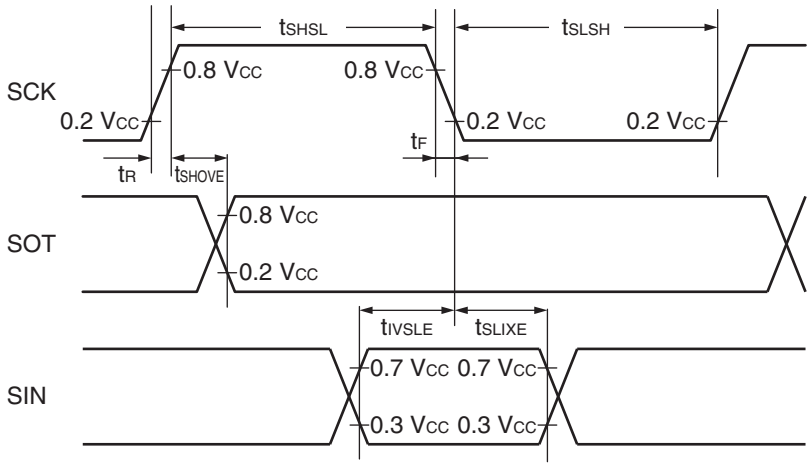
Any use of semiconductor devices will be under their recommended operating condition.
Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

- Internal shift clock mode



- External shift clock mode



Sampling is executed at the rising edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 0, ECCR register: SCDE bit = 1)

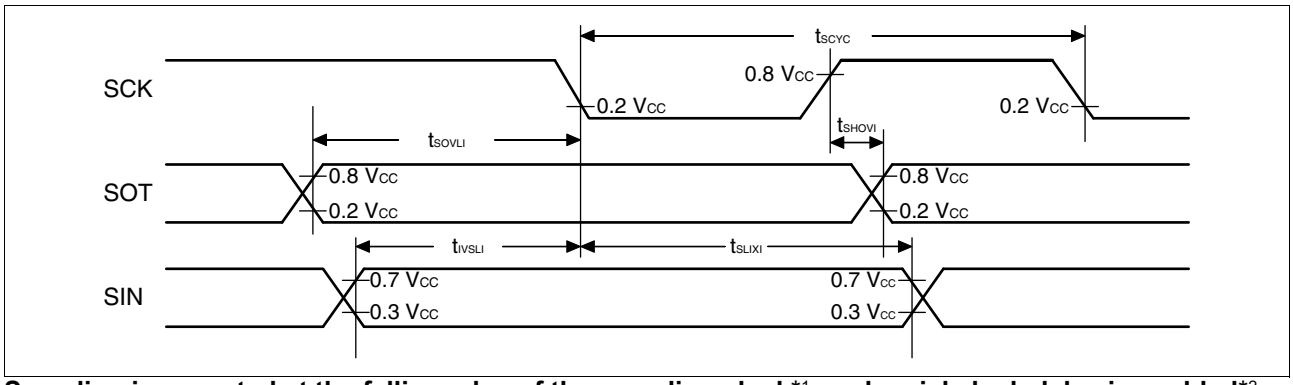
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operation output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↑→ SOT delay time	t_{SHOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↓	t_{IVSLI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↓→ valid SIN hold time	t_{SLIXI}	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCK, SOT		3 t_{MCLK}*3 – 70	—	ns

*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

*3: See “Source Clock / Machine Clock” for t_{MCLK}.



Sampling is executed at the falling edge of the sampling clock*1, and serial clock delay is enabled*2. (ESCR register: SCES bit = 1, ECCR register: SCDE bit = 1)

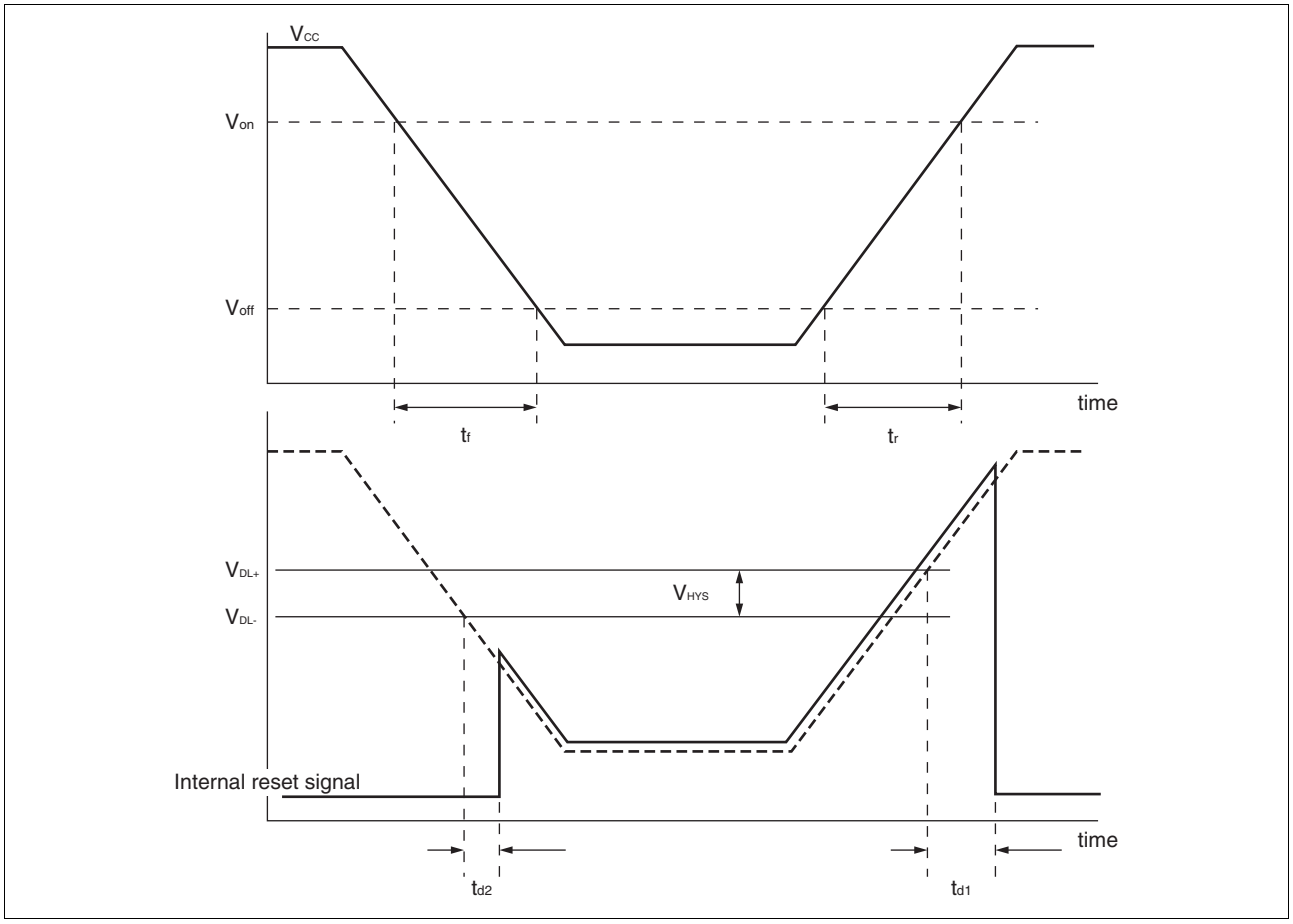
(V_{CC} = 5.0 V ± 10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCK	Internal clock operating output pin: C_L = 80 pF + 1 TTL	5 t_{MCLK}*3	—	ns
SCK ↓→ SOT delay time	t_{SLOVI}	SCK, SOT		–50	+50	ns
Valid SIN → SCK ↑	t_{IVSHI}	SCK, SIN		t_{MCLK}*3 + 80	—	ns
SCK ↑→ valid SIN hold time	t_{SHIXI}	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCK, SOT		3 t_{MCLK}*3 – 70	—	ns

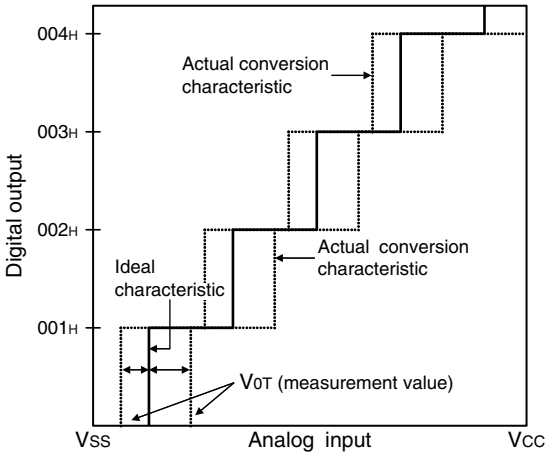
*1: There is a function used to choose whether the sampling of reception data is performed at a rising edge or a falling edge of the serial clock.

*2: The serial clock delay function is a function that delays the output signal of the serial clock for half clock.

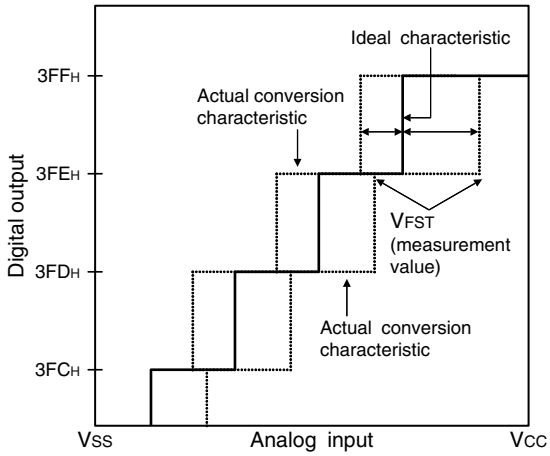
*3: See “Source Clock / Machine Clock” for t_{MCLK}.


Vcc
Von
Voff
time
tf
tr
VDL+
VDL-
VHYS
Internal reset signal
time
td2
td1

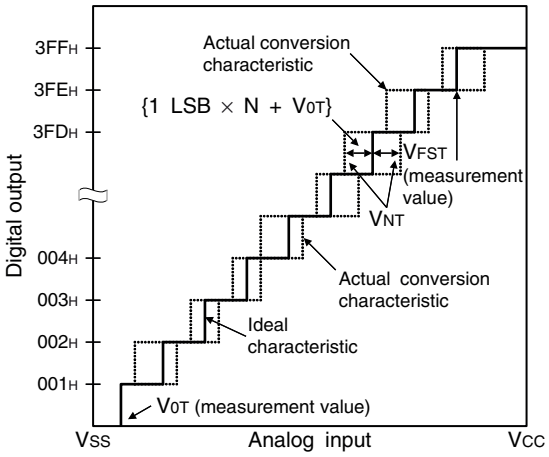
Zero transition error



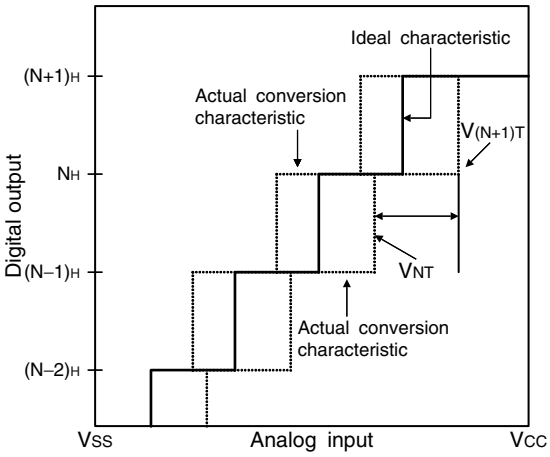
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

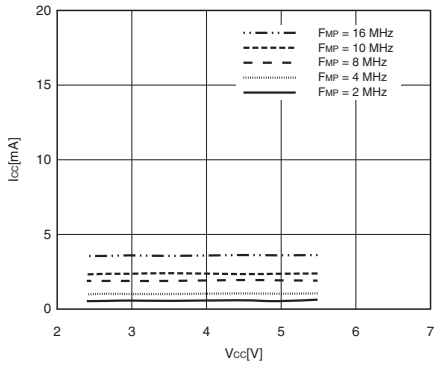
V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} – 2 LSB [V]

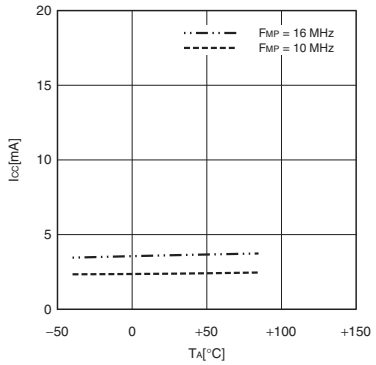
25. Sample Characteristics

- Power supply current temperature characteristics

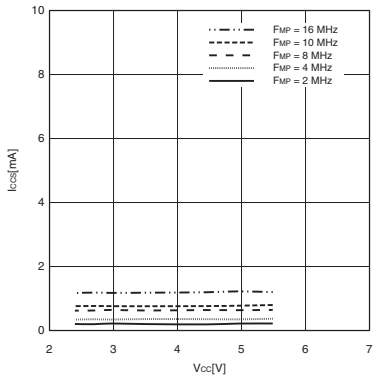
I_{CC} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



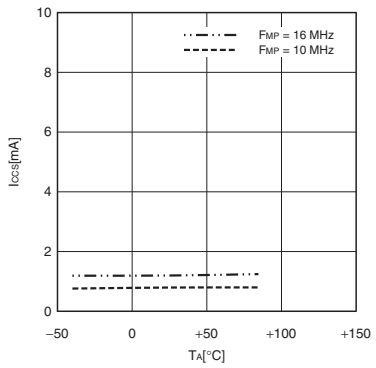
I_{CC} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main clock mode with the external clock operating



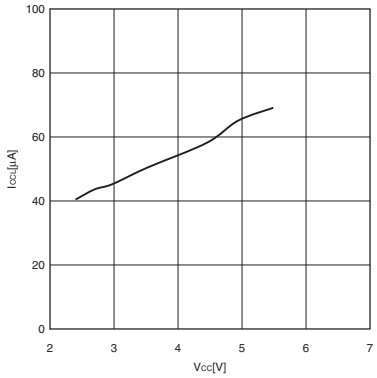
I_{CCS} – V_{CC}
T_A = +25 °C, F_{MP} = 2, 4, 8, 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



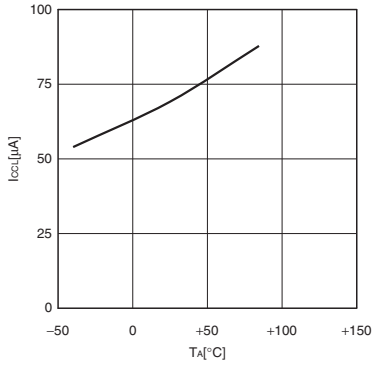
I_{CCS} – T_A
V_{CC} = 5.5 V, F_{MP} = 10, 16 MHz (divided by 2)
Main sleep mode with the external clock operating



I_{CCL} – V_{CC}
T_A = +25 °C, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



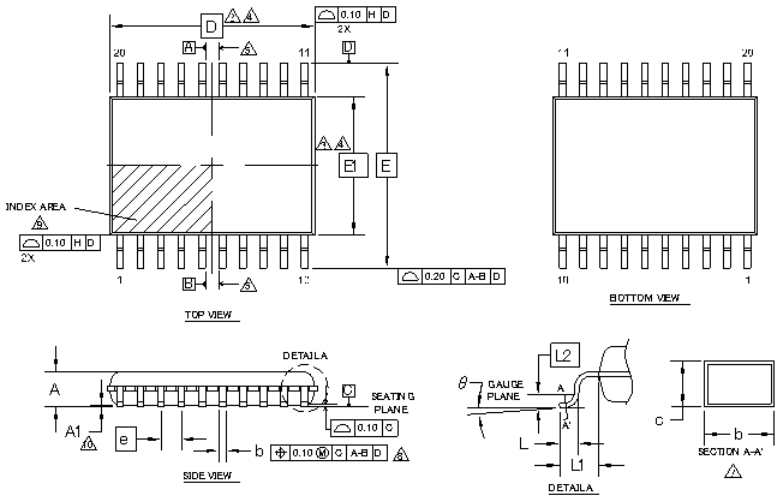
I_{CCL} – T_A
V_{CC} = 5.5 V, F_{MPL} = 16 kHz (divided by 2)
Subclock mode with the external clock operating



26. Mask Options

No.	Part Number	MB95F562H MB95F563H MB95F564H MB95F572H MB95F573H MB95F574H MB95F582H MB95F583H MB95F584H	MB95F562K MB95F563K MB95F564K MB95F572K MB95F573K MB95F574K MB95F582K MB95F583K MB95F584K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

Package Type	Package Code
TSSOP 20	STG020



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	6.50 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.20	0.24	0.28
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
3. DIMENSIONING D INCLUDE MOLD FLASH. DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF: N/A

PACKAGE OUTLINE, 20 LEAD TSSOP
6.50X6.40X1.20 MM STG020 REV**

002-15916 **