Welcome to E-XFL.COM

## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | Power Line Communications |
| Core Processor | ADD8051C3A |
| Program Memory Type | SRAM |
| Controller Series | - |
| RAM Size | 128K x 8 |
| Interface | SPI, UART |
| Number of I/O | 20 |
| Voltage - Supply | 3V ~ 3.6V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (16x16) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/atpl00b-azu-y |

Table 3-1. **Pin Description List (Continued)**

| Pin Number | Pin Name | Type | Comments |
|---|---|---|---|
| 34, 35, 36, 37 | TRIAC(3:0) | Output | TRIAC outputs<br>• These four pins are outputs to control home automation devices by the ATPL00B dimmer peripheral. TRIAC outputs can be configured to work as phase angle controllers or as PWM controllers |
| 38 | P5.5/TxD1/INTA1 | I/O | Microcontroller port 5.5 / Standard Serial Port 1 Tx / Dimmer switch 1<br>• When configured as P5.5, this pin is a pseudo-bidirectional microcontroller I/O port<br>• When configured as TxD1, this pin is the digital output of the asynchronous standard serial port 1<br>• When configured as INTA1, this pin is the input to dimmer peripheral signal INTERR(1)<br>• Internal configuration: 33kΩ typ. pull-up resistor |
| 39 | P5.4/RxD1/INTA0 | I/O | Microcontroller port 5.4 / Standard Serial Port 1 Rx / Dimmer switch 0<br>• When configured as P5.4, this pin is a pseudo-bidirectional microcontroller I/O port<br>• When configured as RxD1, this pin is the digital input of the asynchronous standard serial port 1<br>• When configured as INTA0, this pin is the input to dimmer peripheral signal INTERR(0)<br>• Internal configuration: 33kΩ typ. pull-up resistor |
| 40 | P4.7/T2EX/INTA3 | I/O | Microcontroller port 4.7 / T2EX / Dimmer switch 3<br>• When configured as P4.7, this pin is a pseudo-bidirectional microcontroller I/O port<br>• When configured as T2EX, this pin is the Timer/Counter 2 capture/reload trigger described in Timer2 section<br>• When configured as INTA3, this pin is the input to dimmer peripheral signal INTERR(3)<br>• Internal configuration: 33kΩ typ. pull-up resistor |
| 41 | P4.6/T2/INTA2 | I/O | Microcontroller port 4.6 / T2 / Dimmer switch 2<br>• When configured as P4.6, this pin is a pseudo-bidirectional microcontroller I/O port<br>• When configured as T2, this pin works as the external T2 pin described in Timer2 section<br>• When configured as INTA2, this pin is the input to dimmer peripheral signal INTERR(2)<br>• Internal configuration: 33kΩ typ. pull-up resistor |
| 42 | P1.7/SSN | I/O | Microcontroller port 1.7 / Silicon Serial Number<br>• When configured as P1.7, this pin is a pseudo-bidirectional microcontroller I/O port<br>• This pin is the digital input used to read a Serial number if a valid SSN device is being used. This Serial Number is used for encryption purposes. Precaution should be taken if used as generic control port since it searches for a Silicon Serial Number device at start-up and could put out undesirable transient values<br>• Internal configuration: 33kΩ typ. pull-up resistor |

Common and extended memory sizes vary depending on the value in P0(7:6), as shown above. According to these size values, the core knows when the PC is pointing to an address located in common memory and when it is pointing to an address located in extended memory. When PC is pointing to an address in extended memory, then P0(5:0) indicates the extended page number and the physical address is automatically calculated. Some examples are shown below.

**Example:** SX(1:0)=”00” (common memory size = 32KB)

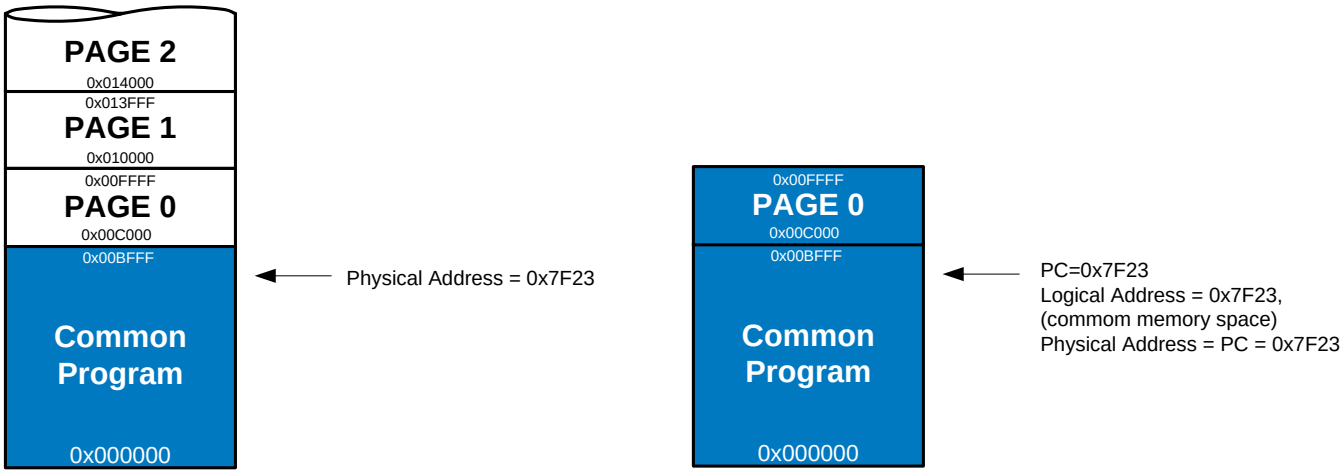
PC=0x7F23 (PC pointing to an address in common memory space)

P0(5:0)= don’t care

LOGIC ADDRESS=0x7F23, common memory space

PHYSICAL ADDRESS=0x7F23 (common memory space → P0(5:0) is ignored)

**Figure 4-5. Extended Addressing example 1**



The functions of some SFRs are described in the text below, while others are described with their related peripherals.

- **Accumulator (address: E0H**)

  ACC is the Accumulator register. Note that mnemonics for accumulator specific instructions usually refer to the Accumulator simply as A.

- **B Register (address: F0H)**

  The B register is used during multiply and divide operations. For other instructions it can be treated as another scratch pad register.

- **PSW register (address: D0H)**

  The PSW register contains program status information as detailed below.

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **PSW** | CY | AC | F0 | RS1 | RS0 | OV | F1 | P |

  - CY: Carry flag
  - AC: Auxiliary carry flag
  - F0: General purpose flag
  - RS(1:0): Register bank select control bits
  - OV: Overflow flag
  - F1: User definable flag
  - P: Parity flag

- **Stack Pointer (address: 81H)**

  8 bit stack pointer that is initialized to internal memory of 07H. The user program can initialize it at any internal RAM location ranging from 07H to FFH.

- **Auxiliary 1**

  The AUX1 register includes the data pointer selection bit, the software reset control and the switch to enable wake-up from power-down using external interrupts.

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **AUX1** | -- | -- | SRST | GF2 | WUPD | 0 | -- | DPS |

  - --: Reserved bits
  - SRST: Software reset
  - GF2: General purpose flag
  - WUPD: When set, enables external interrupts driven wake-up from power down
  - 0: fixed ‘0’
  - DPS: Data pointer selector, selects between DPTR0 and DPTR1

- **P0, P1, P2, P3, P4, P5 registers**

  P1, P3, P4 and P5 are the SFR registers of Ports 1, 3, 4 and 5 respectively.

  Writing a one/zero to a bit in these registers causes the corresponding port output pin to switch high/low. When a port bit is used as an input the corresponding port SFR must be set to ‘1’.

  Ports 3, 4 and 5 are pseudo bidirectional by default, and can be configured to push-pull or pseudo bidirectional using SFRs P3M, P4M and P5M respectively, as follows: when P4M(i) is set, P4(i) is configured as push-pull.

Table 4-8. **Boolean Instructions**

| MNEMONIC | OPERATION | EXECUTION TIME (mc) |
|---|---|---|
| **ANL C,bit** | C = C.AND.bit | 1 |
| **ANL C,/bit** | C = C.AND..NOT.bit | 1 |
| **ORL C,bit** | C = C.OR.bit | 1 |
| **ORL C,/bit** | C = C.OR..NOT.bit | 1 |
| **MOV C,bit** | C = bit | 1 |
| **MOV bit,C** | bit = C | 1 |
| **CLR C** | C = 0 | 1 |
| **CLR bit** | bit = 0 | 1 |
| **SETB C** | C = 1 | 1 |
| **SETB bit** | bit = 1 | 1 |
| **CPL C** | C = .NOT.C | 1 |
| **CPL bit** | bit = .NOT.bit | 1 |
| **JC rel** | Jump if C = 1 | 2 |
| **JNC rel** | Jump if C = 0 | 2 |
| **JB bit,rel** | Jump if bit = 1 | 2 |
| **JNB bit,rel** | Jump if bit = 0 | 2 |
| **JBC bit,rel** | Jump if bit = 1; CLR bit | 2 |

**Relative Offset**

The destination address for these jumps is specified to the assembler by a label or by an actual address in Program memory. However, the destination address assembles to a relative offset byte. This is a signed (two's complement) offset byte which is added to the PC in two's complement arithmetic if the jump is executed. The range of the jump is therefore –128 to +127 Program Memory bytes relative to the first byte following the instruction.

### 4.4.7 Jump Instructions

Table 4-9 shows the list of unconditional jumps and the execution time associated.

The table lists SJMP, LJMP, and AJMP, which differ in the format of the destination address. JMP is a generic mnemonic which can be used if the programmer does not care which way the jump is encoded.

The SJMP instruction encodes the destination address as a relative offset, as described above. The instruction is 2 bytes long, consisting of the opcode and the relative offset byte. The jump distance is limited to a range of –128 to +127 bytes relative to the instruction following the SJMP.

The LJMP instruction encodes the destination address as a 16-bit constant. The instruction is 3 bytes long, consisting of the opcode and two address bytes. The destination address can be anywhere in the 64k Program Memory space.

Table 4-13. **P3, P4, P5 ports Alternate Functions**

| Pin | Alternate Function |
|---|---|
| P3.0 | RxD (serial port 0 input) |
| P3.1 | TxD (serial port 0 output) |
| P3.2 | INT0 (external interrupt 0) |
| P3.3 | INT1 (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | WR(external data memory write strobe) |
| P3.7 | RD (external data memory read strobe) |
| P4.0 | RxD (serial port 2 input) |
| P4.1 | TxD (serial port 2 output) |
| P4.2 | SS1 (SPI1 slave select input) |
| P4.3 | SPICLK1 (SPI1 clock input/output) |
| P4.4 | MOSI1 (SPI1 master out / slave in data) |
| P4.5 | MISO1 (SPI1 master in / slave out data |
| P4.6 | T2 (timer 2 input/output) |
| P4.7 | T2EX (timer 2 external input) |
| P5.0 | SS (SPI0 slave select input) |
| P5.1 | SPICLK (SPI0 clock input/output) |
| P5.2 | MOSI (SPI0 master output / slave input data) |
| P5.3 | MISO (SPI0 master input / slave output data) |
| P5.4 | RxD (serial port 1 input) |
| P5.5 | TxD (serial port 1 output) |

Note: To use an Alternate Function the corresponding bit (or bits) in the SFR must contain a 1.

### 4.7.1 I/O Configurations

Figure 4-13 and Figure 4-14 show a functional diagram of bit register and I/O buffer in each of the four ports. The level of the port pin is placed on the internal bus and instructions can read the port pin value or the SFR register value.

If a bit in a register with AOF (Alternate Output Function) contains a 1, then the output level is controlled by the signal labeled “Alternate Output function”.

**Figure 4-13. Pins with AOF structure**

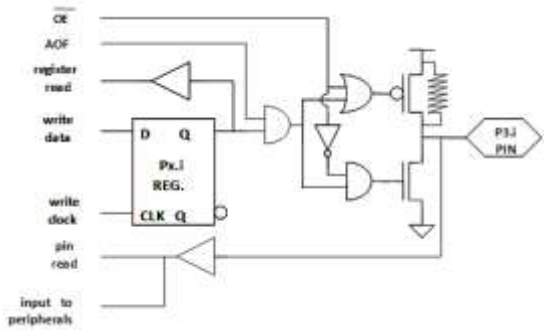


Table 5-1. **Timer 2 operating modes**

| Mode | T2CON(5) OR T2CON(4) | CP/RL2 | T2OE |
|---|---|---|---|
| Auto-reload | 0 | 0 | 0 |
| Programmable clock-out | 0 | 0 | 1 |
| Capture | 0 | 1 | 0 |
| *stopped* | 0 | 1 | 1 |
| Baud Rate generator | 1 | X | X |

Timer 2 operation is similar to timer 0 and timer 1. C/T2 selects between timer operation mode (internal clock input) or counter operation mode (external pin T2 as the time register input). Setting TR2 allows TL2 to be incremented by the selected input.

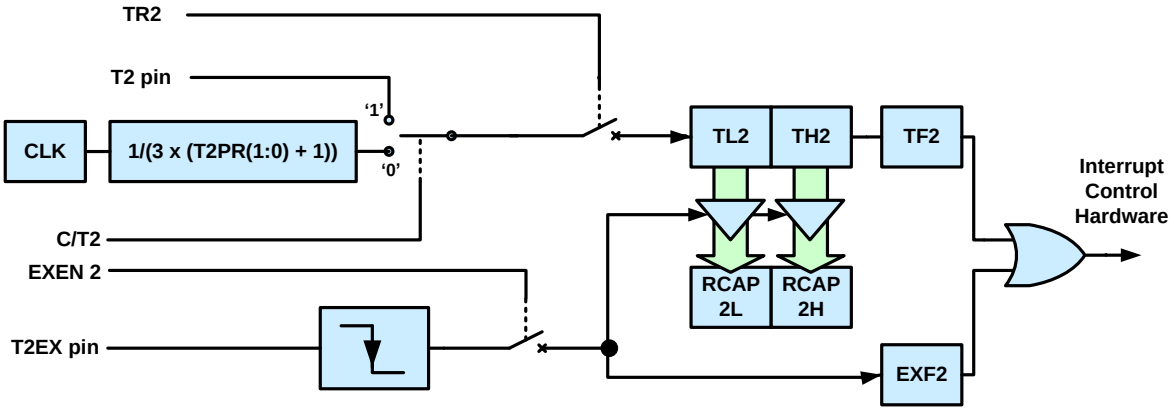
The timer 2 related interrupt flags (TF2, EXF2) can be configured to be cleared by hardware when the interrupt routine is vectored to, or by user software using TF2SC and EXF2SC.

The operating modes are described in the following paragraphs.

### 5.2.2 Capture mode

In the capture mode, timer 2 operates as a 16-bit timer or counter. An overflow condition sets bit TF2, which can be used to request an interrupt. Setting the external enable bit EXEN2 allows the RCAP2H and RCAP2L registers to capture the current value in timer registers TH2 and TL2 in response to a 1-to-0 transition at external input T2EX. The transition at T2EX also sets bit EXF2 in T2CON. The EXF2 bit, like TF2, can generate an interrupt.

**Figure 5-3. Timer 2 capture mode**




### 5.2.3 Auto-Reload mode

The auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. The timer operates as an up counter or as an up/down counter, as determined by the down counter enable bit (DCEN). When reset occurs, DCEN is cleared, so in the auto-reload mode, timer 2 in configured as an up counter by default.

When timer 2 is configured as a timer and in baud rate generator mode, do not read or write the TH2 or TL2 registers. The timer is being incremented every state time, and the results of a read or write may not be accurate. In addition, user shall read, but not write to, the RCAP2 registers; a write may overlap a reload and cause write and/or reload errors.

Table 5-3 lists commonly used baud rates and shows how they are generated by timer 2.

Table 5-3. **Timer 2 generated baud rates with a 11.0592MHz oscillator**

| Baud rate | T2PRE | RCAP2H | RCAP2L |
|---|---|---|---|
| 230400 | 0 | FF | FF |
| 115200 | 0 | FF | FE |
| 57600 | 0 | FF | FC |
| 38400 | 0 | FF | FA |
| 19200 | 0 | FF | F4 |
| 9600 | 0 | FF | E8 |
| 4800 | 0 | FF | D0 |
| 2400 | 0 | FF | A0 |
| 1200 | 0 | FF | 40 |
| 600 | 0 | FE | 80 |
| 300 | 0 | FD | 0 |
| 150 | 0 | FA | 0 |
| 110 | 0 | F7 | D2 |

## 5.3 Watchdog (timer 3)

The watchdog timer includes a 18-bit preescaler which is set to 0 when T3 is reloaded.

T3 is active only when /EWDG pin is tied to ‘0’.

T3 must be reloaded by software to avoid T3 rollover and program restart.

Reload of T3 is allowed only if WLE watchdog load enable (PCON(4)) is set.

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **PCON** | SMOD | -- | -- | WLE | GF1 | GF0 | PD | IDL |

- SMOD: Doubles baud rate bit when timer 1 is used as time generator and serial port is in modes 1,2 or 3
- --: Reserved bit
- WLE: Watchdog load enable. It must be set by software to enable T3 reload. WLE is reset by hardware 13 machine cycles after been set by user software.
- GF1: General purpose flag bit, user programmable
- GF0: General purpose flag bit, user programmable
- PD: Sets power down mode
- IDL: Sets idle mode

Reload of T3 register automatically resets the preescaler and WLE

Table 7-1. **SPI0 port map**

| ADD8051C3A Port | Alternate Function |
|---|---|
| P5.0 | /SS0 |
| P5.1 | SPICLK0 |
| P5.2 | MOSI0 |
| P5.3 | MISO0 |

SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on the MOSI (Master Out Slave In) pin and flows from slave to master on the MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e. SPEN (SPCTL.6) = 0 (reset value), these pins can be used as general purpose I/O pins.

SS is an optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its SS pin to determine whether it is selected or not. The SS is ignored if any of the following conditions are true:

- The SPI0 system is disabled, i.e. SPEN (SPCTL.6) = 0 (reset value)
- SPI0 is enabled but SS pin is not needed in such system, i.e. SSIG(SPCTL.7) = 1; in this case SS pin can be used as general purpose pin on P5.

### 7.1.2 SPI clock phase, polarity and operation

There are four combinations (CPHA, CPOL) for sampling and shifting activities on data and clock lines in the SPI. Master can switch between any of them at any time thus having ability to communicate with slaves supporting data transfer using different modes.

In order to have successful data transfer between SPI devices, proper selection of the SPI clock phase and polarity is crucial. It is important to note that some of these configurations offer less capabilities than others. Clock Phase Bit CPHA allows user to specify the edges for sampling and shifting data. Clock Polarity bit CPOL allows user to set the clock polarity Figure 7-2 and Figure 7-3 show transfers with different values of CPHA and CPOL.

The SPI clock preescaler selection uses the PSC1-PSC0 bits in the SPCTL register and PSC2 in SPSTAT register. Master selects one of the available baud rates for the SPI communication. SPI Clock Preescaler bits do not have affect on the part acting as a slave, since it uses SPI clock supplied by the master.

When microcontroller operates as a slave with CPHA=’0’, some restrictions are present.

- SSIG must be ‘0’ and the SS pin must be negated and reasserted between each successive byte transfer.
- If the SPDAT register is written while SS is active (low), a write collision error results.
- Microcontroller’s behavior is undefined if CPHA is ‘0’ and SSIG is ‘1’.

On the other hand, slave having CPHA=’1’ may set SSIG to ‘1’. If SSIG = 1, the SS pin may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line. Microcontroller configured as a master with CPHA=’0’ does not need to negate and reassert slave’s SS line in order to send and receive byte(s) of data.

In SPI, transfers are always initiated by the master. If the SPI is enabled (SPEN = 1) and microcontroller is configured as SPI master, writing to the SPI data register by the master will start the SPI clock generator and data transfer. The data will start to appear on MOSI about one half SPI bit-time to one SPI bit-time after data is written to SPDAT.

**Figure 7-2. SPI0 transfer with CPHA=0**

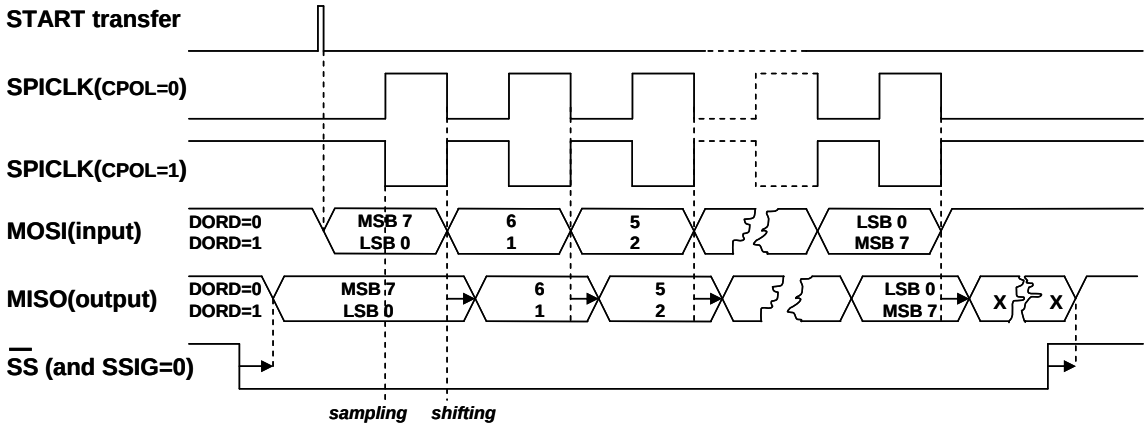
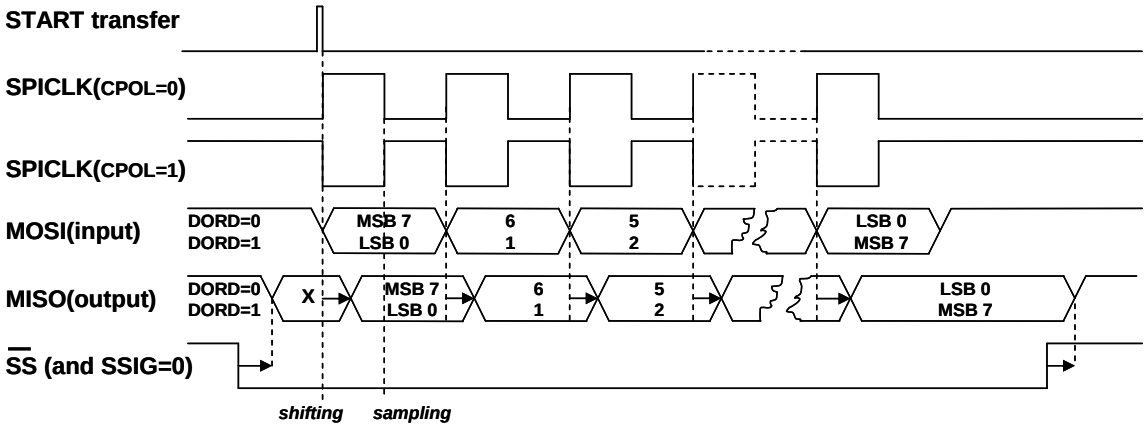


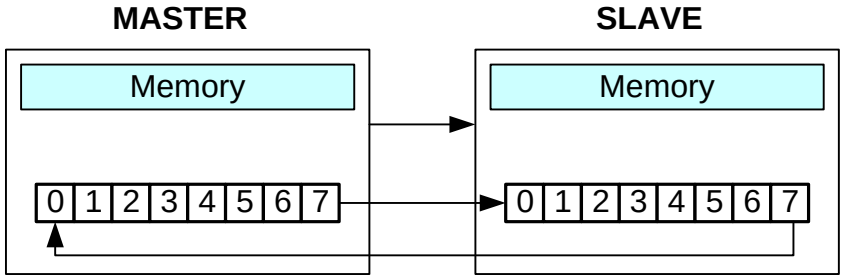

**Figure 7-3. SPI0 transfer with CPHA=1**




Note that the master selects a slave by driving the slave select pin of the corresponding slave device. Data written to the SPDAT register of the master is shifted out of the MOSI pin of the master to the MOSI pin of the slave, at the same time the data in SPDAT register on slave side is shifted out on its MISO pin to the MISO pin of the master.

After shifting one byte, the SPI clock generator stops, setting the transfer completion flag (SPIF) and an interrupt will be created if the SPI interrupt is enabled (ESPI, or IEN1.3 = 1). The two shift registers in the master CPU and slave CPU can be considered as one distributed 16-bit circular shift register. When data is shifted from the master to the slave, data is also shifted in the opposite direction simultaneously. This means that during one shift cycle, data in the master and the slave are interchanged.

**Figure 7-4. SPI shift registers**



## 8.3 System startup

When the system is configured in execution mode (/PROG pin is set) and after a power up or reload process, the boot loader checks the system configuration and performs the required operations to ensure the correct execution of the firmware.

Boot loader transfers a volatile copy of the firmware from the flash memory to the SRAM memory starting at address 000000 (Hex). The internal SRAM size is 128Kbytes and the maximum SPI flash size supported is 16Mbits. The part of the SRAM that is not used to store the firmware is used by the system to store the volatile data in the execution process.

The volatile data is stored in the SRAM memory from top to bottom. This arrangement is done automatically by the system, that is, when the microcontroller wants to save data at address A the system automatically converts the target address to (top address – A). Using this storage method, the amount of volatile data that can be stored in the RAM is determined by the firmware size.

The transfer process can last about 400ms depending on flash device and code size. The first time this process will be longer if auto encryption is activated. Auto encryption must be done once, and **care must be taken about respecting encryption times**.

When the transfer process is finished, the microcontroller begins to execute the program and the system is ready to use. The startup cycle is performed each time the system is powered up or when the microcontroller via software or watchdog forces a firmware reload process writing in a specific register.

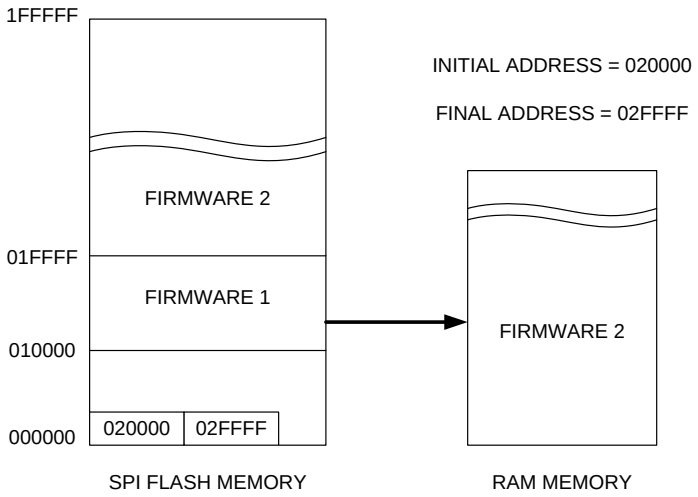
Both the location of the firmware at the SPI flash and the transfer size are configurable. The lower six bytes of the SPI flash are used to store the initial and final position of the firmware (from address 0x000000 to 0x000005).

This feature allows working with a SPI flash device that has multiple firmware versions stored in different addresses. The version to be used can be selected by means of its initial and final addresses.

The transfer size is equal to the firmware size.

Bank-switching is supported, so firmware code bigger than 64KB can be managed. Extreme caution must be taken when using bank-switching in order to respect code and variables spaces and avoid overlapping.

**Figure 8-4. Flash & SRAM memories diagram**



### 9.1.1 DIM_CTRL register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **DIM_CTRL** | -- | -- | -- | -- | FQ | VEZC | REZC | FECZ |

**Name:** DIM_CTRL

**Address:** 0xFEA0

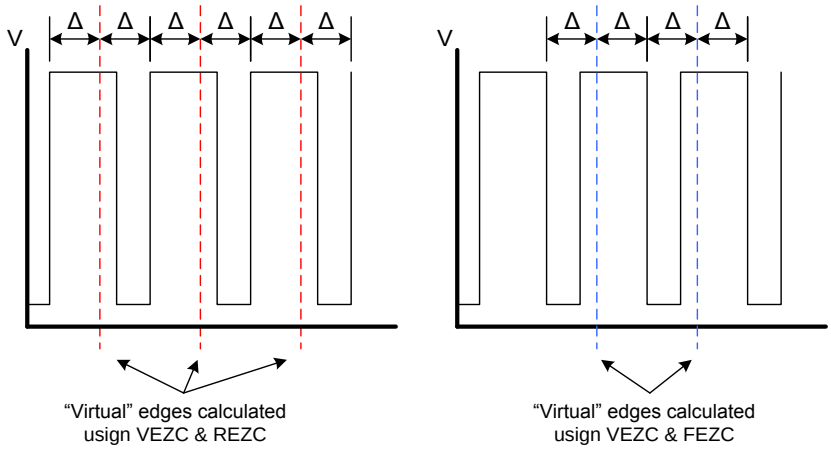
**Reset:** “00000110”

This register selects how to calculate the zero-crossing point depending on the external circuit type connected to VNR pin.

- **--:** Reserved bit
- **FQ:** Selects the mains frequency.
  - ‘0’: 50Hz frequency
  - ‘1’: 60Hz frequency
- **VECZ:** Virtual Edge for Zero Crossing

  In this bit is equal to one, the hardware calculates the middle point between two VNR edges to calculate de zero crossing.

  This mode is useful when the VNR signal duty cycle is different from 50%:




  VECZ can be used simultaneously with REZC or FECZ.

  Using the three of them at a time is not recommended.

- **REZC**: Rising Edge for zero crossing

  If this bit is set to ‘1’, the hardware uses the VNR rising edges to calculate zero-crossing.

  FEZC and REZC can be used simultaneously
- **FECZ**: Falling Edge for Zero Crossing-

  If this bit is set to ‘1’, the hardware uses the VNR falling edges to calculate zero-crossing.

  FEZC and REZC can be used simultaneously

### 9.1.3 OUT_ST register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **OUT_ST** | -- | -- | -- | -- | D3 | D2 | D1 | D0 |

**Name:** OUT_ST

**Address:** 0XFEA2

**Reset:** “00000000”

This register selects which loads are switched on. If PWM mode is selected, then this register is used to indicate which PWM outputs are active.

- **D3:** This bit sets the state of the load connected to TRIAC3 output
  - ‘0’: The load connected to TRIAC3 output is OFF
  - ‘1’: The load connected to TRIAC3 output is ON
- **D2:** This bit sets the state of the load connected to TRIAC2 output
  - ‘0’: The load connected to TRIAC2 output is OFF
  - ‘1’: The load connected to TRIAC2 output is ON
- **D1:** This bit sets the state of the load connected to TRIAC1 output
  - ‘0’: The load connected to TRIAC1 output is OFF
  - ‘1’: The load connected to TRIAC1 output is ON
- **D0:** This bit sets the state of the load connected to TRIAC0 output
  - ‘0’: The load connected to TRIAC0 output is OFF
  - ‘1’: The load connected to TRIAC0 output is ON

### 9.1.7 V_SWC register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **V_SWC** | HVI3 | HVI2 | HVI1 | HVI0 | PWM3 | PWM2 | PWM1 | PWM0 |

**Name:** V_SWC

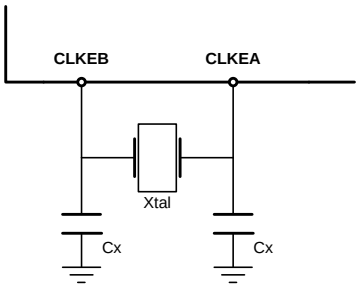
**Address:** 0XFEA9

**Reset:** “11111111”

This register selects the voltage switches type (AC alternating-current high voltage switch or DC direct-current low voltage switch) and activates the PWM (Pulse Width Modulation) control.

- **HVI3:** Selects the switch type (AC switch or DC switch) that is connected to INTERR3 (internal logic acts in different way depending on the switch type)
  - ‘0’: DC switch is connected
  - ’1’: AC switch is connected
- **HVI2:** Selects the switch type (AC switch or DC switch) that is connected to INTERR2 (internal logic acts in different way depending on the switch type)
  - ‘0’: DC switch is connected
  - ’1’: AC switch is connected
- **HVI1:** Selects the switch type (AC switch or DC switch) that is connected to INTERR1 (internal logic acts in different way depending on the switch type)
  - ‘0’: DC switch is connected
  - ’1’: AC switch is connected
- **HVI0:** Selects the switch type (AC switch or DC switch) that is connected to INTERR0 (internal logic acts in different way depending on the switch type)
  - ‘0’: DC switch is connected
  - ’1’: AC switch is connected
- **PWM3:** Sets the behavior of TRIAC3 output mode
  - ‘0’: PWM output
  - ’1’: Phase angle control output
- **PWM2:** Sets the behavior of TRIAC2 output mode
  - ‘0’: PWM output
  - ’1’: Phase angle control output
- **PWM1:** Sets the behavior of TRIAC1 output mode
  - ‘0’: PWM output
  - ’1’: Phase angle control output
- **PWM0:** Sets the behavior of TRIAC0 output mode
  - ‘0’: PWM output
  - ’1’: Phase angle control output

Notes:
1. This pin is part of the JTAG Boundary Scan interface and is only used for boundary scan purposes
2. See supported devices section **8.3.2**
3. The crystal should be located as close as possible to CLKEA and CLKEB pins. Recommended value for Cx is 18pF. This value may depend on the specific crystal characteristics




4. Different configurations allowed depending on external topology and net behavior

# 10. Media Access Layer

In power line communication (PLC) systems, medium access control (MAC) tasks require a high percent of the CPU available computational time. To reduce the computational load of the integrated MCU (8051C3A Core) the ATPL00B accelerates the execution of critical tasks by means of additional specific hardware units such as ADD1210 hardwired MAC unit

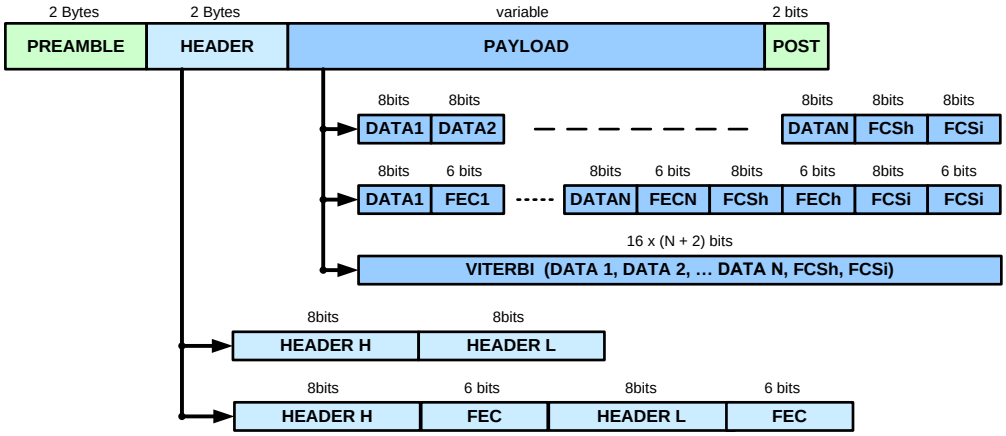
MAC functional capabilities involve the construction of message packets and the management of correction and error detection mechanisms.

The ATPL00B MAC is compatible with EHS and KONNEX. Moreover, its design is very versatile and allows the construction of a wide range of datagram structures with the only constrain of hardware correction and detection codes.

## 10.1 Packet Encapsulation

Depending on enabled error correction and detection mechanisms, MAC can encapsulate packets following different configurations:

**Figure 10-1. Packet Encapsulation diagram**




A standard packet encapsulation has the following structure

**Figure 10-2. Datagram structure**

| 2 byte | 2 byte | variable | 2 bit |
|---|---|---|---|
| PREAMBLE | HEADER | PAYLOAD | POSTAMBLE |

- **Preamble:** two bytes long, containing 0xAAAA for bit synchronization. The preamble size is configurable by a field in CTRL register 10.3.1
- **Header:** two bytes long. It defines the type of datagram. ATPL00B supports FEC (Forward Error Correction) shielded and unshielded headers. In shielded headers, each byte of the header field is protected by a FEC field as shown below:
  - Unshielded header:

| 8-bit | 8-bit |
|---|---|
| Header MSB | Header LSB |

  - Shielded header:

| 8-bit | 6-bit | 8-bit | 6-bit |
|---|---|---|---|
| Header MSB | FEC | Header LSB | FEC |

### 11.3.6 COMP register

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **COMP** | -- | -- | -- | -- | -- | -- | -- | CCLK_IDLE |

**Name:** COMP

**Address:** 0xFE1F

**Reset:** “00000100”

- **--:** Reserved bit
- **CCLK_IDLE:** Converter Clock Idle

  Set the state of the clock that drives the external comparator (ENABLE pin)
  - ‘0’:External Comparator clock enabled
  - ‘1’: External Comparator clock disabled

### 11.3.10 **CD_DECISION_ERROR register**

| Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | B it 0 |
|---|---|---|---|---|---|---|---|---|
| **CD_DECISION_ERROR** | -- | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

**Name:** CD_DECISION_ERROR

**Address:** 0xFE4A

**Reset:** “00001111”

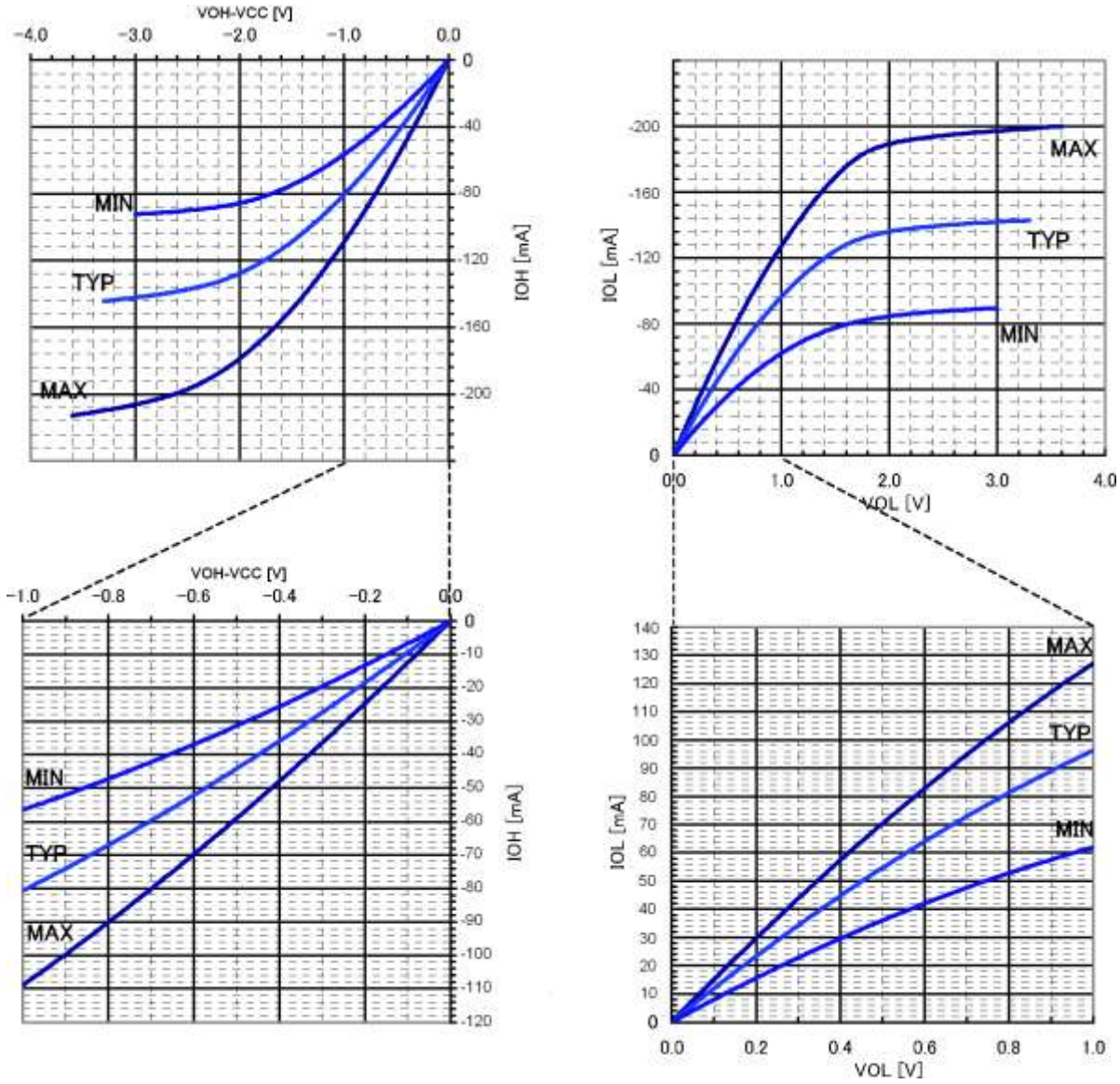
- **--:** Reserved bit
- **D(6:0):** This register sets the number of errors allowed before taking a decision in the automatic carrier detection algorithm.

  It is used only in automatic mode (CD_ENABLE(0)=’1’ ).

**V-I Characteristics 3.3 Vstandard CMOS IO H, V type**
**Pins marked in Table 2-1 - pinout table with Nominal Current I(mA)=±X**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Condition: | MIN | Process= | Slow | Tj= | 125°C | VCC= | 3.0 V |
| | TYP | Process=Typical | | Tj= | 25°C | VCC= | 3.3 V |
| | MAX | Process=Fast | | Tj= | -40°C | VCC= | 3.6 V |

**Figure 12-3. CMOS IO X type, V-I curves**



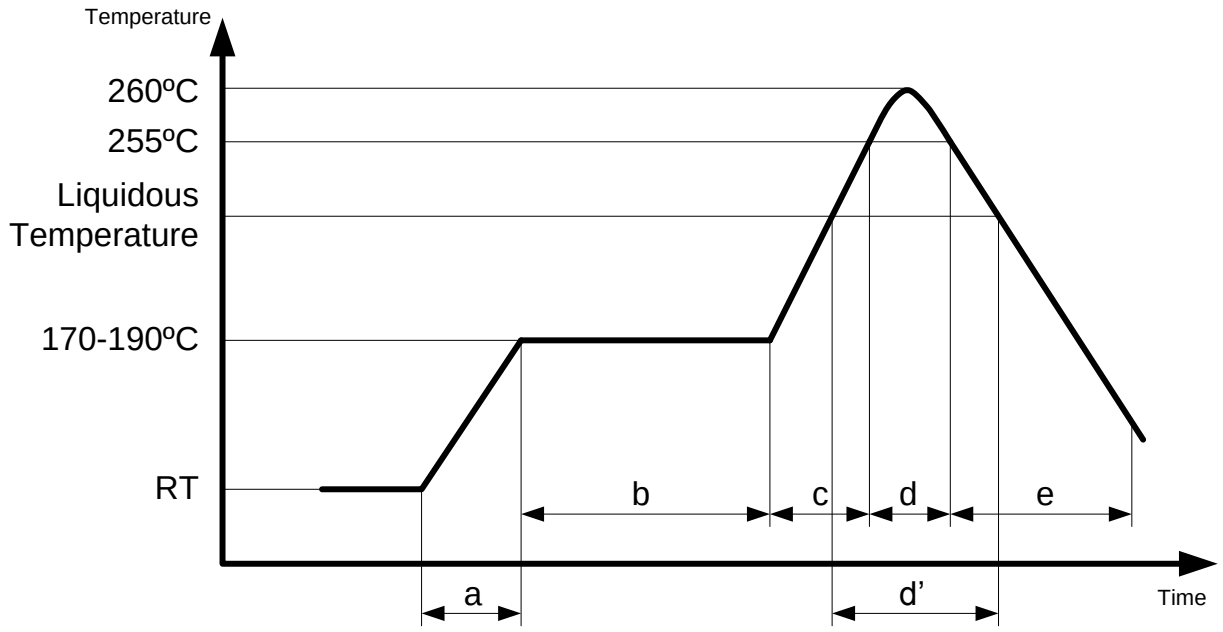
# 14. Recommended mounting conditions

## 14.1 Conditions of Standard Reflow

Table 14-1. **Conditions of standard Reflow**

| Items | Contents | |
|---|---|---|
| Method | IR(Infrared Reflow)/Convection | |
| Times | 2 | |
| Floor Life | Before unpacking | Please use within 2 years after production |
| | From unpacking to second reflow | Within 8 days |
| | In case over period of floor life | Baking with 125ºC +/- 3ºC for 24hrs +2hrs/-0hrs is required. Then please use within 8 days. (please remember baking is up to 2 times) |
| Floor Life Condition | Between 5ºC and 30ºC and also below 70%RH required. (It is preferred lower humidity in the required temp range.) | |

**Figure 14-1. Temperature Profile**




Note: H rank: 260ºC Max

**a:** Average ramp-up rate: 1ºC/s to 4ºC/s

**b:** Preheat & Soak: 170ºC to 190ºC, 60s to 180s

**c:** Average ramp-up rate: 1ºC/s to 4ºC

**d:** Peak temperature: 260ºC Max, up to 255ºC within 10s

**d':** Liquidous temperature: Up to 230ºC within 40s or
Up to 225ºC within 60s or
Up to 220ºC within 80s

**e:** Cooling: Natural cooling or forced cooling