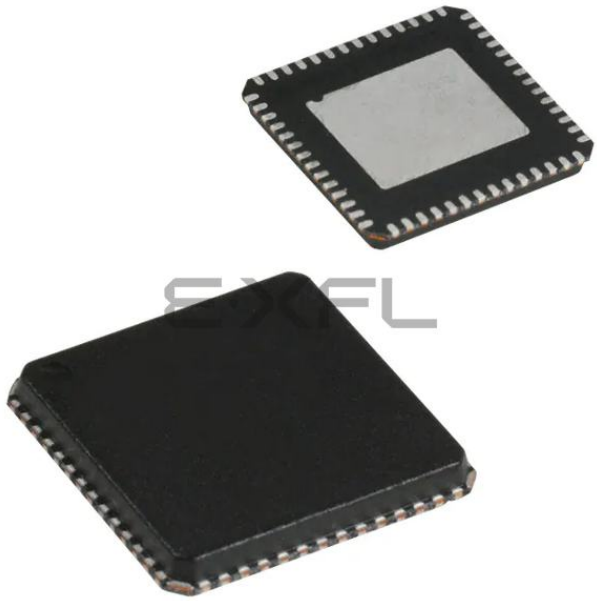

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24894-24lfxi

2. PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with On-Chip Controller devices. All PSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. The PSoC CY8C24x94 devices are unique members of the PSoC family because it includes a full featured, full speed (12 Mbps) USB port. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of industrial, consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources including a full speed USB port. Configurable global busing enables all the device resources to be combined into a complete custom system. The PSoC CY8C24x94 devices can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks.

2.1 The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPI/O (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

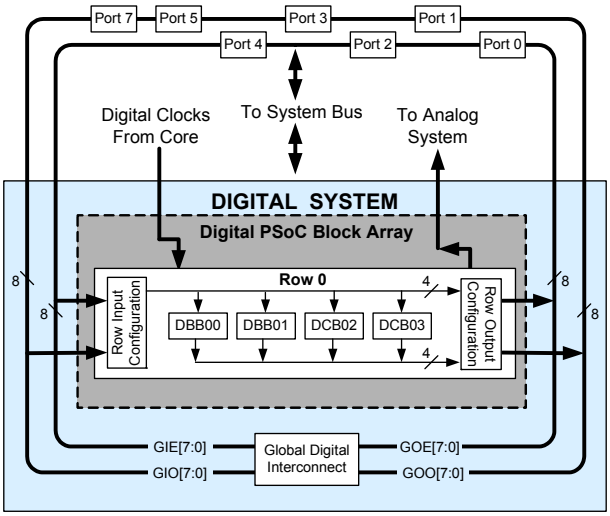
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 8% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device. In USB systems, the IMO self tunes to ± 0.25% accuracy for USB communication.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin is also capable of generating a system interrupt on high level, low level, and change from last read.

2.2 The Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 2-1. Digital System Block Diagram



Digital peripheral configurations include the following:

- Full Speed USB (12 Mbps)
- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPI/O through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees the designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This enables you the optimum choice of system resources for your application. Family resources are shown in Table 2-1 on page 4.

7. Pin Information

This section describes, lists, and illustrates the CY8C24x94 PSoC device family pins and pinout configuration.

The CY8C24x94 PSoC devices are available in the following packages, all of which are shown on the following pages. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

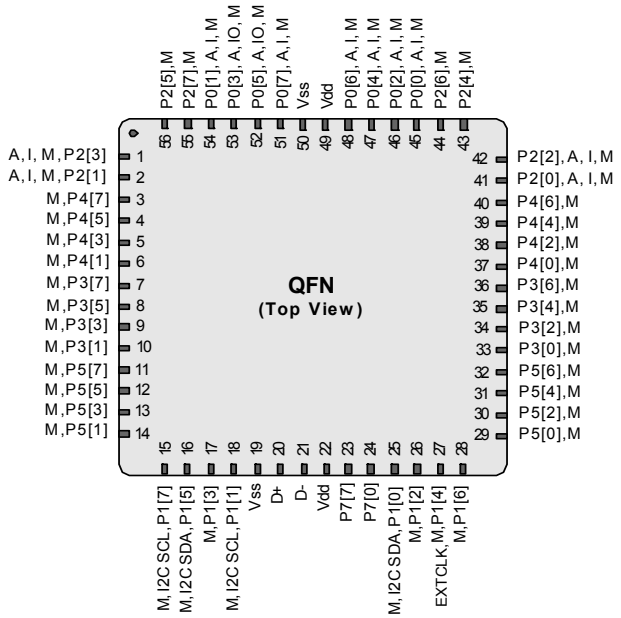
Note CY8C24794 must use Power Cycle programming when using the MiniProg.

7.1 56-Pin Part Pinout

Table 7-1. 56-Pin Part Pinout (QFN[2]) See LEGEND details and footnotes in Table 7-2 **on page 9**.

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.
2	I/O	I, M	P2[1]	Direct switched capacitor block input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I2C Serial Clock (SCL).
16	I/O	M	P1[5]	I2C Serial Data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK[1].
19	Power		Vss	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		Vdd	Supply voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA[1].
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	I/O	M	P3[6]	
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input.
42	I/O	I, M	P2[2]	Direct switched capacitor block input.
43	I/O	M	P2[4]	External Analog Ground (AGND) input.
44	I/O	M	P2[6]	External Voltage Reference (VREF) input.
45	I/O	I, M	P0[0]	Analog column mux input.
46	I/O	I, M	P0[2]	Analog column mux input.
47	I/O	I, M	P0[4]	Analog column mux input VREF.
48	I/O	I, M	P0[6]	Analog column mux input.
49	Power		Vdd	Supply voltage.
50	Power		Vss	Ground connectI/On.
51	I/O	I, M	P0[7]	Analog column mux input,.
52	I/O	I/O, M	P0[5]	Analog column mux input and column output.
53	I/O	I/O, M	P0[3]	Analog column mux input and column output.
54	I/O	I, M	P0[1]	Analog column mux input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

Figure 7-1. CY8C24794 56-Pin PSoC Device



7.4 68-Pin Part Pinout (On-Chip Debug)

The following 68-pin QFN part table and drawing is for the CY8C24094 On-Chip Debug (OCD) PSoC device.

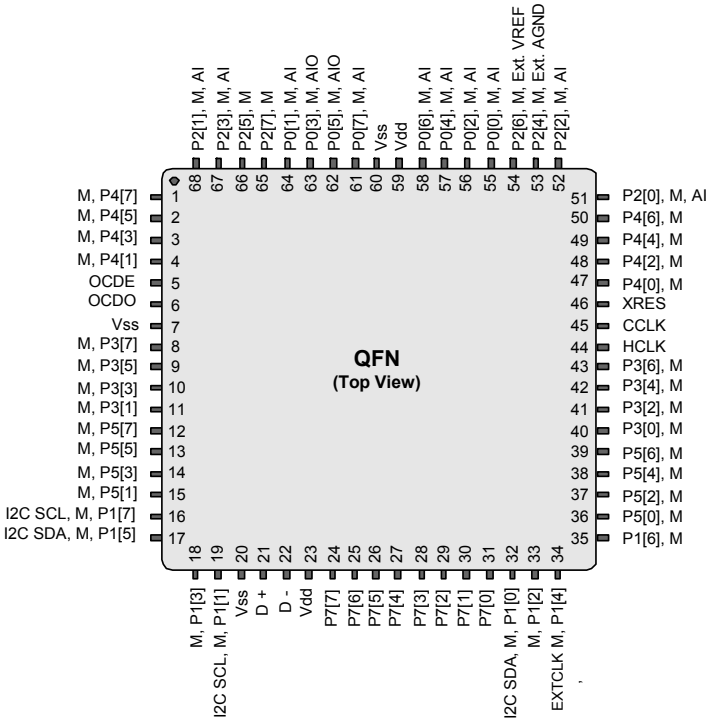
Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7-4. 68-Pin Part Pinout (QFN[2])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			OCDE	OCD even data I/O.
6			OCDO	OCD odd data output.
7	Power		Vss	Ground connection.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I2C Serial Clock (SCL).
17	I/O	M	P1[5]	I2C Serial Data (SDA).
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK[1].
20	Power		Vss	Ground connection.
21	USB		D+	
22	USB		D-	
23	Power		Vdd	Supply voltage.
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA[1].
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			HCLK	OCD high speed clock output.
45			CCLK	OCD CPU clock output.
46	Input		XRES	Active high pin reset with internal pull down.
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I,M	P2[0]	Direct switched capacitor block input.
52	I/O	I,M	P2[2]	Direct switched capacitor block input.
53	I/O	M	P2[4]	External Analog Ground (AGND) input.
54	I/O	M	P2[6]	External Voltage Reference (VREF) input.
55	I/O	I,M	P0[0]	Analog column mux input.
56	I/O	I,M	P0[2]	Analog column mux input and column output.
57	I/O	I,M	P0[4]	Analog column mux input and column output.
58	I/O	I,M	P0[6]	Analog column mux input.
59	Power		Vdd	Supply voltage.
60	Power		Vss	Ground connection.
61	I/O	I,M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O,M	P0[5]	Analog column mux input and column output, integration input #2.
63	I/O	I/O,M	P0[3]	Analog column mux input and column output.
64	I/O	I,M	P0[1]	Analog column mux input.
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I,M	P2[3]	Direct switched capacitor block input.
68	I/O	I,M	P2[1]	Direct switched capacitor block input.

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7-4. CY8C24094 68-Pin OCD PSoC Device



7.5 100-Ball VFBGA Part Pinout

The 100-ball VFBGA part is for the CY8C24994 PSoC device.

Table 7-5. 100-Ball Part Pinout (VFBGA)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
A1	Power		Vss	Ground connection.	F1			NC	No connection.
A2	Power		Vss	Ground connection.	F2	I/O	M	P5[7]	
A3			NC	No connection.	F3	I/O	M	P3[5]	
A4			NC	No connection.	F4	I/O	M	P5[1]	
A5			NC	No connection.	F5	Power		Vss	Ground connection.
A6	Power		Vdd	Supply voltage.	F6	Power		Vss	Ground connection.
A7			NC	No connection.	F7	I/O	M	P5[0]	
A8			NC	No connection.	F8	I/O	M	P3[0]	
A9	Power		Vss	Ground connection.	F9			XRES	Active high pin reset with internal pull down.
A10	Power		Vss	Ground connection.	F10	I/O		P7[1]	
B1	Power		Vss	Ground connection.	G1			NC	No connection.
B2	Power		Vss	Ground connection.	G2	I/O	M	P5[5]	
B3	I/O	I,M	P2[1]	Direct switched capacitor block input.	G3	I/O	M	P3[3]	
B4	I/O	I,M	P0[1]	Analog column mux input.	G4	I/O	M	P1[7]	I2C Serial Clock (SCL).
B5	I/O	I,M	P0[7]	Analog column mux input.	G5	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK[1].
B6	Power		Vdd	Supply voltage.	G6	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA[1].
B7	I/O	I,M	P0[2]	Analog column mux input.	G7	I/O	M	P1[6]	
B8	I/O	I,M	P2[2]	Direct switched capacitor block input.	G8	I/O	M	P3[4]	
B9	Power		Vss	Ground connection.	G9	I/O	M	P5[6]	
B10	Power		Vss	Ground connection.	G10	I/O		P7[2]	
C1			NC	No connection.	H1			NC	No connection.
C2	I/O	M	P4[1]		H2	I/O	M	P5[3]	
C3	I/O	M	P4[7]		H3	I/O	M	P3[1]	
C4	I/O	M	P2[7]		H4	I/O	M	P1[5]	I2C Serial Data (SDA).
C5	I/O	I/O,M	P0[5]	Analog column mux input and column output.	H5	I/O	M	P1[3]	
C6	I/O	I,M	P0[6]	Analog column mux input.	H6	I/O	M	P1[2]	
C7	I/O	I,M	P0[0]	Analog column mux input.	H7	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
C8	I/O	I,M	P2[0]	Direct switched capacitor block input.	H8	I/O	M	P3[2]	
C9	I/O	M	P4[2]		H9	I/O	M	P5[4]	
C10			NC	No connection.	H10	I/O		P7[3]	
D1			NC	No connection.	J1	Power		Vss	Ground connection.
D2	I/O	M	P3[7]		J2	Power		Vss	Ground connection.
D3	I/O	M	P4[5]		J3	USB		D+	
D4	I/O	M	P2[5]		J4	USB		D-	
D5	I/O	I/O,M	P0[3]	Analog column mux input and column output.	J5	Power		Vdd	Supply voltage.
D6	I/O	I,M	P0[4]	Analog column mux input.	J6	I/O		P7[7]	
D7	I/O	M	P2[6]	External Voltage Reference (VREF) input.	J7	I/O		P7[0]	
D8	I/O	M	P4[6]		J8	I/O	M	P5[2]	
D9	I/O	M	P4[0]		J9	Power		Vss	Ground connection.
D10			NC	No connection.	J10	Power		Vss	Ground connection.
E1			NC	No connection.	K1	Power		Vss	Ground connection.
E2			NC	No connection.	K2	Power		Vss	Ground connection.
E3	I/O	M	P4[3]		K3			NC	No connection.
E4	I/O	I,M	P2[3]	Direct switched capacitor block input.	K4			NC	No connection.
E5	Power		Vss	Ground connection.	K5	Power		Vdd	Supply voltage.
E6	Power		Vss	Ground connection.	K6	I/O		P7[6]	
E7	I/O	M	P2[4]	External Analog Ground (AGND) input.	K7	I/O		P7[5]	
E8	I/O	M	P4[4]		K8	I/O		P7[4]	
E9	I/O	M	P3[6]		K9	Power		Vss	Ground connection.
E10			NC	No connection.	K10	Power		Vss	Ground connection.

LEGENDA = Analog, I = Input, O = Output, M = Analog Mux Input, NC = No Connection.

7.7 100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C24094 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7-7. 100-Pin Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No connection.	51	I/O	M	P1[6]	
2			NC	No connection.	52	I/O	M	P5[0]	
3	I/O	I, M	P0[1]	Analog column mux input.	53	I/O	M	P5[2]	
4	I/O	M	P2[7]		54	I/O	M	P5[4]	
5	I/O	M	P2[5]		55	I/O	M	P5[6]	
6	I/O	I, M	P2[3]	Direct switched capacitor block input.	56	I/O	M	P3[0]	
7	I/O	I, M	P2[1]	Direct switched capacitor block input.	57	I/O	M	P3[2]	
8	I/O	M	P4[7]		58	I/O	M	P3[4]	
9	I/O	M	P4[5]		59	I/O	M	P3[6]	
10	I/O	M	P4[3]		60			HCLK	OCD high speed clock output.
11	I/O	M	P4[1]		61			CCLK	OCD CPU clock output.
12			OCDE	OCD even data I/O.	62	Input		XRES	Active high pin reset with internal pull down.
13			OCDO	OCD odd data output.	63	I/O	M	P4[0]	
14			NC	No connection.	64	I/O	M	P4[2]	
15	Power		Vss	Ground connection.	65	Power		Vss	Ground connection.
16	I/O	M	P3[7]		66	I/O	M	P4[4]	
17	I/O	M	P3[5]		67	I/O	M	P4[6]	
18	I/O	M	P3[3]		68	I/O	I, M	P2[0]	Direct switched capacitor block input.
19	I/O	M	P3[1]		69	I/O	I, M	P2[2]	Direct switched capacitor block input.
20	I/O	M	P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input.
21	I/O	M	P5[5]		71			NC	No connection.
22	I/O	M	P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input.
23	I/O	M	P5[1]		73			NC	No connection.
24	I/O	M	P1[7]	I2C Serial Clock (SCL).	74	I/O	I	P0[0]	Analog column mux input.
25			NC	No connection.	75			NC	No connection.
26			NC	No connection.	76			NC	No connection.
27			NC	No connection.	77	I/O	I, M	P0[2]	Analog column mux input and column output.
28	I/O		P1[5]	I2C Serial Data (SDA)	78			NC	No connection.
29	I/O		P1[3]		79	I/O	I, M	P0[4]	Analog column mux input and column output.
30	I/O		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP SCLK[1].	80			NC	No connection.
31			NC	No connection.	81	I/O	I, M	P0[6]	Analog column mux input.
32	Power		Vss	Ground connection.	82	Power		Vdd	Supply voltage.
33	USB		D+		83			NC	No connection.
34	USB		D-		84	Power		Vss	Ground connection.
35	Power		Vdd	Supply voltage.	85			NC	No connection.
36	I/O		P7[7]		86			NC	No connection.
37	I/O		P7[6]		87			NC	No connection.
38	I/O		P7[5]		88			NC	No connection.
39	I/O		P7[4]		89			NC	No connection.
40	I/O		P7[3]		90			NC	No connection.
41	I/O		P7[2]		91			NC	No connection.
42	I/O		P7[1]		92			NC	No connection.
43	I/O		P7[0]		93			NC	No connection.
44			NC	No connection.	94			NC	No connection.
45			NC	No connection.	95	I/O	I, M	P0[7]	Analog column mux input.
46			NC	No connection.	96			NC	No connection.
47			NC	No connection.	97	I/O	I/O, M	P0[5]	Analog column mux input and column output.
48	I/O		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP SDATA[1].	98			NC	No connection.
49	I/O		P1[2]		99	I/O	I/O, M	P0[3]	Analog column mux input and column output.
50	I/O		P1[4]	Optional External Clock Input (EXTCLK).	100			NC	No connection.

8. Register Reference

This section lists the registers of the CY8C24x94 PSoC device family. For detailed register information, reference the *PSoC Programmable System-on-Chip Technical Reference Manual*.

8.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

8.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

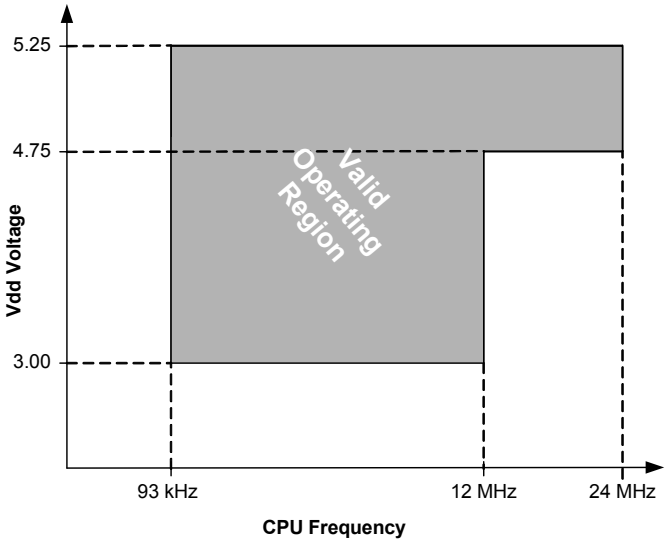
Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

9. Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C24x94 PSoC device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted. Specifications for devices running at greater than 12 MHz are valid for -40°C ≤ T_A ≤ 70°C and T_J ≤ 82°C.

Figure 9-1. Voltage versus CPU Frequency



The following table lists the units of measure that are used in this chapter.

Table 9-1. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Table 9-7. 5V DC Operational Amplifier Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

9.3.5 DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 9-8. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

9.3.6 DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-9. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x Vdd - 1.3) ≤ V_{OUT} ≤ (Vdd - 2.3).

Table 9-10. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 W W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	– –	– –	V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	(0.5 x Vdd - 1.0) ≤ V_{OUT} ≤ (0.5 x Vdd + 0.9).

Table 9-12. 3.3V DC Analog Reference Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units
–	RefHi = 3.2 x BandGap		Not Allowed		
–	RefLo = Vdd/2 - BandGap		Not Allowed		
–	RefLo = BandGap		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

9.3.8 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-13. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

Note
4. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.
5. Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

9.4 AC Electrical Characteristics

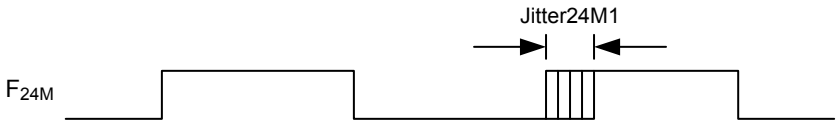
9.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-16. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[9,10]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[10,11]	MHz	Trimmed for 3.3V operation using factory trim values.
$F_{IMOUSB5V}$	Internal Main Oscillator Frequency with USB (5V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[10]	MHz	-10°C ≤ T_A ≤ 85°C 4.35 ≤ Vdd ≤ 5.15
$F_{IMOUSB3V}$	Internal Main Oscillator Frequency with USB (3.3V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[10]	MHz	-0°C ≤ T_A ≤ 70°C 3.15 ≤ Vdd ≤ 3.45
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[9,10]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[10,11]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[9,10,12]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[10,12]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[9,11]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Figure 9-2. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
9. 4.75V < Vdd < 5.25V.
10. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
11. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
12. See the individual user module data sheets for information on maximum frequencies for user modules

9.4.4 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 9-19. 5V AC Operational Amplifier Specifications

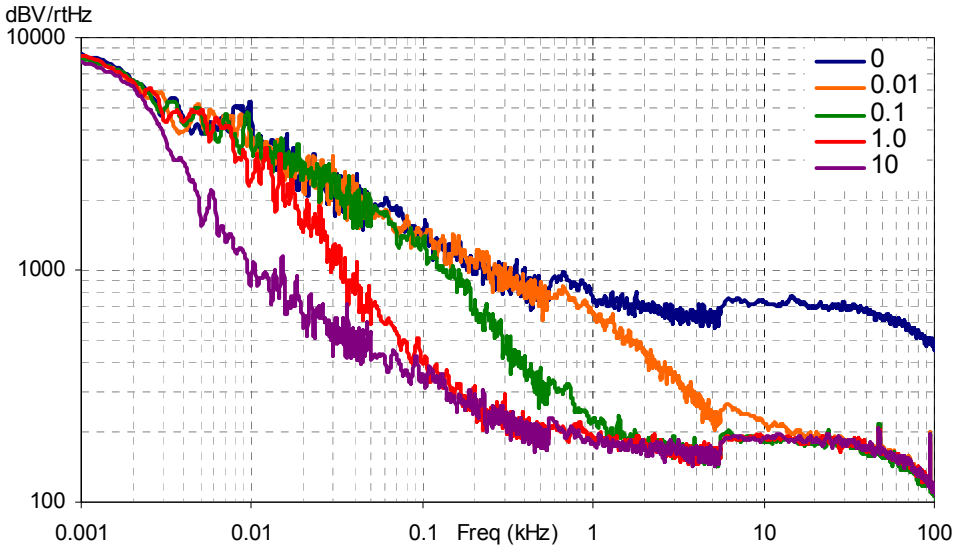
Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 9-20. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

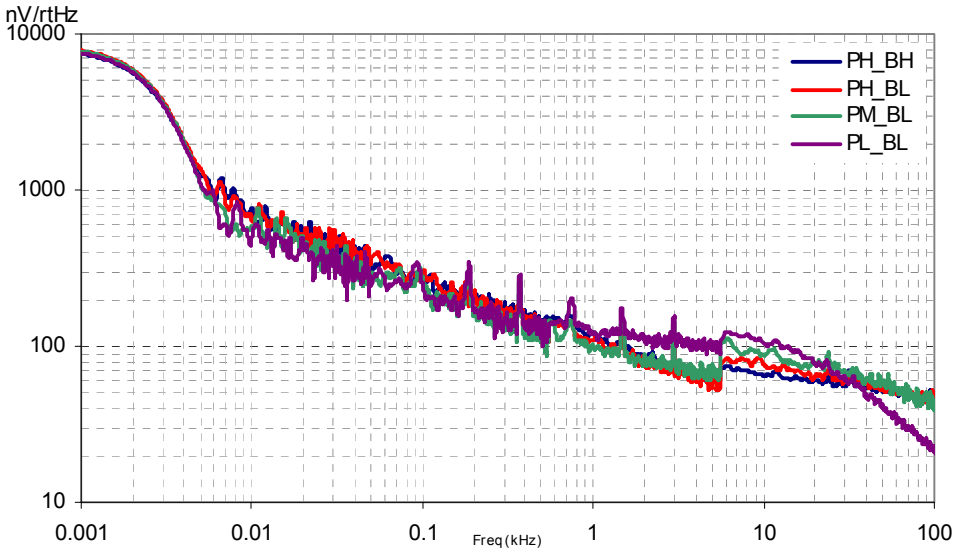
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1k resistance and the external capacitor.

Figure 9-4. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 9-5. Typical Opamp Noise

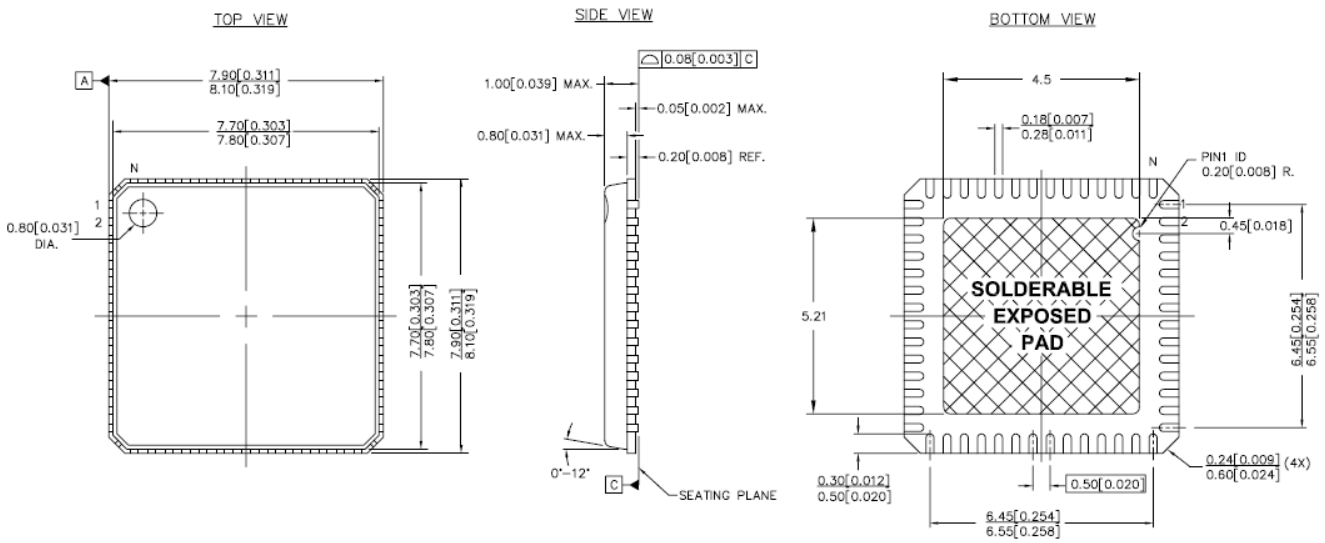


10. Packaging Dimensions

This section illustrates the package specification for the CY8C24x94 PSoC devices, along with the thermal impedance for the package and solder reflow peak temperatures.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

Figure 10-1. 56-Pin (8x8 mm) QFN



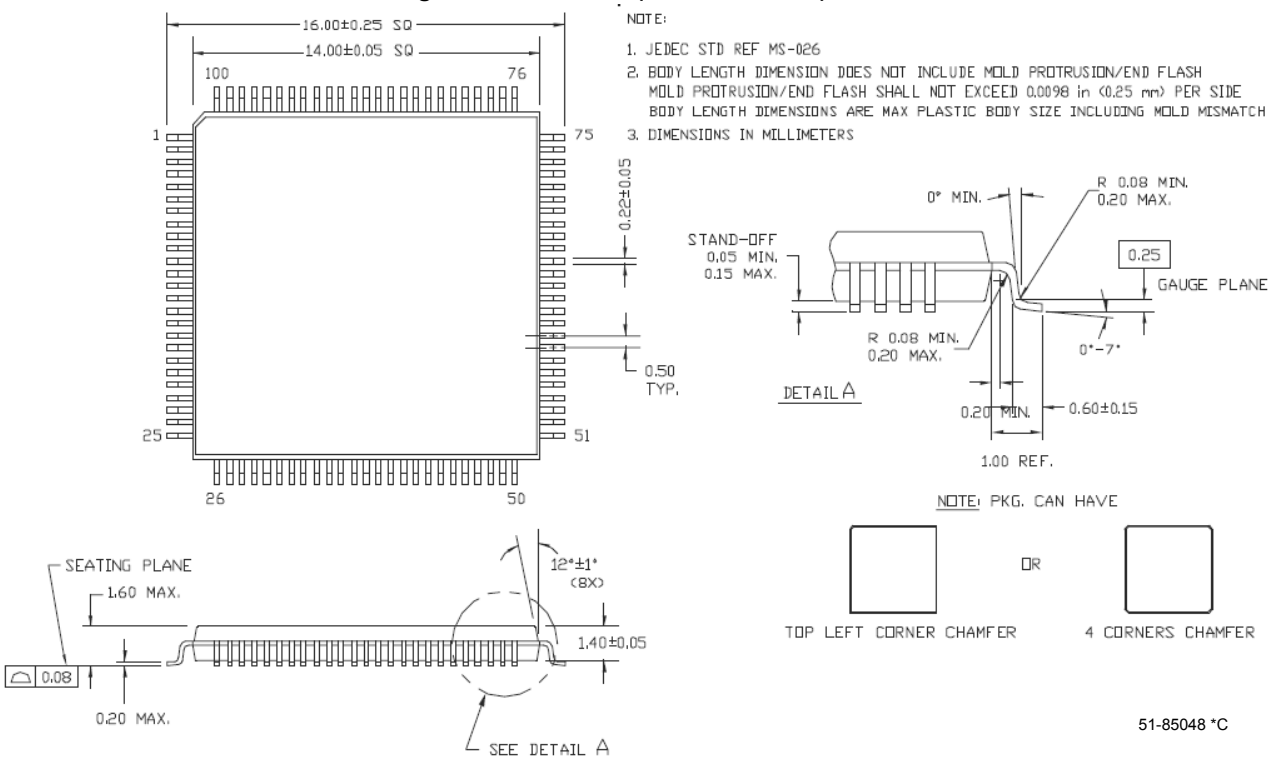
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF56A	STANDARD
LY56A	PB-FREE

001-12921 **

Figure 10-6. 100-Pin (14x14 x 1.4 mm) TQFP



10.1 Thermal Impedance

Table 10-1. Thermal Impedance for the Package

Package	Typical θ_{JA} [15]
56 QFN[16]	12.93 °C/W
68 QFN[16]	13.05 °C/W
100 VFBGA	65 °C/W
100 TQFP	51 °C/W

10.2 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 10-2. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[17]	Maximum Peak Temperature
56 QFN	240°C	260°C
68 QFN	240°C	260°C
100 VFBGA	240°C	260°C

Notes
15. $T_J = T_A + POWER \times \theta_{JA}$
16. To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.
17. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5°C with Sn-Pb or 245 ± 5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

11. Development Tool Selection

11.1 Software

11.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

11.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

11.2 Development Kits

All development kits can be purchased from the Cypress Online Store.

11.2.1 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

11.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

11.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit enables a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

11.4 Device Programmers

All device programmers can be purchased from the Cypress Online Store.

11.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

11.5 Accessories (Emulation and Programming)

Table 11-1. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[18]	Foot Kit[19]	Adapter[20]
CY8C24794-24LFXI	56 QFN	CY3250-24X94QFN	CY3250-56QFN-FK	AS-56-28
CY8C24894-24LFXI	56 QFN	CY3250-24X94QFN	CY3250-56QFN-FK	AS-28-28-02SS-6ENG-GANG

11.5.1 3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools are found at http://www.cypress.com under Design Resources > Evaluation Boards.

11.5.2 Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/an2323.

Notes
18. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
19. Foot kit includes surface mount feet that are soldered to the target PCB.
20. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at http://www.emulation.com.

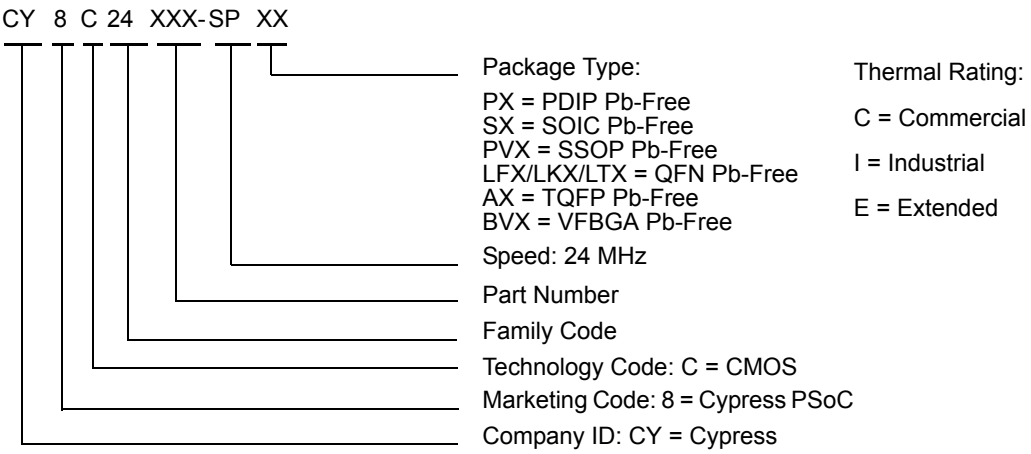
12. Ordering Information

Table 12-1. CY8C24x94 PSoC Device's Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
56-Pin (8x8 mm) QFN (Sawn)	CY8C24794-24LTXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN (Sawn) (Tape and Reel)	CY8C24794-24LTXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LTXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LTXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24794-24LFXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8C24794-24LFXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LFXI	16K	1K	-40°C to +85°C	4	6	49	47	2	Yes
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8C24894-24LFXIT	16K	1K	-40°C to +85°C	4	6	49	47	2	Yes
68 Pin OCD (8x8 mm) QFN[21]	CY8C24094-24LFXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68 Pin (8x8 mm) QFN	CY8C24994-24LFXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68 Pin (8x8 mm) QFN (Tape and Reel)	CY8C24994-24LFXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24994-24LTXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24994-24LTXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100-Ball OCD (6x6 mm) VFBGA[21]	CY8C24094-24BVXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100-Ball (6x6 mm) VFBGA	CY8C24994-24BVXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100 Pin OCD TQFP[21]	CY8C24094-24AXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24094-24LTXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24094-24LTXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

12.1 Ordering Code Definitions



Note
21. This part may be used for in-circuit debugging. It is NOT available for production.

Sales, Solutions, and Legal Information

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