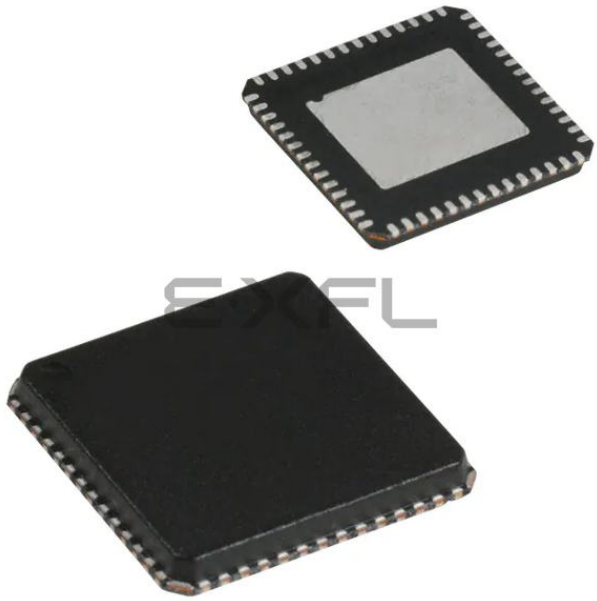

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	POR, PWM, WDT
Number of I/O	49
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 48x14b; D/A 2x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c24894-24lfxit

2. PSoC Functional Overview

The PSoC family consists of many programmable system-on-chips with On-Chip Controller devices. All PSoC family devices are designed to replace traditional MCUs, system ICs, and the numerous discrete components that surround them. The PSoC CY8C24x94 devices are unique members of the PSoC family because it includes a full featured, full speed (12 Mbps) USB port. Configurable analog, digital, and interconnect circuitry enable a high level of integration in a host of industrial, consumer, and communication applications.

This architecture enables the user to create customized peripheral configurations that match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts and packages.

The PSoC architecture, as illustrated on the left, is comprised of four main areas: PSoC Core, Digital System, Analog System, and System Resources including a full speed USB port. Configurable global busing enables all the device resources to be combined into a complete custom system. The PSoC CY8C24x94 devices can have up to seven I/O ports that connect to the global digital and analog interconnects, providing access to 4 digital blocks and 6 analog blocks.

2.1 The PSoC Core

The PSoC Core is a powerful engine that supports a rich feature set. The core includes a CPU, memory, clocks, and configurable GPI/O (General Purpose I/O).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

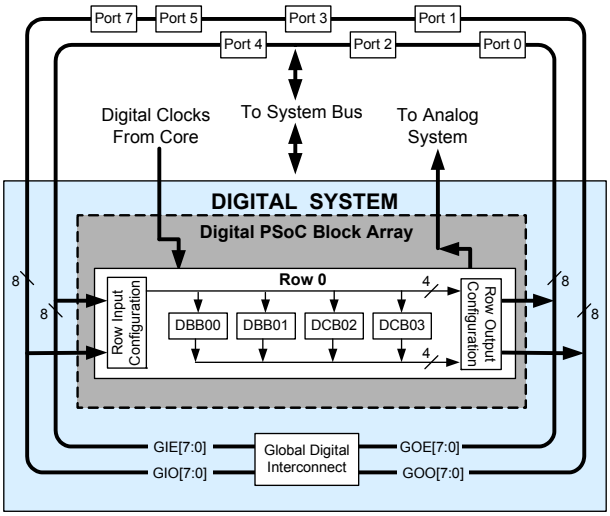
The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 8% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device. In USB systems, the IMO self tunes to ± 0.25% accuracy for USB communication.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin is also capable of generating a system interrupt on high level, low level, and change from last read.

2.2 The Digital System

The Digital System is composed of four digital PSoC blocks. Each block is an 8-bit resource used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 2-1. Digital System Block Diagram



Digital peripheral configurations include the following:

- Full Speed USB (12 Mbps)
- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPI/O through a series of global buses that can route any signal to any pin. The buses also enable signal multiplexing and performing logic operations. This configurability frees the designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This enables you the optimum choice of system resources for your application. Family resources are shown in Table 2-1 on page 4.

2.4 Additional System Resources

System Resources, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Full Speed USB (12 Mbps) with 5 configurable endpoints and 256 bytes of RAM. No external components required except two series resistors. Wider than commercial temperature USB operation (-10°C to +85°C).
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications including creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, multi-master are supported.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

2.5 PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific PSoC device groups. The device covered by this data sheet is shown in the highlighted row of the table

Table 2-1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	12	4	4	12	2K	32K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	56	1	4	48	2	2	6	1K	16K
CY8C24x23A	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C21x34	up to 28	1	4	28	0	2	4	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3	512 Bytes	8K

3. Getting Started

The quickest way to understand PSoC silicon is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming information, see the PSoC® Programmable System-on-Chip Technical Reference Manual for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

3.1 Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

3.2 Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

3.3 Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

3.4 CyPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

3.5 Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

3.6 Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

4. Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

4.1 PSoC Designer Software Subsystems

4.1.1 System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

4.1.2 Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration enables changing configurations at run time.

4.1.3 Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

4.1.4 Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

4.1.5 Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

4.1.6 Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

4.2 In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

5. Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

5.1 Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

5.2 Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

5.3 Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the I/O pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

5.4 Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

6. Document Conventions

6.1 Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPI/O	general purpose I/O
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

6.2 Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 9-1 on page 20 lists all the abbreviations used to measure the PSoC devices.

6.3 Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (e.g., 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimal.

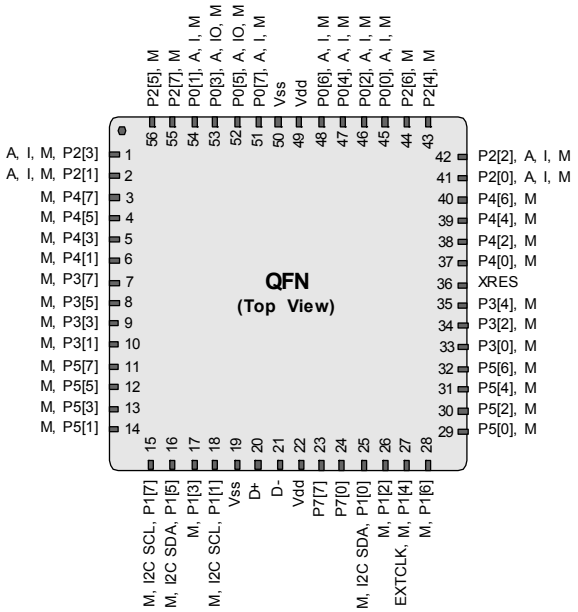
7.2 56-Pin Part Pinout (with XRES)

Table 7-2. 56-Pin Part Pinout (QFN[2])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P2[3]	Direct switched capacitor block input.
2	I/O	I, M	P2[1]	Direct switched capacitor block input.
3	I/O	M	P4[7]	
4	I/O	M	P4[5]	
5	I/O	M	P4[3]	
6	I/O	M	P4[1]	
7	I/O	M	P3[7]	
8	I/O	M	P3[5]	
9	I/O	M	P3[3]	
10	I/O	M	P3[1]	
11	I/O	M	P5[7]	
12	I/O	M	P5[5]	
13	I/O	M	P5[3]	
14	I/O	M	P5[1]	
15	I/O	M	P1[7]	I2C Serial Clock (SCL).
16	I/O	M	P1[5]	I2C Serial Data (SDA).
17	I/O	M	P1[3]	
18	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK[1].
19	Power		Vss	Ground connection.
20	USB		D+	
21	USB		D-	
22	Power		Vdd	Supply voltage.
23	I/O		P7[7]	
24	I/O		P7[0]	
25	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA[1].
26	I/O	M	P1[2]	
27	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
28	I/O	M	P1[6]	
29	I/O	M	P5[0]	
30	I/O	M	P5[2]	
31	I/O	M	P5[4]	
32	I/O	M	P5[6]	
33	I/O	M	P3[0]	
34	I/O	M	P3[2]	
35	I/O	M	P3[4]	
36	Input		XRES	Active high external reset with internal pull down.
37	I/O	M	P4[0]	
38	I/O	M	P4[2]	
39	I/O	M	P4[4]	
40	I/O	M	P4[6]	
41	I/O	I, M	P2[0]	Direct switched capacitor block input.
42	I/O	I, M	P2[2]	Direct switched capacitor block input.
43	I/O	M	P2[4]	External Analog Ground (AGND) input.
44	I/O	M	P2[6]	External Voltage Reference (VREF) input.
45	I/O	I, M	P0[0]	Analog column mux input.
46	I/O	I, M	P0[2]	Analog column mux input.
47	I/O	I, M	P0[4]	Analog column mux input VREF.
48	I/O	I, M	P0[6]	Analog column mux input.
49	Power		Vdd	Supply voltage.
50	Power		Vss	Ground connection.
51	I/O	I, M	P0[7]	Analog column mux input,.
52	I/O	I/O, M	P0[5]	Analog column mux input and column output.
53	I/O	I/O, M	P0[3]	Analog column mux input and column output.
54	I/O	I, M	P0[1]	Analog column mux input.
55	I/O	M	P2[7]	
56	I/O	M	P2[5]	

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 7-2. CY8C24894 56-Pin PSoC Device



Notes
1. These are the ISSP pins, which are not High Z at POR. See the PSoC Programmable System-on-Chip Technical Reference Manual for details.
2. The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

7.4 68-Pin Part Pinout (On-Chip Debug)

The following 68-pin QFN part table and drawing is for the CY8C24094 On-Chip Debug (OCD) PSoC device.

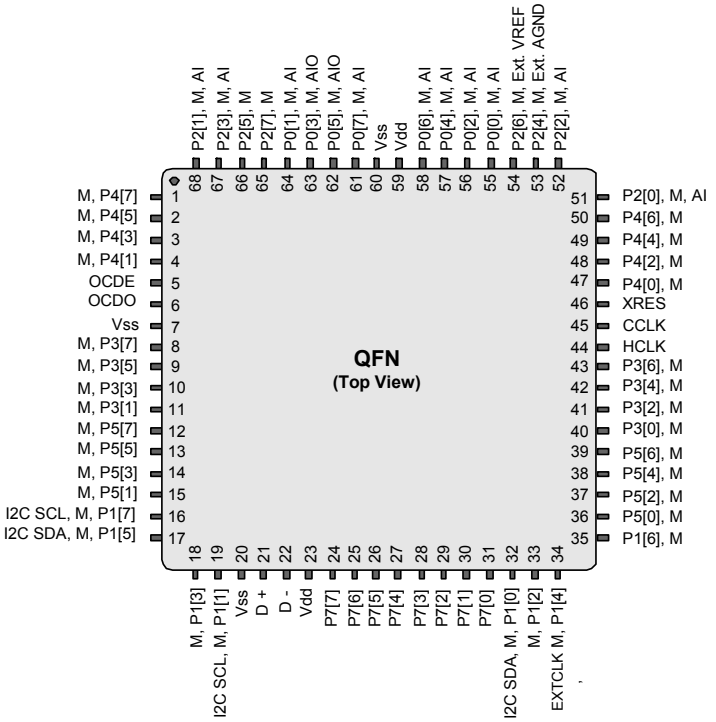
Note This part is only used for in-circuit debugging. It is NOT available for production.

Table 7-4. 68-Pin Part Pinout (QFN[2])

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	M	P4[7]	
2	I/O	M	P4[5]	
3	I/O	M	P4[3]	
4	I/O	M	P4[1]	
5			OCDE	OCD even data I/O.
6			OCDO	OCD odd data output.
7	Power		Vss	Ground connection.
8	I/O	M	P3[7]	
9	I/O	M	P3[5]	
10	I/O	M	P3[3]	
11	I/O	M	P3[1]	
12	I/O	M	P5[7]	
13	I/O	M	P5[5]	
14	I/O	M	P5[3]	
15	I/O	M	P5[1]	
16	I/O	M	P1[7]	I2C Serial Clock (SCL).
17	I/O	M	P1[5]	I2C Serial Data (SDA).
18	I/O	M	P1[3]	
19	I/O	M	P1[1]	I2C Serial Clock (SCL), ISSP SCLK[1].
20	Power		Vss	Ground connection.
21	USB		D+	
22	USB		D-	
23	Power		Vdd	Supply voltage.
24	I/O		P7[7]	
25	I/O		P7[6]	
26	I/O		P7[5]	
27	I/O		P7[4]	
28	I/O		P7[3]	
29	I/O		P7[2]	
30	I/O		P7[1]	
31	I/O		P7[0]	
32	I/O	M	P1[0]	I2C Serial Data (SDA), ISSP SDATA[1].
33	I/O	M	P1[2]	
34	I/O	M	P1[4]	Optional External Clock Input (EXTCLK).
35	I/O	M	P1[6]	
36	I/O	M	P5[0]	
37	I/O	M	P5[2]	
38	I/O	M	P5[4]	
39	I/O	M	P5[6]	
40	I/O	M	P3[0]	
41	I/O	M	P3[2]	
42	I/O	M	P3[4]	
43	I/O	M	P3[6]	
44			HCLK	OCD high speed clock output.
45			CCLK	OCD CPU clock output.
46	Input		XRES	Active high pin reset with internal pull down.
47	I/O	M	P4[0]	
48	I/O	M	P4[2]	
49	I/O	M	P4[4]	
50	I/O	M	P4[6]	
51	I/O	I,M	P2[0]	Direct switched capacitor block input.
52	I/O	I,M	P2[2]	Direct switched capacitor block input.
53	I/O	M	P2[4]	External Analog Ground (AGND) input.
54	I/O	M	P2[6]	External Voltage Reference (VREF) input.
55	I/O	I,M	P0[0]	Analog column mux input.
56	I/O	I,M	P0[2]	Analog column mux input and column output.
57	I/O	I,M	P0[4]	Analog column mux input and column output.
58	I/O	I,M	P0[6]	Analog column mux input.
59	Power		Vdd	Supply voltage.
60	Power		Vss	Ground connection.
61	I/O	I,M	P0[7]	Analog column mux input, integration input #1
62	I/O	I/O,M	P0[5]	Analog column mux input and column output, integration input #2.
63	I/O	I/O,M	P0[3]	Analog column mux input and column output.
64	I/O	I,M	P0[1]	Analog column mux input.
65	I/O	M	P2[7]	
66	I/O	M	P2[5]	
67	I/O	I,M	P2[3]	Direct switched capacitor block input.
68	I/O	I,M	P2[1]	Direct switched capacitor block input.

LEGEND A = Analog, I = Input, O = Output, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7-4. CY8C24094 68-Pin OCD PSoC Device



7.7 100-Pin Part Pinout (On-Chip Debug)

The 100-pin TQFP part is for the CY8C24094 On-Chip Debug (OCD) PSoC device.

Note This part is only used for in-circuit debugging. It is NOT available for production.

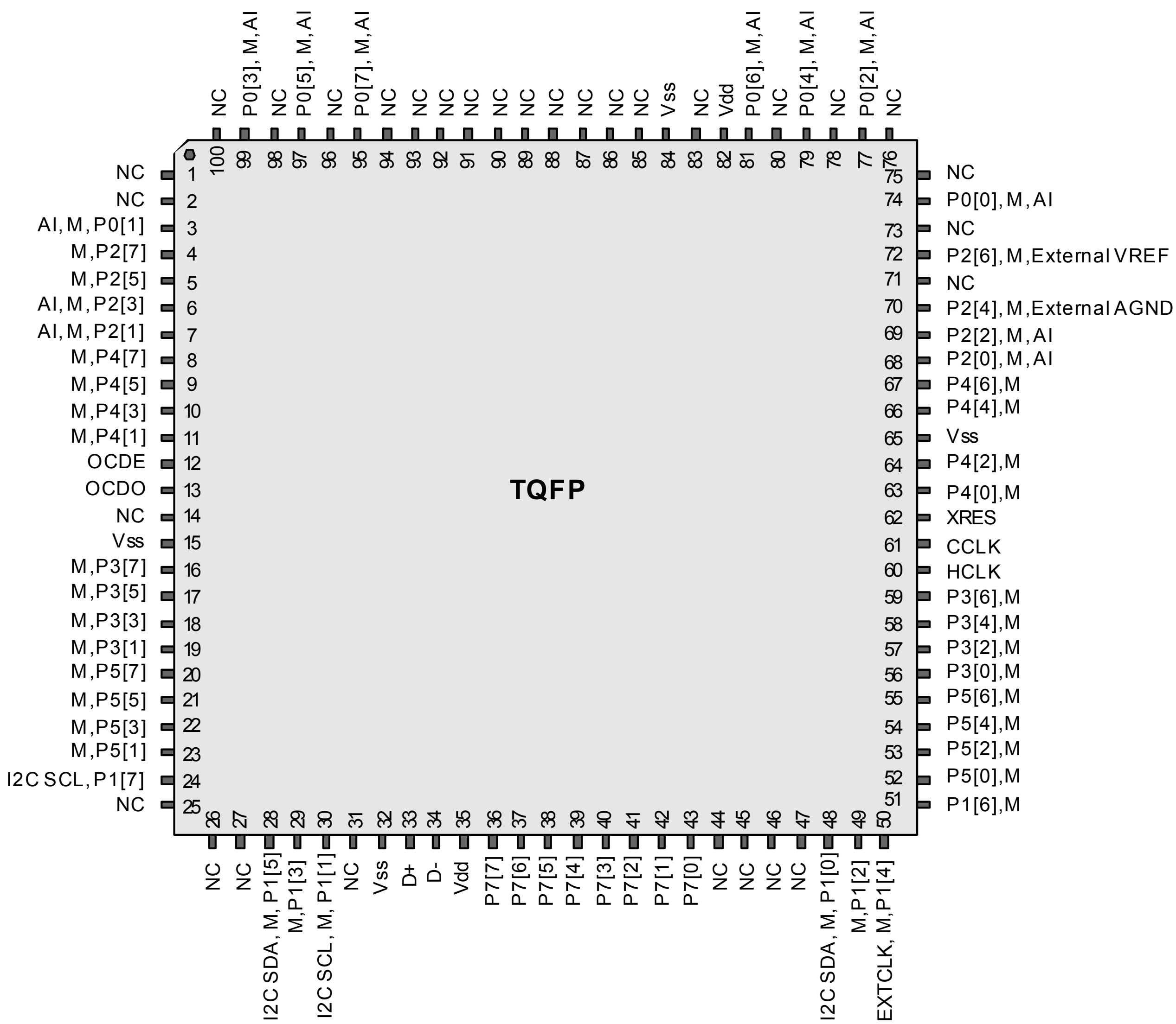
Table 7-7. 100-Pin Part Pinout (TQFP)

Pin No.	Digital	Analog	Name	Description	Pin No.	Digital	Analog	Name	Description
1			NC	No connection.	51	I/O	M	P1[6]	
2			NC	No connection.	52	I/O	M	P5[0]	
3	I/O	I, M	P0[1]	Analog column mux input.	53	I/O	M	P5[2]	
4	I/O	M	P2[7]		54	I/O	M	P5[4]	
5	I/O	M	P2[5]		55	I/O	M	P5[6]	
6	I/O	I, M	P2[3]	Direct switched capacitor block input.	56	I/O	M	P3[0]	
7	I/O	I, M	P2[1]	Direct switched capacitor block input.	57	I/O	M	P3[2]	
8	I/O	M	P4[7]		58	I/O	M	P3[4]	
9	I/O	M	P4[5]		59	I/O	M	P3[6]	
10	I/O	M	P4[3]		60			HCLK	OCD high speed clock output.
11	I/O	M	P4[1]		61			CCLK	OCD CPU clock output.
12			OCDE	OCD even data I/O.	62	Input		XRES	Active high pin reset with internal pull down.
13			OCDO	OCD odd data output.	63	I/O	M	P4[0]	
14			NC	No connection.	64	I/O	M	P4[2]	
15	Power		Vss	Ground connection.	65	Power		Vss	Ground connection.
16	I/O	M	P3[7]		66	I/O	M	P4[4]	
17	I/O	M	P3[5]		67	I/O	M	P4[6]	
18	I/O	M	P3[3]		68	I/O	I, M	P2[0]	Direct switched capacitor block input.
19	I/O	M	P3[1]		69	I/O	I, M	P2[2]	Direct switched capacitor block input.
20	I/O	M	P5[7]		70	I/O		P2[4]	External Analog Ground (AGND) input.
21	I/O	M	P5[5]		71			NC	No connection.
22	I/O	M	P5[3]		72	I/O		P2[6]	External Voltage Reference (VREF) input.
23	I/O	M	P5[1]		73			NC	No connection.
24	I/O	M	P1[7]	I2C Serial Clock (SCL).	74	I/O	I	P0[0]	Analog column mux input.
25			NC	No connection.	75			NC	No connection.
26			NC	No connection.	76			NC	No connection.
27			NC	No connection.	77	I/O	I, M	P0[2]	Analog column mux input and column output.
28	I/O		P1[5]	I2C Serial Data (SDA)	78			NC	No connection.
29	I/O		P1[3]		79	I/O	I, M	P0[4]	Analog column mux input and column output.
30	I/O		P1[1]	Crystal (XTALin), I2C Serial Clock (SCL), ISSP SCLK[1].	80			NC	No connection.
31			NC	No connection.	81	I/O	I, M	P0[6]	Analog column mux input.
32	Power		Vss	Ground connection.	82	Power		Vdd	Supply voltage.
33	USB		D+		83			NC	No connection.
34	USB		D-		84	Power		Vss	Ground connection.
35	Power		Vdd	Supply voltage.	85			NC	No connection.
36	I/O		P7[7]		86			NC	No connection.
37	I/O		P7[6]		87			NC	No connection.
38	I/O		P7[5]		88			NC	No connection.
39	I/O		P7[4]		89			NC	No connection.
40	I/O		P7[3]		90			NC	No connection.
41	I/O		P7[2]		91			NC	No connection.
42	I/O		P7[1]		92			NC	No connection.
43	I/O		P7[0]		93			NC	No connection.
44			NC	No connection.	94			NC	No connection.
45			NC	No connection.	95	I/O	I, M	P0[7]	Analog column mux input.
46			NC	No connection.	96			NC	No connection.
47			NC	No connection.	97	I/O	I/O, M	P0[5]	Analog column mux input and column output.
48	I/O		P1[0]	Crystal (XTALout), I2C Serial Data (SDA), ISSP SDATA[1].	98			NC	No connection.
49	I/O		P1[2]		99	I/O	I/O, M	P0[3]	Analog column mux input and column output.
50	I/O		P1[4]	Optional External Clock Input (EXTCLK).	100			NC	No connection.

Table 7-7. 100-Pin Part Pinout (TQFP) *(continued)*

LEGENDA = Analog, I = Input, O = Output, NC = No Connection, M = Analog Mux Input, OCD = On-Chip Debugger.

Figure 7-7. CY8C24094 OCD (Not for Production)



[+] Feedback

9.1 Absolute Maximum Ratings

Table 9-2. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
$V_{I/O}$	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
$V_{I/O2}$	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
$I_{MI/O}$	Maximum Current into any Port Pin	-25	–	+50	mA	
$I_{MAI/O}$	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch-up Current	–	–	200	mA	

9.2 Operating Temperature

Table 9-3. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature	-40	–	+85	°C	
T_{AUSB}	Ambient Temperature using USB	-10	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedance on page 41. The user must limit the power consumption to comply with this requirement.

9.3 DC Electrical Characteristics

9.3.1 DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 9-14 on page 28.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[3]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[3]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < T_A ≤ 85 °C, analog power = off.

9.3.2 DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-5. DC GPI/O Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	I/OH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I/OH budget.
V_{OL}	Low Output Level	–	–	0.75	V	I/OL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined I/OL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

Note
3. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

9.3.3 DC Full Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -10°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -10°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-6. DC Full Speed (12 Mbps) USB Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
USB Interface						
V_{DI}	Differential Input Sensitivity	0.2	–	–	V	| (D+) - (D-) |
V_{CM}	Differential Input Common Mode Range	0.8	–	2.5	V	
V_{SE}	Single Ended Receiver Threshold	0.8	–	2.0	V	
C_{IN}	Transceiver Capacitance	–	–	20	pF	
$I_{I/O}$	High-Z State Data Line Leakage	-10	–	10	µA	0V < V_{IN} < 3.3V.
R_{EXT}	External USB Series Resistor	23	–	25	W	In series with each USB pin.
V_{UOH}	Static Output High, Driven	2.8	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
V_{UOHI}	Static Output High, Idle	2.7	–	3.6	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
V_{UOL}	Static Output Low	–	–	0.3	V	15 kΩ ± 5% to Ground. Internal pull up enabled.
Z_O	USB Driver Output Impedance	28	–	44	W	Including R_{EXT} Resistor.
V_{CRS}	D+/D- Crossover Voltage	1.3	–	2.0	V	

9.3.4 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 9-7. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	–	–	dB	

Table 9-12. 3.3V DC Analog Reference Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units
–	RefHi = 3.2 x BandGap		Not Allowed		
–	RefLo = Vdd/2 - BandGap		Not Allowed		
–	RefLo = BandGap		Not Allowed		
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)		Not Allowed		
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)		Not Allowed		
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

9.3.8 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-13. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

Note
4. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.
5. Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

9.4 AC Electrical Characteristics

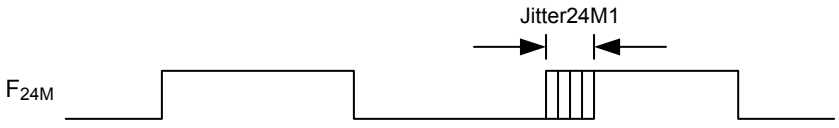
9.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-16. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[9,10]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[10,11]	MHz	Trimmed for 3.3V operation using factory trim values.
$F_{IMOUSB5V}$	Internal Main Oscillator Frequency with USB (5V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[10]	MHz	-10°C ≤ T_A ≤ 85°C 4.35 ≤ Vdd ≤ 5.15
$F_{IMOUSB3V}$	Internal Main Oscillator Frequency with USB (3.3V) Frequency locking enabled and USB traffic present.	23.94	24	24.06[10]	MHz	-0°C ≤ T_A ≤ 70°C 3.15 ≤ Vdd ≤ 3.45
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[9,10]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[10,11]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[9,10,12]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[10,12]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[9,11]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.96	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

Figure 9-2. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
9. 4.75V < Vdd < 5.25V.
10. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
11. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
12. See the individual user module data sheets for information on maximum frequencies for user modules

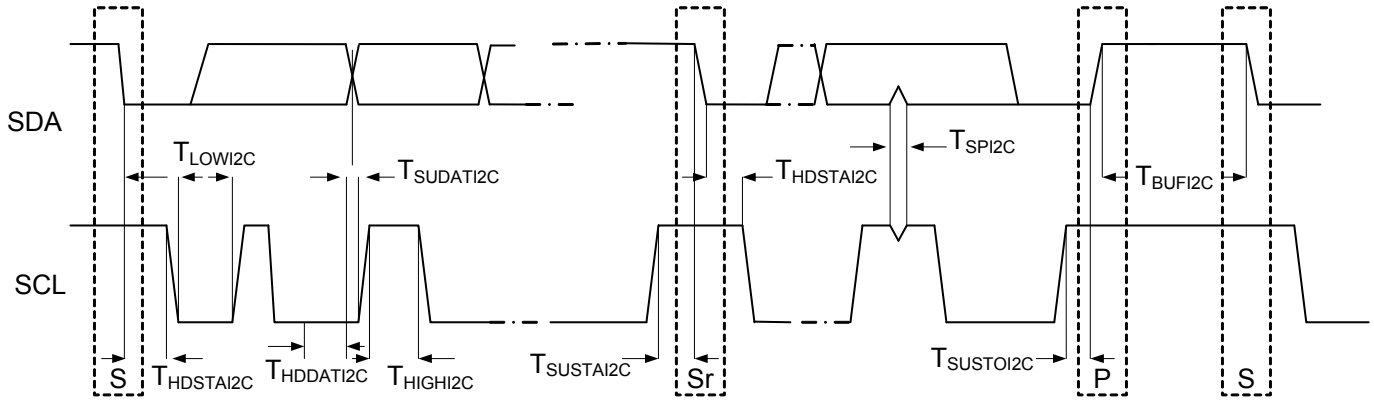
9.4.10 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 9-27. AC Characteristics of the I²C SDA and SCL Pins for Vdd

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[14]	–	ns	
$T_{SUSTOI2C}$	Setup Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 9-6. Definition for Timing for Fast/Standard Mode on the I²C Bus



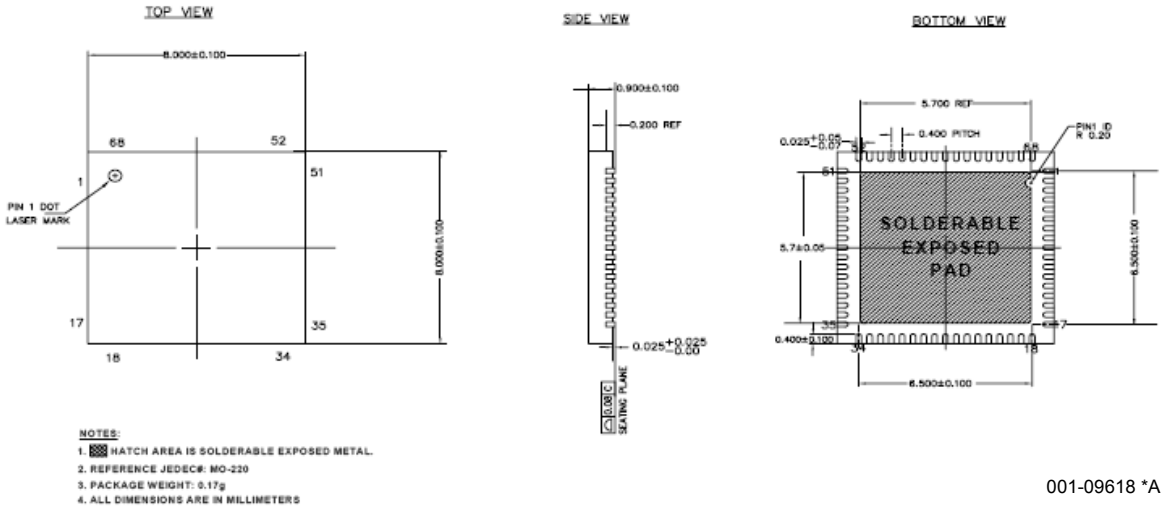
Note

14. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT}$ Š 250 ns must then be met. This automatically is the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Important Note

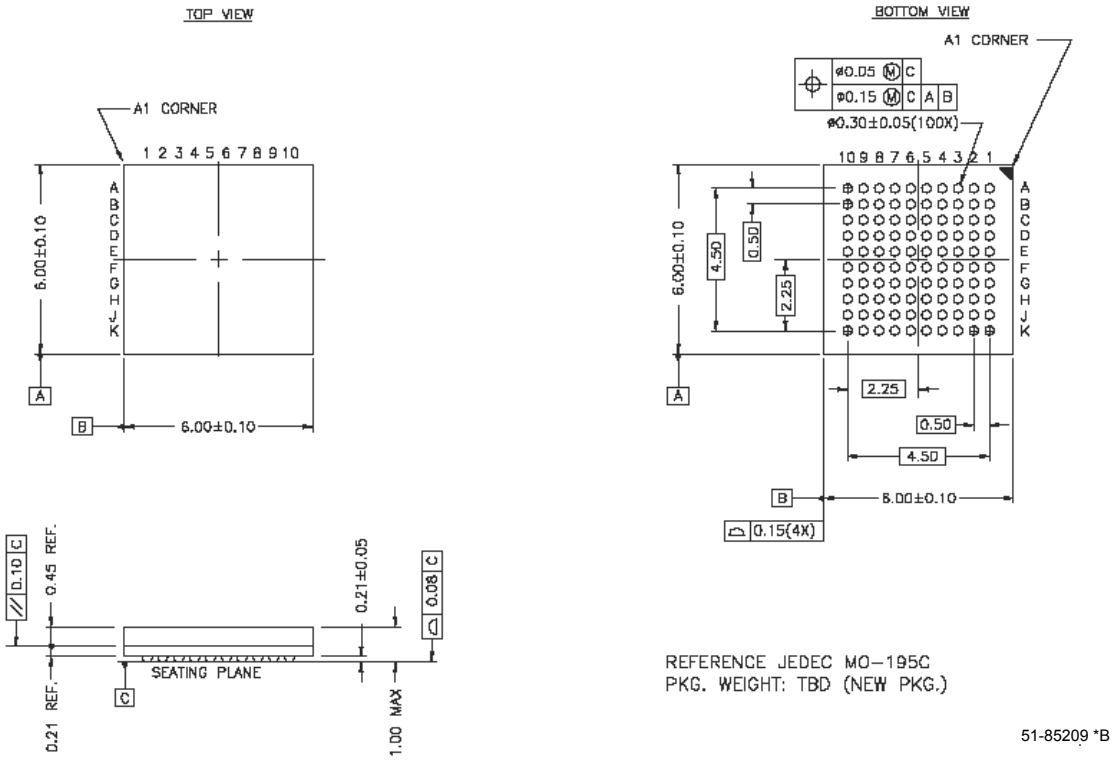
- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low-power PSoC device.

Figure 10-4. 68-Pin SAWN QFN (8X8 mm X 0.90 mm)



001-09618 *A

Figure 10-5. 100-Ball (6x6 mm) VFBGA



51-85209 *B

11. Development Tool Selection

11.1 Software

11.1.1 PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com/psocdesigner and includes a free C compiler.

11.1.2 PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

11.2 Development Kits

All development kits can be purchased from the Cypress Online Store.

11.2.1 CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

11.3 Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

11.3.1 CY3210-MiniProg1

The CY3210-MiniProg1 kit enables a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.2 CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.3.3 CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

11.4 Device Programmers

All device programmers can be purchased from the Cypress Online Store.

11.4.1 CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

11.4.2 CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

11.5 Accessories (Emulation and Programming)

Table 11-1. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[18]	Foot Kit[19]	Adapter[20]
CY8C24794-24LFXI	56 QFN	CY3250-24X94QFN	CY3250-56QFN-FK	AS-56-28
CY8C24894-24LFXI	56 QFN	CY3250-24X94QFN	CY3250-56QFN-FK	AS-28-28-02SS-6ENG-GANG

11.5.1 3rd-Party Tools

Several tools have been specially designed by the following 3rd-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools are found at http://www.cypress.com under Design Resources > Evaluation Boards.

11.5.2 Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, see Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/an2323.

Notes
18. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
19. Foot kit includes surface mount feet that are soldered to the target PCB.
20. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters are found at http://www.emulation.com.

12. Ordering Information

Table 12-1. CY8C24x94 PSoC Device's Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
56-Pin (8x8 mm) QFN (Sawn)	CY8C24794-24LTXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN (Sawn) (Tape and Reel)	CY8C24794-24LTXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LTXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LTXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24794-24LFXI	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8C24794-24LFXIT	16K	1K	-40°C to +85°C	4	6	50	48	2	No
56-Pin (8x8 mm) QFN	CY8C24894-24LFXI	16K	1K	-40°C to +85°C	4	6	49	47	2	Yes
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8C24894-24LFXIT	16K	1K	-40°C to +85°C	4	6	49	47	2	Yes
68 Pin OCD (8x8 mm) QFN[21]	CY8C24094-24LFXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68 Pin (8x8 mm) QFN	CY8C24994-24LFXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68 Pin (8x8 mm) QFN (Tape and Reel)	CY8C24994-24LFXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24994-24LTXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24994-24LTXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100-Ball OCD (6x6 mm) VFBGA[21]	CY8C24094-24BVXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100-Ball (6x6 mm) VFBGA	CY8C24994-24BVXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
100 Pin OCD TQFP[21]	CY8C24094-24AXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24094-24LTXI	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes
68-Pin QFN (Sawn)	CY8C24094-24LTXIT	16K	1K	-40°C to +85°C	4	6	56	48	2	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

13. Document History Page

Document Title: CY8C24094, CY8C24794, CY8C24894 and CY8C24994 PSoC® Programmable System-on-Chip™ Document Number: 38-12018				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	133189	01.27.2004	NWJ	New silicon and new document – Advance Data Sheet.
*A	251672	See ECN	SFV	First Preliminary Data Sheet. Changed title to encompass only the CY8C24794 because the CY8C24494 and CY8C24694 are not being offered by Cypress.
*B	289742	See ECN	HMT	Add standard DS items from SFV memo. Add Analog Input Mux on pinouts. 2 MACs. Change 512 bytes of SRAM to 1K. Add dimension key to package. Remove HAPI. Update diagrams, registers and specs.
*C	335236	See ECN	HMT	Add CY logo. Update CY copyright. Update new CY.com URLs. Re-add ISSP programming pinout notation. Add Reflow Temp. table. Update features (MAC, Oscillator, and voltage range), registers (INT_CLR2/MSK2, second MAC), and specs. (Rext, IMO, analog output buffer...).
*D	344318	See ECN	HMT	Add new color and logo. Expand analog arch. diagram. Fix I/O #. Update Electrical Specifications.
*E	346774	See ECN	HMT	Add USB temperature specifications. Make data sheet Final.
*F	349566	See ECN	HMT	Remove USB logo. Add URL to preferred dimensions for mounting MLF packages.
*G	393164	See ECN	HMT	Add new device, CY8C24894 56-pin MLF with XRES pin. Add Fimousb3v char. to specs. Upgrade to CY Perform logo and update corporate address and copyright.
*H	469243	See ECN	HMT	Add ISSP note to pinout tables. Update typical and recommended Storage Temperature per industrial specs. Update Low Output Level maximum I/OL budget. Add FLS_PR1 to Register Map Bank 1 for users to specify which Flash bank should be used for SROM operations. Add two new devices for a 68-pin QFN and 100-ball VFBGA under RPNs: CY8C24094 and CY8C24994. Add two packages for 68-pin QFN. Add OCD non-production pinouts and package diagrams. Update CY branding and QFN convention. Add new Dev. Tool section. Update copyright and trademarks.
*I	561158	See ECN	HMT	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Add detailed dimensions to 56-pin QFN package diagram and update revision. Secure one package diagram/manufacturing per QFN. Update emulation pod/feet kit part numbers. Fix pinout type-o per TestTrack.
*J	728238	See ECN	HMT	Add CapSense SNR requirement reference. Update figure standards. Update Technical Training paragraphs. Add QFN package clarifications and dimensions. Update ECN-ed Amkor dimensioned QFN package diagram revisions. Reword SNR reference. Add new 56-pin QFN spec.
*K	2552459	08/14/08	AZIE/PYRS	Add footnote on AGND descriptions to avoid using P2[4] for digital signaling as it may add noise to AGND. Remove reference to CMP_GO_EN1 in Map Bank 1 Table on Address 65; this register has no functionality on 24xxx. Add footnote on die sales. Add description 'Optional External Clock Input' on P1[4] to match description of P1[4].
*L	2616550	12/05/08	OGNE/PYRS	Updated Programmable Pin Configuration detail. Changed title from PSoC® Mixed-Signal Array to PSoC® Programmable System-on-Chip™
*M	2657956	02/11/09	DPT/PYRS	Added package diagram 001-09618 and updated Ordering Information table
*N	2708135	05/18/2009	BRW	Added Note in the Pin Information section on page 8. Removed reference to Hi-Tech Lite Compiler in the section Development Tools Selection on page 42.
*O	2718162	06/11/2009	DPT	Added 56-Pin QFN (Sawn) package diagram and updated ordering information