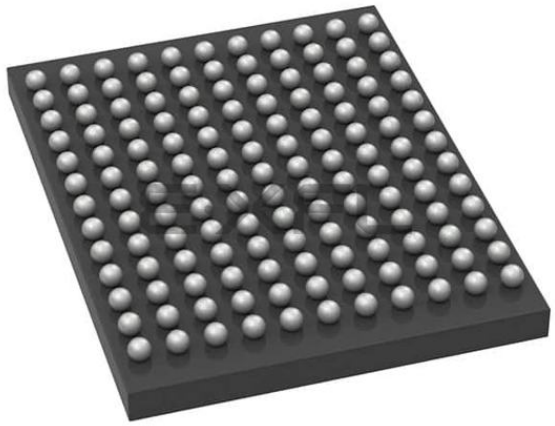

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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

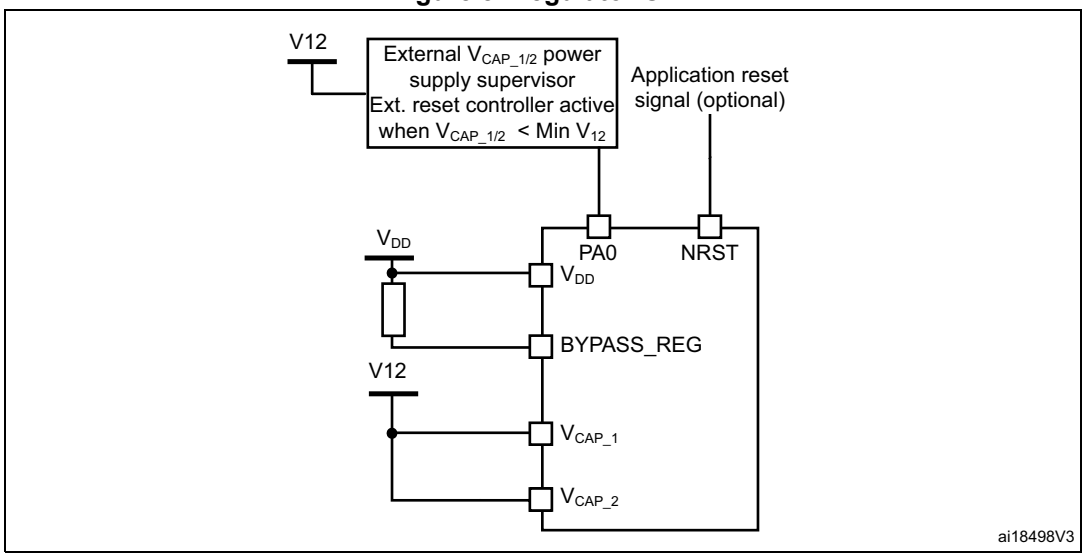
| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M7 |
| Core Size | 32-Bit Single-Core |
| Speed | 216MHz |
| Connectivity | CANbus, Ethernet, HDMI-CEC, I²C, IrDA, LINbus, MMC/SD, SAI, SPDIFRX, SPI, UART/USART, USB OTG |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 114 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 320K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.7V ~ 3.6V |
| Data Converters | A/D 24x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 143-UFBGA, WLCSP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f756zgy6tr |

# Contents

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the $V_{12}$ logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.
- The over-drive and under-drive modes are not available.
- The Standby mode is not available.

**Figure 8. Regulator OFF**

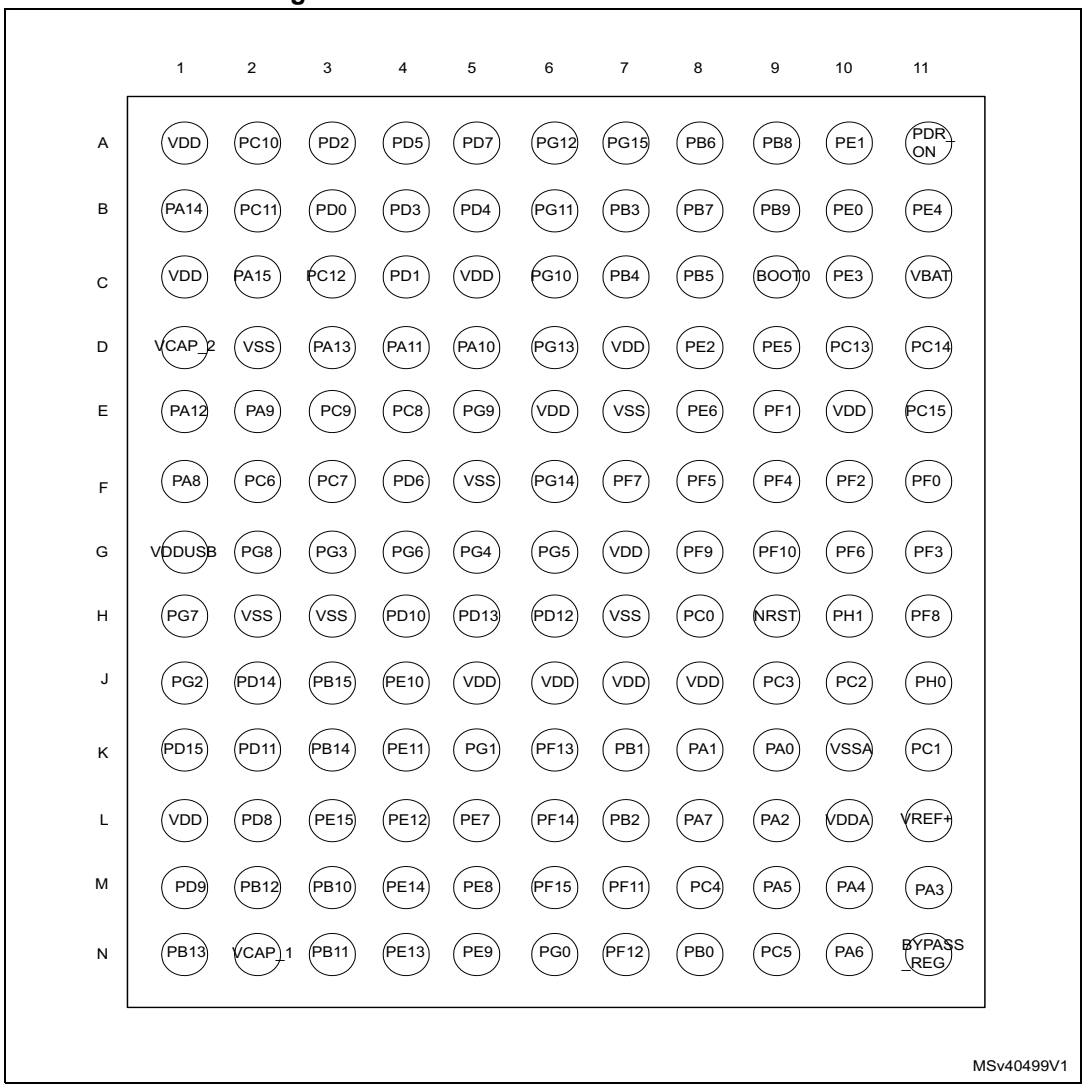



The following conditions must be respected:

- $V_{DD}$ should always be higher than $V_{CAP\_1}$ and $V_{CAP\_2}$ to avoid current injection between power domains.
- If the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is faster than the time for $V_{DD}$ to reach 1.7 V, then PA0 should be kept low to cover both conditions: until $V_{CAP\_1}$ and $V_{CAP\_2}$ reach $V_{12}$ minimum value and until $V_{DD}$ reaches 1.7 V (see *Figure 9*).
- Otherwise, if the time for $V_{CAP\_1}$ and $V_{CAP\_2}$ to reach $V_{12}$ minimum value is slower than the time for $V_{DD}$ to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 10*).
- If $V_{CAP\_1}$ and $V_{CAP\_2}$ go below $V_{12}$ minimum value and $V_{DD}$ is higher than 1.7 V, then a reset must be asserted on PA0 pin.

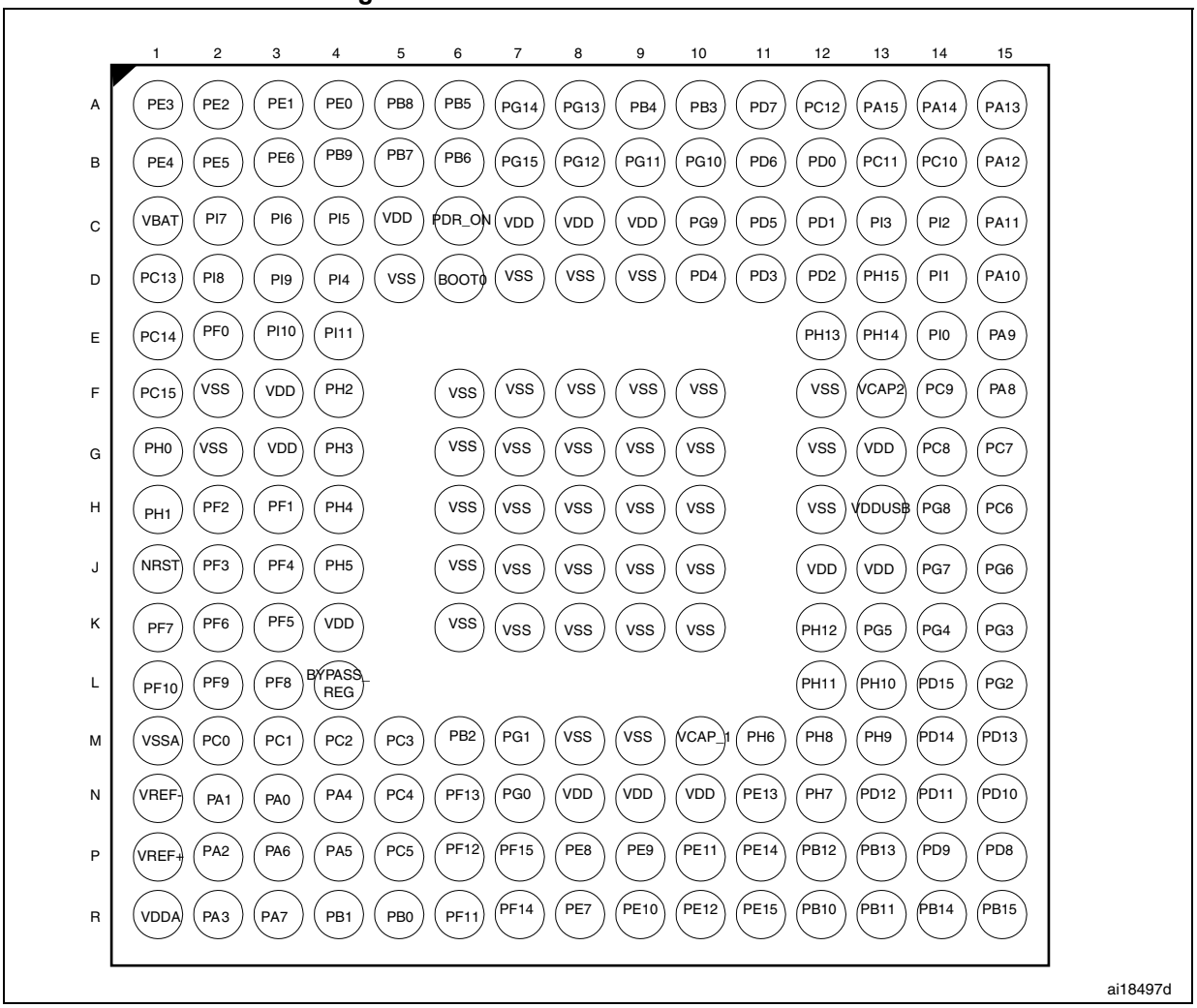
*Note: The minimum value of $V_{12}$ depends on the maximum frequency targeted in the application.*

**Figure 13. STM32F756Zx WLCSP143 ballout**




1. The above figure shows the package top view.

**Figure 17. STM32F756Ix UFBGA176 ballout**




1. The above figure shows the package top view.

Table 11. FMC pin definition (continued)

| Pin name | NOR/PSRAM/SRAM | NOR/PSRAM Mux | NAND16 | SDRAM |
|---|---|---|---|---|
| PF6 | - | - | - | - |
| PF7 | - | - | - | - |
| PF8 | - | - | - | - |
| PF9 | - | - | - | - |
| PF10 | - | - | - | - |
| PG6 | - | - | - | - |
| PG7 | - | - | INT | - |
| PE0 | NBL0 | NBL0 | - | NBL0 |
| PE1 | NBL1 | NBL1 | - | NBL1 |
| PI4 | NBL2 | - | - | NBL2 |
| PI5 | NBL3 | - | - | NBL3 |
| PG8 | - | - | - | SDCLK |
| PC0 | - | - | - | SDNWE |
| PF11 | - | - | - | SDNRAS |
| PG15 | - | - | - | SDNCAS |
| PH2 | - | - | - | SDCKE0 |
| PH3 | - | - | - | SDNE0 |
| PH6 | - | - | - | SDNE1 |
| PH7 | - | - | - | SDCKE1 |
| PH5 | - | - | - | SDNWE |
| PC2 | - | - | - | SDNE0 |
| PC3 | - | - | - | SDCKE0 |
| PB5 | - | - | - | SDCKE1 |
| PB6 | - | - | - | SDNE1 |

**Table 12. STM32F756xx alternate function mapping (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2 | TIM3/4/5 | TIM8/9/10/11/LPTIM1/CEC | I2C1/2/3/4/CEC | SPI1/2/3/4/5/6 | SPI3/SAI1 | SPI2/3/USART1/2/3/UART5/SPDIFRX | SAI2/USART6/UART4/5/7/8/SPDIFRX | CAN1/2/TIM12/13/14/QUADSPI/LCD | SAI2/QUADSPI/OTG2_HS/OTG1_FS | ETH/OTG1_FS | FMC/SDMMC1/OTG2_FS | DCMI | LCD | SYS |
| Port E | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCK_B | - | FMC_D11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | - | - | - | - | - | - | - | FMC_D12 | - | LCD_R7 | EVENTOUT |
| Port F | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENTOUT |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENTOUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENTOUT |
| | PF3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENTOUT |
| | PF4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENTOUT |
| | PF5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENTOUT |
| | PF6 | - | - | - | TIM10_CH1 | - | SPI5_NSS | SAI1_SD_B | - | UART7_Rx | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENTOUT |
| | PF7 | - | - | - | TIM11_CH1 | - | SPI5_SCK | SAI1_MCLK_B | - | UART7_Tx | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENTOUT |
| | PF8 | - | - | - | - | - | SPI5_MISO | SAI1_SCK_B | - | UART7_RTS | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENTOUT |
| | PF9 | - | - | - | - | - | SPI5_MOSI | SAI1_FS_B | - | UART7_CTS | TIM14_CH1 | QUADSPI_BK1_IO1 | - | - | - | - | EVENTOUT |
| | PF10 | - | - | - | - | - | - | - | - | - | - | - | - | - | DCMI_D11 | LCD_DE | EVENTOUT |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - | - | - | SAI2_SD_B | - | FMC_SDNRAS | DCMI_D12 | - | EVENTOUT |
| | PF12 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A6 | - | - | EVENTOUT |

**Table 13. STM32F756xx register boundary addresses**

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0xE00F FFFF - 0xFFFF FFFF | Reserved |
| Cortex-M7 | 0xE000 0000 - 0xE00F FFFF | Cortex-M7 internal peripherals |
| AHB3 | 0xD000 0000 - 0xDFFF FFFF | FMC bank 6 |
| | 0xC000 0000 - 0xCFFF FFFF | FMC bank 5 |
| | 0xA000 2000 - 0xBFFF FFFF | Reserved |
| | 0xA000 1000 - 0xA000 1FFF | Quad-SPI control register |
| | 0xA000 0000- 0xA000 0FFF | FMC control register |
| | 0x9000 0000 - 0x9FFF FFFF | Quad-SPI |
| | 0x8000 0000 - 0x8FFF FFFF | FMC bank 3 |
| | 0x7000 0000 - 0x7FFF FFFF | FMC bank 2 |
| | 0x6000 0000 - 0x6FFF FFFF | FMC bank 1 |
| | 0x5006 0C00- 0x5FFF FFFF | Reserved |
| AHB2 | 0x5006 0800 - 0x5006 0BFF | RNG |
| | 0x5006 0400 - 0x5006 07FF | HASH |
| | 0x5006 0000 - 0x5006 03FF | CRYP |
| | 0x5005 0400 - 0x5005 FFFF | Reserved |
| | 0x5005 0000 - 0x5005 03FF | DCMI |
| | 0x5004 0000- 0x5004 FFFF | Reserved |
| | 0x5000 0000 - 0x5003 FFFF | USB OTG FS |

Table 13. STM32F756xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4008 0000- 0x4FFF FFFF | Reserved |
| AHB1 | 0x4004 0000 - 0x4007 FFFF | USB OTG HS |
| | 0x4002 BC00- 0x4003 FFFF | Reserved |
| | 0x4002 B000 - 0x4002 BBFF | Chrom-ART (DMA2D) |
| | 0x4002 9400 - 0x4002 AFFF | Reserved |
| | 0x4002 9000 - 0x4002 93FF | ETHERNET MAC |
| | 0x4002 8C00 - 0x4002 8FFF | |
| | 0x4002 8800 - 0x4002 8BFF | |
| | 0x4002 8400 - 0x4002 87FF | |
| | 0x4002 8000 - 0x4002 83FF | |
| | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | 0x4002 6400 - 0x4002 67FF | DMA2 |
| | 0x4002 6000 - 0x4002 63FF | DMA1 |
| | 0x4002 5000 - 0X4002 5FFF | Reserved |
| | 0x4002 4000 - 0x4002 4FFF | BKPSRAM |
| | 0x4002 3C00 - 0x4002 3FFF | Flash interface register |
| | 0x4002 3800 - 0x4002 3BFF | RCC |
| | 0X4002 3400 - 0X4002 37FF | Reserved |
| | 0x4002 3000 - 0x4002 33FF | CRC |
| | 0x4002 2C00 - 0x4002 2FFF | Reserved |
| | 0x4002 2800 - 0x4002 2BFF | GPIOK |
| | 0x4002 2400 - 0x4002 27FF | GPIOJ |
| | 0x4002 2000 - 0x4002 23FF | GPIOI |
| | 0x4002 1C00 - 0x4002 1FFF | GPIOH |
| | 0x4002 1800 - 0x4002 1BFF | GPIOG |
| | 0x4002 1400 - 0x4002 17FF | GPIOF |
| | 0x4002 1000 - 0x4002 13FF | GPIOE |
| | 0X4002 0C00 - 0x4002 0FFF | GPIOD |
| | 0x4002 0800 - 0x4002 0BFF | GPIOC |
| | 0x4002 0400 - 0x4002 07FF | GPIOB |
| | 0x4002 0000 - 0x4002 03FF | GPIOA |

Table 13. STM32F756xx register boundary addresses (continued)

| Bus | Boundary address | Peripheral |
|---|---|---|
| | 0x4001 6C00- 0x4001 FFFF | Reserved |
| APB2 | 0x4001 6800 - 0x4001 6BFF | LCD-TFT |
| | 0x4001 6000 - 0x4001 67FF | Reserved |
| | 0x4001 5C00 - 0x4001 5FFF | SAI2 |
| | 0x4001 5800 - 0x4001 5BFF | SAI1 |
| | 0x4001 5400 - 0x4001 57FF | SPI6 |
| | 0x4001 5000 - 0x4001 53FF | SPI5 |
| | 0x4001 4C00 - 0x4001 4FFF | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | TIM11 |
| | 0x4001 4400 - 0x4001 47FF | TIM10 |
| | 0x4001 4000 - 0x4001 43FF | TIM9 |
| | 0x4001 3C00 - 0x4001 3FFF | EXTI |
| | 0x4001 3800 - 0x4001 3BFF | SYSCFG |
| | 0x4001 3400 - 0x4001 37FF | SPI4 |
| | 0x4001 3000 - 0x4001 33FF | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | SDMMC |
| | 0x4001 2400 - 0x4001 2BFF | Reserved |
| | 0x4001 2000 - 0x4001 23FF | ADC1 - ADC2 - ADC3 |
| | 0x4001 1800 - 0x4001 1FFF | Reserved |
| | 0x4001 1400 - 0x4001 17FF | USART6 |
| | 0x4001 1000 - 0x4001 13FF | USART1 |
| | 0x4001 0800 - 0x4001 0FFF | Reserved |
| | 0x4001 0400 - 0x4001 07FF | TIM8 |
| | 0x4001 0000 - 0x4001 03FF | TIM1 |

6. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and power-down operation.
7. The over-drive mode is not supported when the internal regulator is OFF.
8. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
9. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{Jmax}$.
10. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$.

**Table 18. Limitations depending on the operating power supply range**

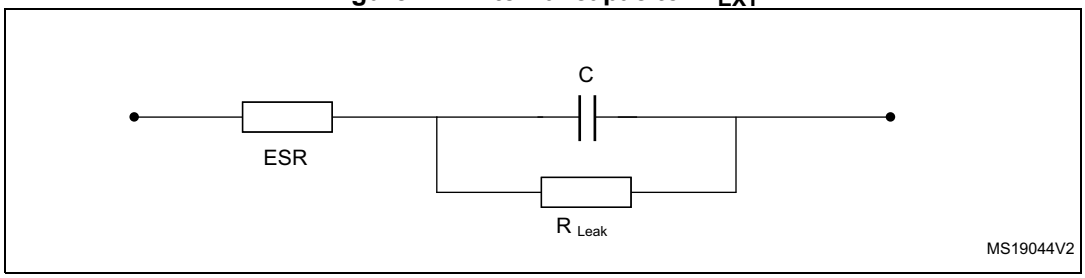
| Operating power supply range | ADC operation | Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$) | Maximum HCLK frequency vs Flash memory wait states (1)(2) | I/O operation | Possible Flash memory operations |
|---|---|---|---|---|---|
| $V_{DD}$ =1.7 to 2.1 V(3) | Conversion time up to 1.2 Msps | 20 MHz | 180 MHz with 8 wait states and over-drive OFF | No I/O compensation | 8-bit erase and program operations only |
| $V_{DD}$ = 2.1 to 2.4 V | Conversion time up to 1.2 Msps | 22 MHz | 216 MHz with 9 wait states and over-drive ON | No I/O compensation | 16-bit erase and program operations |
| $V_{DD}$ = 2.4 to 2.7 V | Conversion time up to 2.4 Msps | 24 MHz | 216 MHz with 8 wait states and over-drive ON | I/O compensation works | 16-bit erase and program operations |
| $V_{DD}$ = 2.7 to 3.6 V(4) | Conversion time up to 2.4 Msps | 30 MHz | 216 MHz with 7 wait states and over-drive ON | I/O compensation works | 32-bit erase and program operations |

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator on ITCM interface and L1-cache on AXI interface, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator or L1-cache allows to achieve a performance equivalent to 0-wait state program execution.
3. $V_{DD}/V_{DDA}$ minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 2.17.2: Internal reset OFF*).
4. The voltage range for USB full speed PHYs can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

## 5.3.2 VCAP1/VCAP2 external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor $C_{EXT}$ to the VCAP1/VCAP2 pins. $C_{EXT}$ is specified in *Table 19*.

**Figure 24. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted both to $f_{HCLK}$ frequency and $V_{DD}$ range (see *Table 18: Limitations depending on the operating power supply range*).
- When the regulator is ON, the voltage scaling and over-drive mode are adjusted to $f_{HCLK}$ frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 144$ MHz
  - Scale 2 for 144 MHz < $f_{HCLK} \leq 168$ MHz
  - Scale 1 for 168 MHz < $f_{HCLK} \leq 216$ MHz. The over-drive is only ON at 216 MHz.
- When the regulator is OFF, the V12 is provided externally as described in *Table 17: General operating conditions*:
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/4$, and $f_{PCLK2} = f_{HCLK}/2$.
- External clock frequency is 25 MHz and PLL is ON when $f_{HCLK}$ is higher than 25 MHz.
- The typical current consumption values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and for $T_A$= 25 °C unless otherwise specified.
- The maximum values are obtained for 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range and a maximum ambient temperature ($T_A$) unless otherwise specified.
- For the voltage range 1.7 V ≤ $V_{DD}$ ≤ 3.6 V, the maximum frequency is 180 MHz.

**Table 24. Typical and maximum current consumption in Run mode, code with data processing running from ITCM RAM, regulator ON**

| Symbol | Parameter | Conditions | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in RUN mode | All peripherals enabled(2)(3) | 216 | 178 | 208(4) | 230(4) | - | mA |
| | | | 200 | 165 | 193 | 212 | 230 | |
| | | | 180 | 147 | 171(4) | 185(4) | 198(4) | |
| | | | 168 | 130 | 152 | 164 | 177 | |
| | | | 144 | 100 | 116 | 127 | 137 | |
| | | | 60 | 44 | 52 | 63 | 73 | |
| | | | 25 | 21 | 25 | 36 | 46 | |
| | | All peripherals disabled(3) | 216 | 102 | 120(4) | 141(4) | - | |
| | | | 200 | 95 | 111 | 131 | 149 | |
| | | | 180 | 84 | 98(4) | 112(4) | 125(4) | |
| | | | 168 | 75 | 87 | 100 | 112 | |
| | | | 144 | 58 | 67 | 77 | 88 | |
| | | | 60 | 25 | 30 | 41 | 51 | |
| | | | 25 | 12 | 15 | 25 | 36 | |

1. Guaranteed by characterization results.

**Figure 25. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in low drive mode)**

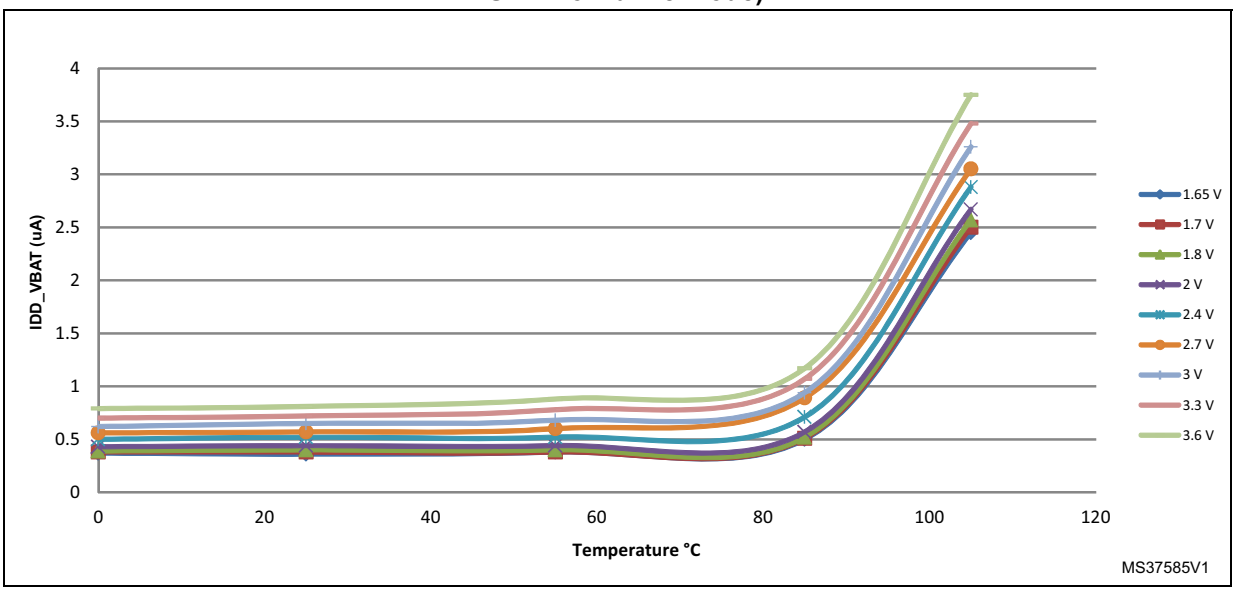
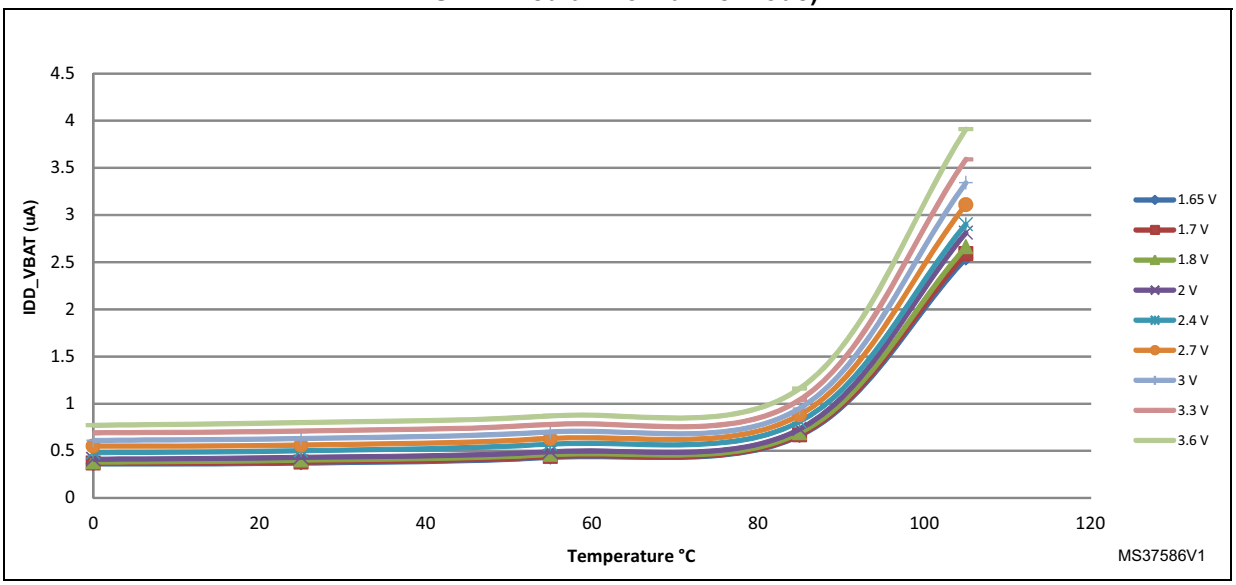



**Figure 26. Typical $V_{BAT}$ current consumption (RTC ON/BKP SRAM OFF and LSE in medium low drive mode)**



pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DD}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

**Table 34. Switching output I/O current consumption(1)**

| Symbol | Parameter | Conditions | I/O toggling frequency (fsw) MHz | Typ $V_{DD}$ = 3.3 V | Typ $V_{DD}$ = 1.8 V | Unit |
|---|---|---|---|---|---|---|
| $I_{DDIO}$ | I/O switching Current | $C_{EXT}$ = 0 pF $C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.1 | 0.1 | mA |
| | | | 8 | 0.4 | 0.2 | |
| | | | 25 | 1.1 | 0.7 | |
| | | | 50 | 2.4 | 1.3 | |
| | | | 60 | 3.1 | 1.6 | |
| | | | 84 | 4.3 | 2.4 | |
| | | | 90 | 4.9 | 2.6 | |
| | | | 100 | 5.4 | 2.8 | |
| | | | 108 | 5.6 | - | |
| | | $C_{EXT}$ = 10 pF $C = C_{INT} + C_S + C_{EXT}$ | 2 | 0.2 | 0.1 | |
| | | | 8 | 0.6 | 0.3 | |
| | | | 25 | 1.8 | 1.1 | |
| | | | 50 | 3.1 | 2.3 | |
| | | | 60 | 4.6 | 3.4 | |
| | | | 84 | 9.7 | 3.6 | |
| | | | 90 | 10.12 | 5.2 | |
| | | | 100 | 14.92 | 5.4 | |
| | | | 108 | 18.11 | - | |

**Table 43. Main PLL characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{LOCK}$ | PLL lock time | VCO freq = 100 MHz | | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | | 100 | - | 300 | |
| Jitter(3) | Cycle-to-cycle jitter | System clock 216 MHz | RMS | - | 25 | - | ps |
| | | | peak to peak | - | ±150 | - | |
| | Period Jitter | | RMS | - | 15 | - | |
| | | | peak to peak | - | ±200 | - | |
| | Main clock output (MCO) for RMII Ethernet | Cycle to cycle at 50 MHz on 1000 samples | | - | 32 | - | |
| | Main clock output (MCO) for MII Ethernet | Cycle to cycle at 25 MHz on 1000 samples | | - | 40 | - | |
| | Bit Time CAN jitter | Cycle to cycle at 1 MHz on 1000 samples | | - | 330 | - | |
| $I_{DD(PLL)}$(4) | PLL power consumption on $V_{DD}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.15<br>0.45 | - | 0.40<br>0.75 | mA |
| $I_{DDA(PLL)}$(4) | PLL power consumption on $V_{DDA}$ | VCO freq = 100 MHz<br>VCO freq = 432 MHz | | 0.30<br>0.55 | - | 0.40<br>0.85 | mA |

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of 2 PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

**Table 44. PLLI2S characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLLI2S\_IN}$ | PLLI2S input clock(1) | - | 0.95(2) | 1 | 2.10 | MHz |
| $f_{PLLI2SP\_OUT}$ | PLLI2S multiplier output clock for SPDIFRX | - | - | - | 216 | |
| $f_{PLLI2SQ\_OUT}$ | PLLI2S multiplier output clock for SAI | - | - | - | 216 | |
| $f_{PLLI2SR\_OUT}$ | PLLI2S multiplier output clock for I2S | - | - | - | 216 | |
| $f_{VCO\_OUT}$ | PLLI2S VCO output | - | 100 | - | 432 | |
| $t_{LOCK}$ | PLLI2S lock time | VCO freq = 100 MHz | 75 | - | 200 | µs |
| | | VCO freq = 432 MHz | 100 | - | 300 | |

### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 76* for the SPI interface are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 76. SPI dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode<br>SPI1,4,5,6<br>2.7≤VDD≤3.6 | - | - | 54(2) | MHz |
| | | Master mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 27 | |
| | | Master transmitter mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 54 | |
| | | Slave receiver mode<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 54 | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5,6<br>2.7≤VDD≤3.6 | | | 50(3) | |
| | | Slave mode transmitter/full duplex<br>SPI1,4,5,6<br>1.71≤VDD≤3.6 | | | 38(3) | |
| | | Master & Slave mode<br>SPI2,3<br>1.71≤VDD≤3.6 | | | 27 | |
| tsu(NSS) | NSS setup time | Slave mode, SPI presc = 2 | 4*Tpclk | - | - | ns |
| th(NSS) | NSS hold time | Slave mode, SPI presc = 2 | 2*Tpclk | - | - | |
| tw(SCKH)<br>tw(SCKL) | SCK high and low time | Master mode | Tpclk-2 | Tpclk | Tpclk+2 | |

**Figure 53. USB OTG full speed timings: definition of data signal rise and fall time**

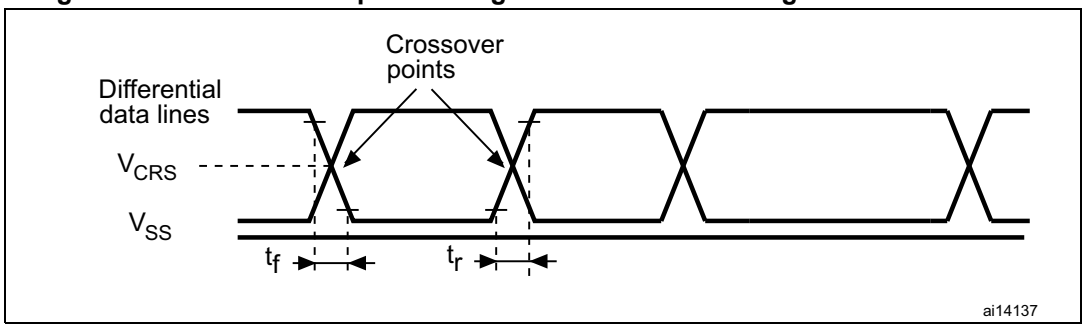



**Table 81. USB OTG full speed electrical characteristics(1)**

| Driver characteristics | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $t_r$ | Rise time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_f$ | Fall time(2) | $C_L$ = 50 pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/ fall time matching | $t_r/t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | - | 1.3 | 2.0 | V |
| $Z_{DRV}$ | Output driver impedance(3) | Driving high or low | 28 | 44 | Ω |

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).
3. No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.

## USB high speed (HS) characteristics

Unless otherwise specified, the parameters given in *Table 84* for ULPI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency summarized in *Table 83* and $V_{DD}$ supply voltage conditions summarized in *Table 82*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11, unless otherwise specified
- Capacitive load C = 20 pF, unless otherwise specified
- Measurement points are done at CMOS levels: $0.5V_{DD}$.

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output characteristics.

**Table 82. USB HS DC electrical characteristics**

| Symbol | | Parameter | Min.(1) | Max.(1) | Unit |
|---|---|---|---|---|---|
| **Input level** | $V_{DD}$ | USB OTG HS operating voltage | 1.7 | 3.6 | V |

1. All the voltages are measured from the local ground potential.

**Figure 63. Synchronous multiplexed PSRAM write timings**

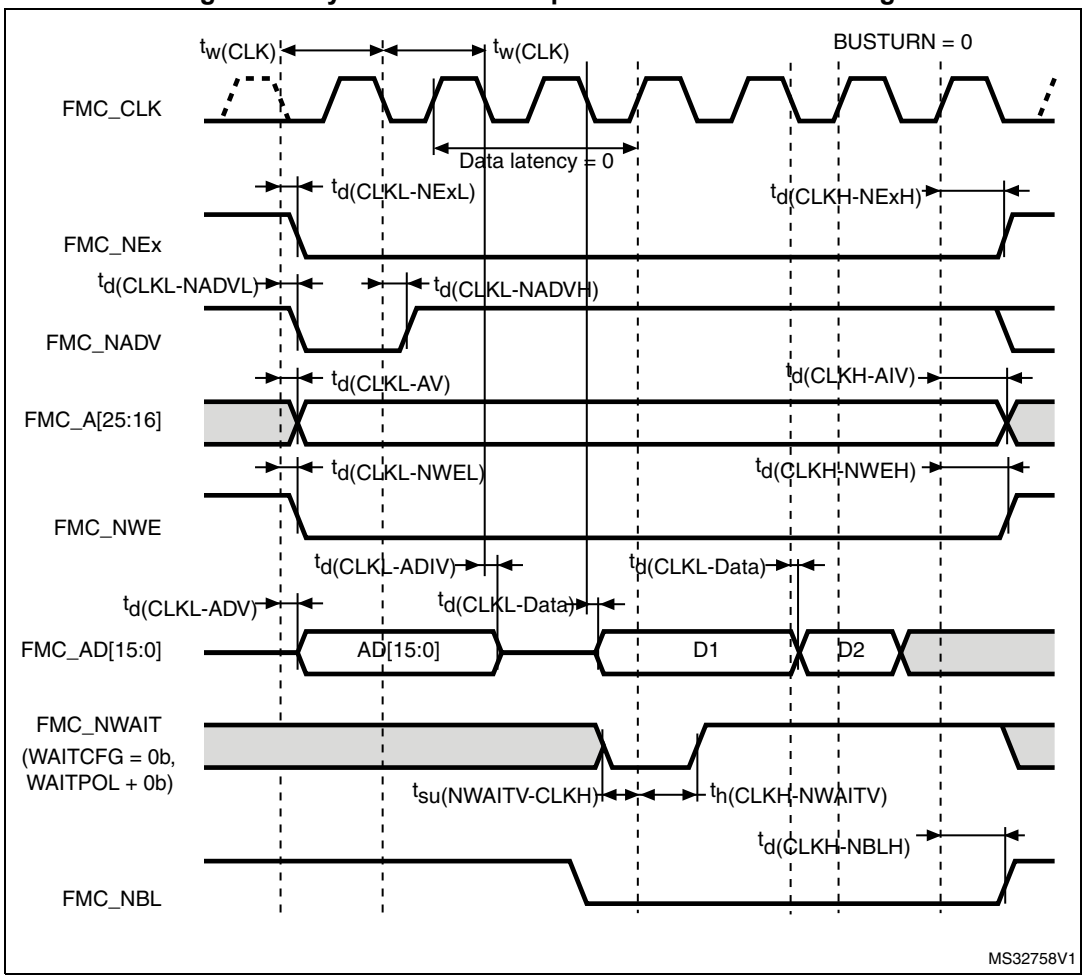


**Table 105. LPSDR SDRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{HCLK}-0.5$ | $2T_{HCLK}+0.5$ | ns |
| $t_{d(SDCLKL\_Data)}$ | Data output valid time | - | 4 | |
| $t_{h(SDCLKL\_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL\_Add)}$ | Address valid time | - | 3.5 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL-SDNE)}$ | Chip select valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

## 5.3.28 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 106* and *Table 107* for Quad-SPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 17: General operating conditions*, with the following configuration:

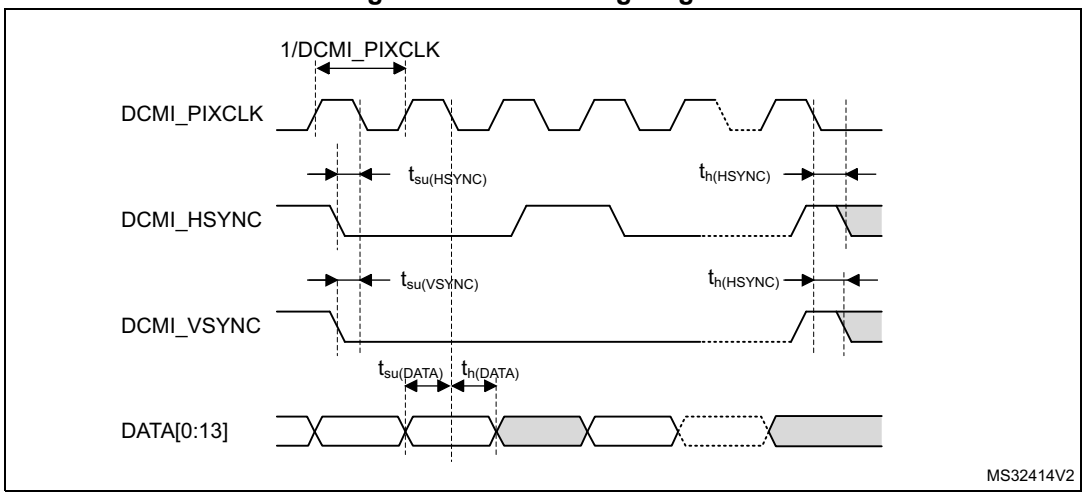
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 5.3.17: I/O port characteristics* for more details on the input/output alternate function characteristics.

**Table 106. Quad-SPI characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fck1/t(CK) | Quad-SPI clock frequency | 2.7 V≤$V_{DD}$<3.6 V CL=20 pF | - | - | 108 | MHz |
| | | 1.71 V<$V_{DD}$<3.6 V CL=15 pF | - | - | 100 | |

**Figure 74. DCMI timing diagram**




## 5.3.30 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 109* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage summarized in *Table 17*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity : low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits

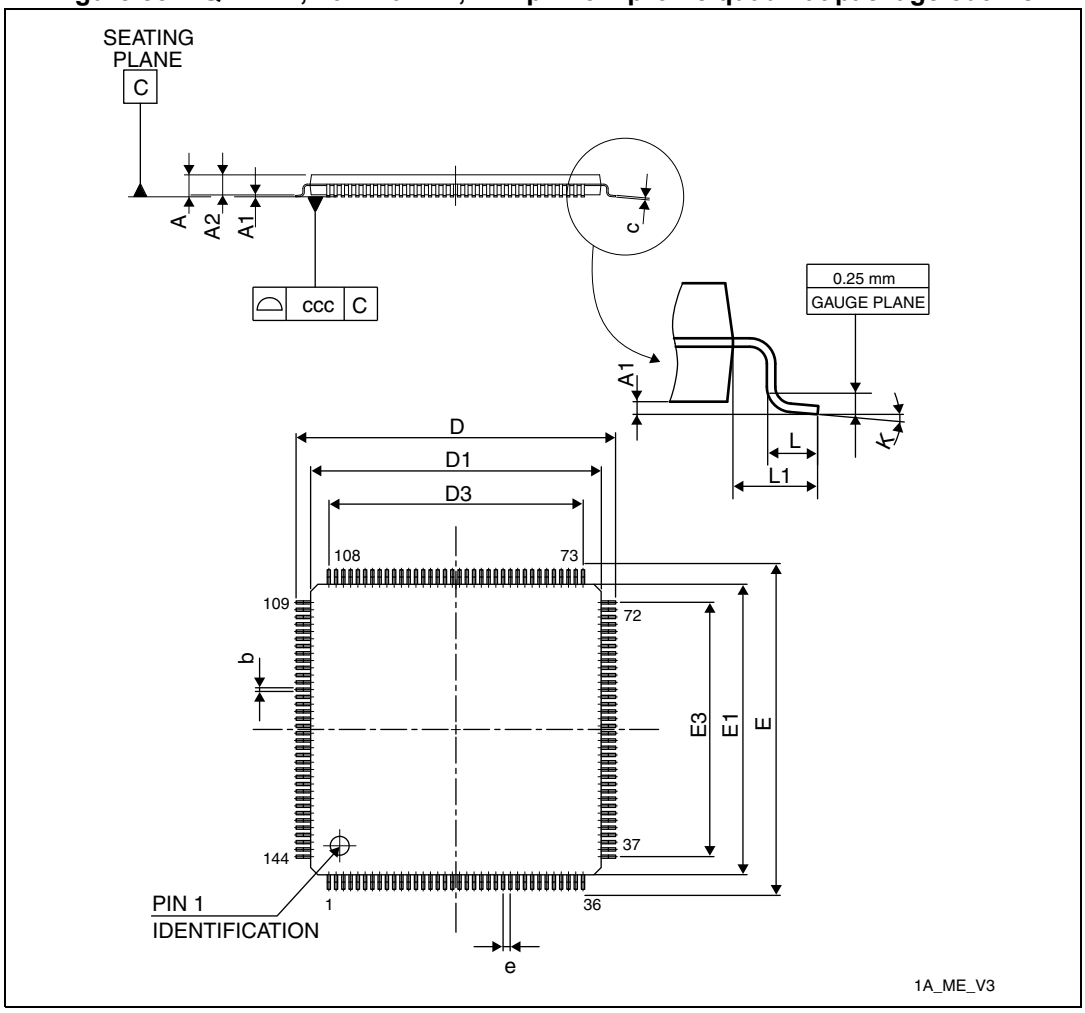
**Table 109. LTDC characteristics (1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{CLK}$ | LTDC clock output frequency | - | 45 | MHz |
| $D_{CLK}$ | LTDC clock output duty cycle | 45 | 55 | % |
| $t_{w(CLKH)}$<br>$t_{w(CLKL)}$ | Clock High time, low time | tw(CLK)/2 − 0.5 | tw(CLK)/2+0.5 | ns |
| $t_{v(DATA)}$ | Data output valid time | - | 6 | |
| $t_{h(DATA)}$ | Data output hold time | 2 | - | |
| $t_{v(HSYNC)}$ | HSYNC/VSYNC/DE output valid time | - | 3 | |
| $t_{v(VSYNC)}$ | | | | |
| $t_{v(DE)}$ | | | | |
| $t_{h(HSYNC)}$ | HSYNC/VSYNC/DE output hold time | 0.5 | - | |
| $t_{h(VSYNC)}$ | | | | |
| th(DE) | | | | |

1. Guaranteed by characterization results.

## 6.4 LQFP144, 20 x 20 mm low-profile quad flat package information

**Figure 88. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 117. LQFP144, 20 x 20 mm, 144-pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.874 |