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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16f873a-e-so">https://www.e-xfl.com/product-detail/microchip-technology/pic16f873a-e-so</a>

# PIC16F87XA

**TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION**

Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1  CLKI	13	14	30	32	I  I	ST/CMOS <sup>(4)</sup>	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2  CLKO	14	15	31	33	O  O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR  VPP	1	2	18	18	I  P	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low Reset to the device. Programming voltage input.
RA0/AN0 RA0 AN0 RA1/AN1 RA1 AN1 RA2/AN2/VREF-/CVREF RA2 AN2 VREF- CVREF RA3/AN3/VREF+ RA3 AN3 VREF+ RA4/T0CKI/C1OUT RA4  T0CKI C1OUT RA5/AN4/SS/C2OUT RA5 AN4 SS C2OUT	2   3   4   5   6   7	3   4   5   6   8	19   20   21   22   23   24	19   20   21   22   23   24	I/O I  I/O I  I/O I I O  I/O I I O  I/O I I O	TTL   TTL   TTL   TTL   ST   TTL	PORTA is a bidirectional I/O port.  Digital I/O. Analog input 0.  Digital I/O. Analog input 1.  Digital I/O. Analog input 2. A/D reference voltage (Low) input. Comparator VREF output.  Digital I/O. Analog input 3. A/D reference voltage (High) input.  Digital I/O – Open-drain when configured as output. Timer0 external clock input. Comparator 1 output.  Digital I/O. Analog input 4. SPI slave select input. Comparator 2 output.

**Legend:** I = input      O = output      I/O = input/output      P = power  
— = Not used      TTL = TTL input      ST = Schmitt Trigger input

- Note** 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.  
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.  
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

## 2.2.2.8 PCON Register

The Power Control (PCON) register contains flag bits to allow differentiation between a Power-on Reset (POR), a Brown-out Reset (BOR), a Watchdog Reset (WDT) and an external MCLR Reset.

**Note:**  $\overline{\text{BOR}}$  is unknown on Power-on Reset. It must be set by the user and checked on subsequent Resets to see if BOR is clear, indicating a brown-out has occurred. The BOR status bit is a “don’t care” and is not predictable if the brown-out circuit is disabled (by clearing the BODEN bit in the configuration word).

### REGISTER 2-8: PCON REGISTER (ADDRESS 8Eh)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-1
—	—	—	—	—	—	POR	$\overline{\text{BOR}}$
bit 7						bit 0	

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **POR:** Power-on Reset Status bit

1 = No Power-on Reset occurred

0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **BOR:** Brown-out Reset Status bit

1 = No Brown-out Reset occurred

0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as ‘0’

- n = Value at POR

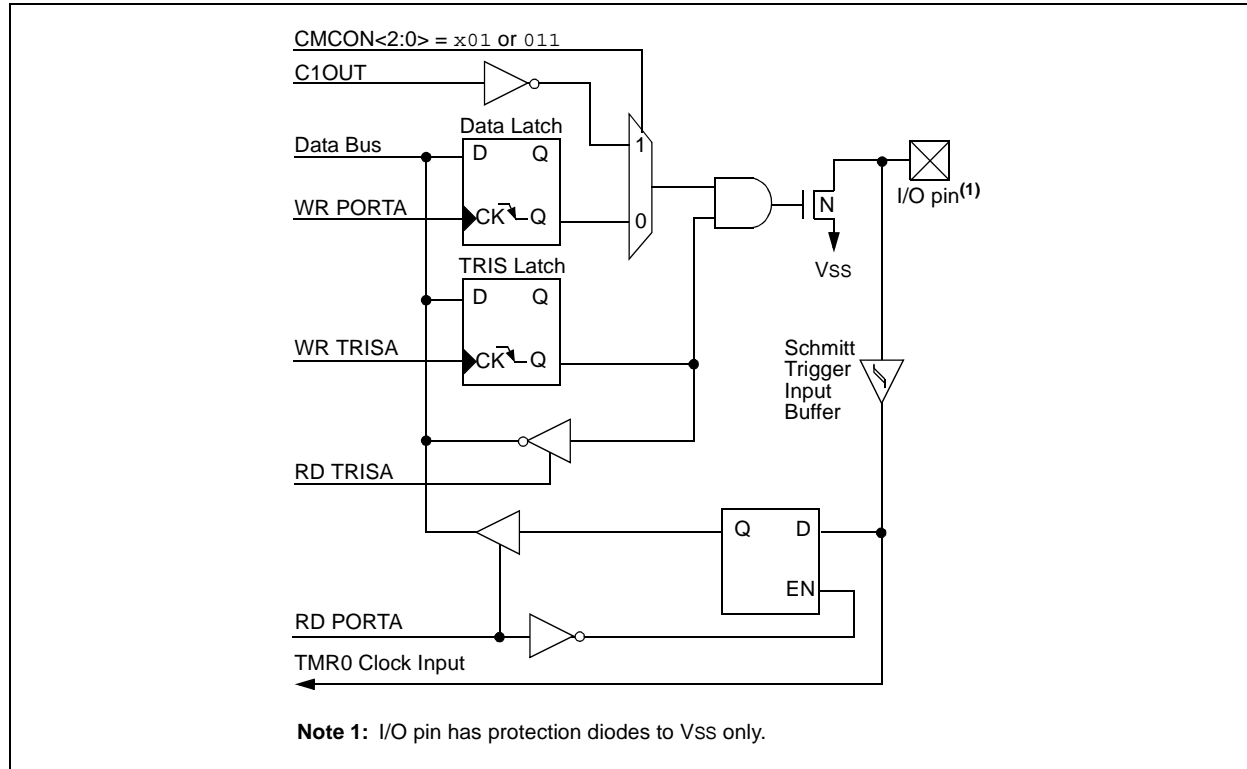
‘1’ = Bit is set

‘0’ = Bit is cleared

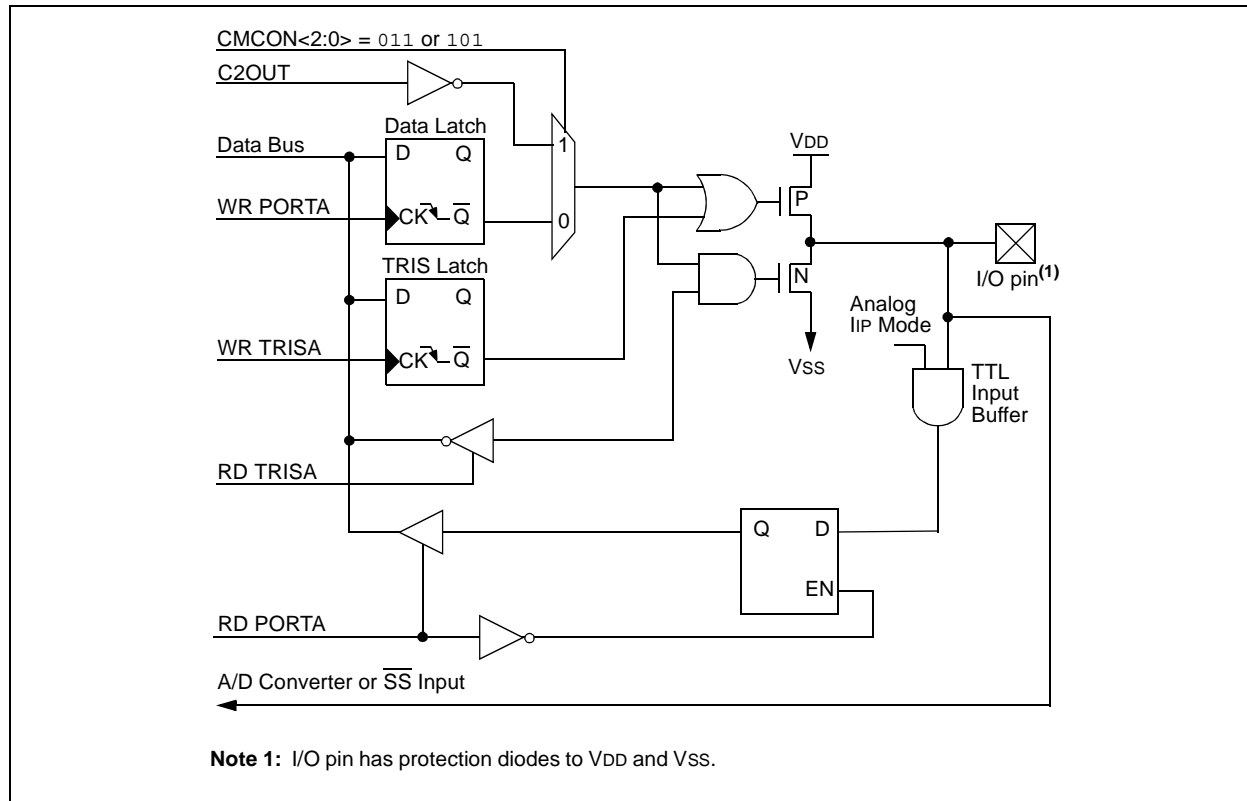
x = Bit is unknown

# PIC16F87XA

**FIGURE 4-2: BLOCK DIAGRAM OF RA4/T0CKI PIN**



**FIGURE 4-3: BLOCK DIAGRAM OF RA5 PIN**



**TABLE 4-3: PORTB FUNCTIONS**

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST <sup>(1)</sup>	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM <sup>(3)</sup>	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST <sup>(2)</sup>	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

**Legend:** TTL = TTL input, ST = Schmitt Trigger input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.

**2:** This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

**3:** Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

**TABLE 4-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBP	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

**Legend:** x = unknown, u = unchanged. Shaded cells are not used by PORTB.

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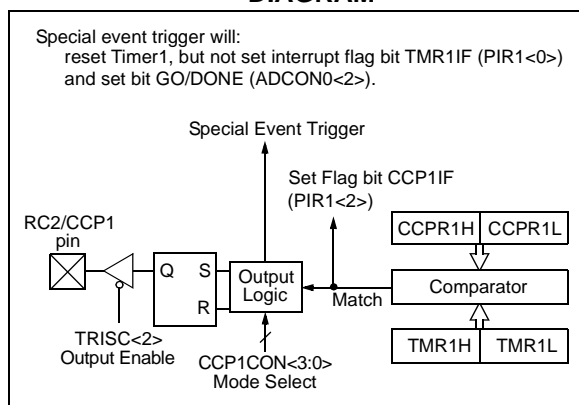
## 8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits, CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

**FIGURE 8-2: COMPARE MODE OPERATION BLOCK DIAGRAM**



### 8.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

**Note:** Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

### 8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

### 8.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen, the CCP1 pin is not affected. The CCPIF bit is set, causing a CCP interrupt (if enabled).

### 8.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of CCP2 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled).

**Note:** The special event trigger from the CCP1 and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

## 9.4 I<sup>2</sup>C Mode

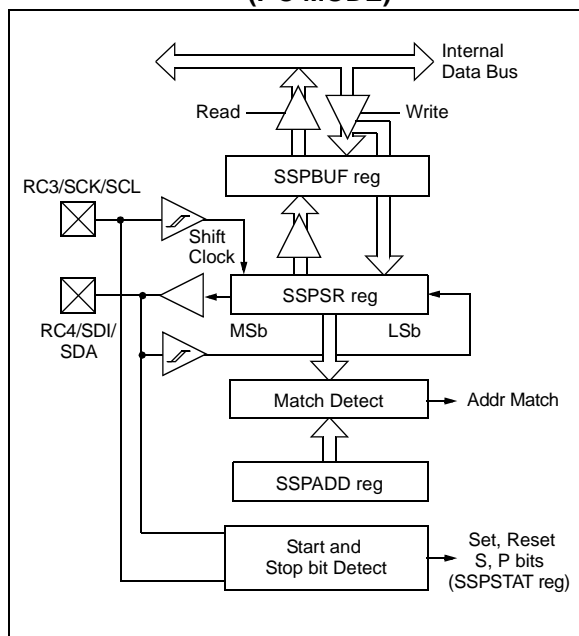
The MSSP module in I<sup>2</sup>C mode fully implements all master and slave functions (including general call support) and provides interrupts on Start and Stop bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer:

- Serial clock (SCL) – RC3/SCK/SCL
- Serial data (SDA) – RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

**FIGURE 9-7: MSSP BLOCK DIAGRAM (I<sup>2</sup>C MODE)**



### 9.4.1 REGISTERS

The MSSP module has six registers for I<sup>2</sup>C operation. These are:

- MSSP Control Register (SSPCON)
- MSSP Control Register 2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer Register (SSPBUF)
- MSSP Shift Register (SSPSR) – Not directly accessible
- MSSP Address Register (SSPADD)

SSPCON, SSPCON2 and SSPSTAT are the control and status registers in I<sup>2</sup>C mode operation. The SSPCON and SSPCON2 registers are readable and writable. The lower six bits of the SSPSTAT are read-only. The upper two bits of the SSPSTAT are read/write.

SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

SSPADD register holds the slave device address when the SSP is configured in I<sup>2</sup>C Slave mode. When the SSP is configured in Master mode, the lower seven bits of SSPADD act as the baud rate generator reload value.

In receive operations, SSPSR and SSPBUF together create a double-buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not double-buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

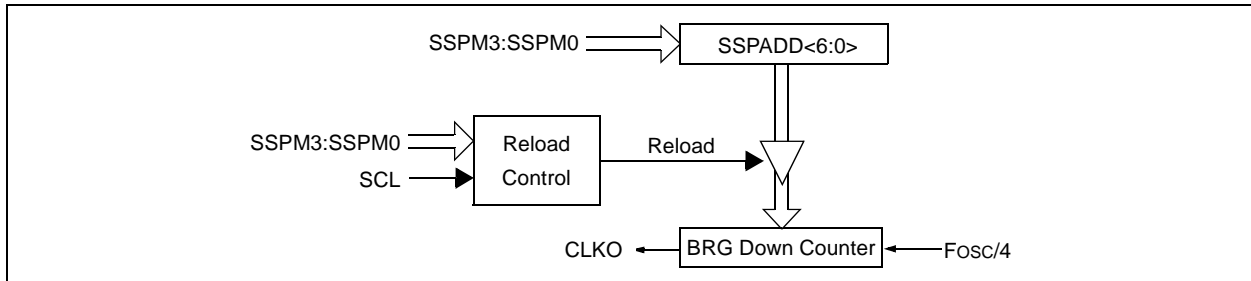
## 9.4.7 BAUD RATE GENERATOR

In I<sup>2</sup>C Master mode, the Baud Rate Generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 9-17). When a write occurs to SSPBUF, the Baud Rate Generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (Tcy) on the Q2 and Q4 clocks. In I<sup>2</sup>C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 9-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

**FIGURE 9-17: BAUD RATE GENERATOR BLOCK DIAGRAM**



**TABLE 9-3: I<sup>2</sup>C CLOCK RATE W/BRG**

Fcy	Fcy*2	BRG Value	Fscl (2 Rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz <sup>(1)</sup>
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	3Fh	100 kHz
4 MHz	8 MHz	0Ah	400 kHz <sup>(1)</sup>
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz <sup>(1)</sup>
1 MHz	2 MHz	0Ah	100 kHz
1 MHz	2 MHz	00h	1 MHz <sup>(1)</sup>

**Note 1:** The I<sup>2</sup>C interface does not conform to the 400 kHz I<sup>2</sup>C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.



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## 9.4.17.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

- A low level is sampled on SDA when SCL goes from low level to high level.
- SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user deasserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

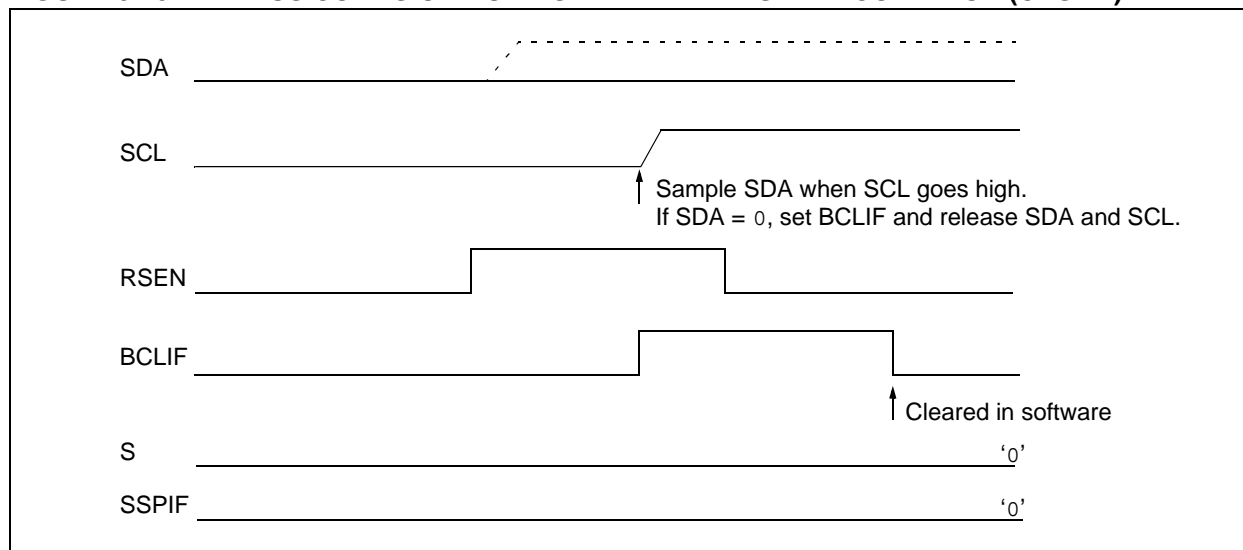
If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', see Figure 9-29). If SDA is sampled high, the BRG is

reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

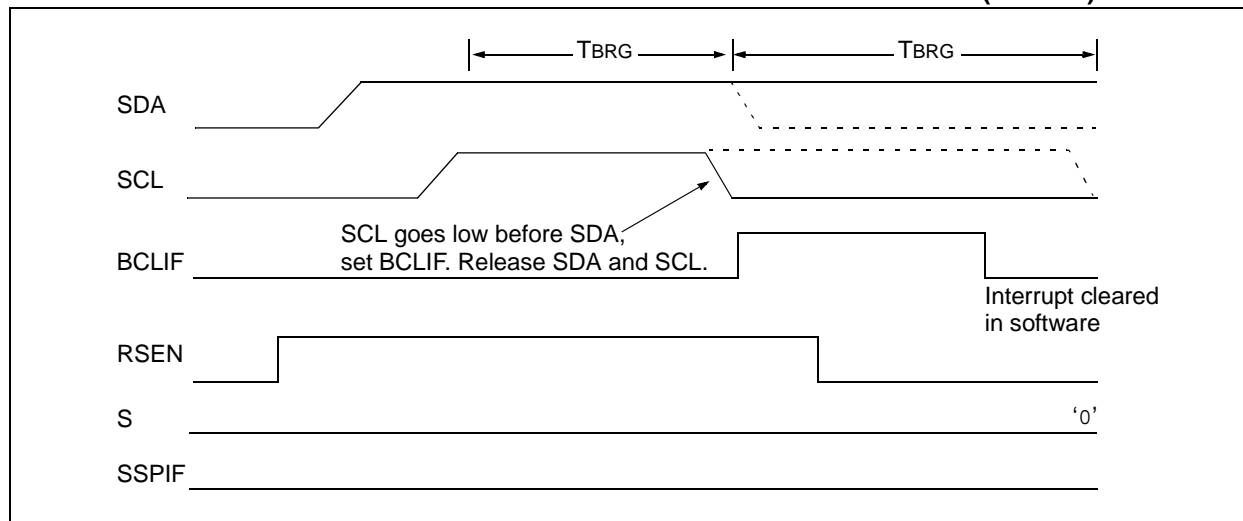
If SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition (Figure 9-30).

If at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

**FIGURE 9-29: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)**



**FIGURE 9-30: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)**



## 11.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the 40/44-pin devices.

The conversion of an analog input signal results in a corresponding 10-bit digital number. The A/D module has high and low-voltage reference input that is software selectable to some combination of VDD, VSS, RA2 or RA3.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D clock must be derived from the A/D's internal RC oscillator.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

The ADCON0 register, shown in Register 11-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 11-2, configures the functions of the port pins. The port pins can be configured as analog inputs (RA3 can also be the voltage reference) or as digital I/O.

Additional information on using the A/D module can be found in the PIC® Mid-Range MCU Family Reference Manual (DS33023).

### REGISTER 11-1: ADCON0 REGISTER (ADDRESS 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)  
 001 = Channel 1 (AN1)  
 010 = Channel 2 (AN2)  
 011 = Channel 3 (AN3)  
 100 = Channel 4 (AN4)  
 101 = Channel 5 (AN5)  
 110 = Channel 6 (AN6)  
 111 = Channel 7 (AN7)

**Note:** The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)

0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up

0 = A/D converter module is shut-off and consumes no operating current

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared      x = Bit is unknown

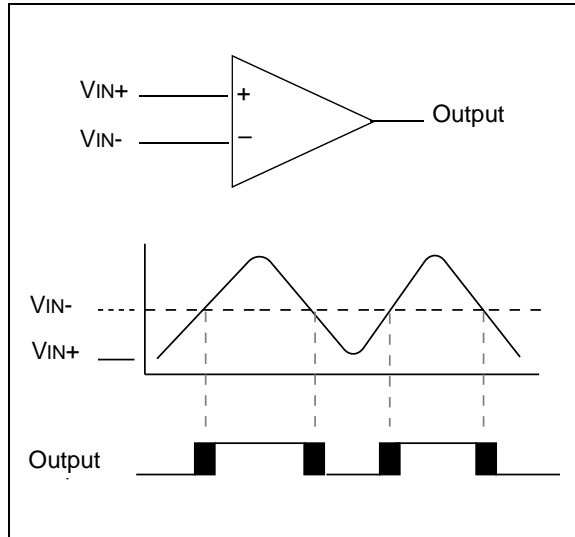
## 12.2 Comparator Operation

A single comparator is shown in Figure 12-2 along with the relationship between the analog input levels and the digital output. When the analog input at  $V_{IN+}$  is less than the analog input  $V_{IN-}$ , the output of the comparator is a digital low level. When the analog input at  $V_{IN+}$  is greater than the analog input  $V_{IN-}$ , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 12-2 represent the uncertainty due to input offsets and response time.

## 12.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal present at  $V_{IN-}$  is compared to the signal at  $V_{IN+}$  and the digital output of the comparator is adjusted accordingly (Figure 12-2).

**FIGURE 12-2: SINGLE COMPARATOR**



### 12.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between  $V_{SS}$  and  $V_{DD}$  and can be applied to either pin of the comparator(s).

### 12.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. **Section 13.0 “Comparator Voltage Reference Module”** contains a detailed description of the Comparator Voltage Reference module that provides this signal. The internal reference signal is used when comparators are in mode,  $CM<2:0> = 110$  (Figure 12-1). In this mode, the internal voltage reference is applied to the  $V_{IN+}$  pin of both comparators.

## 12.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (**Section 17.0 “Electrical Characteristics”**).

## 12.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RA4 and RA5 I/O pins. When enabled, multiplexors in the output path of the RA4 and RA5 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 12-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA4 and RA5 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits ( $CMCON<4:5>$ ).

- Note 1:** When reading the Port register, all pins configured as analog inputs will read as a ‘0’. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
- 2:** Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.
- 3:** RA4 is an open collector I/O pin. When used as an output, a pull-up resistor is required.

# PIC16F87XA

**TABLE 12-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INTIE	RBIE	TMR0IF	INTIF	RBIF	0000 000x	0000 000u
0Dh	PIR2	—	CMIF	—	—	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-- 0000	-0-- 0000
8Dh	PIE2	—	CMIE	—	—	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-- 0000	-0-- 0000
05h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	--11 1111

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are unused by the comparator module.

## 14.13 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKI pin. That means that the WDT will run even if the clock on the OSC1/CLKI and OSC2/CLKO pins of the device has been stopped, for example, by execution of a *SLEEP* instruction.

During normal operation, a WDT time-out generates a device Reset (Watchdog Timer Reset). If the device is in Sleep mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The  $\overline{TO}$  bit in the Status register will be cleared upon a Watchdog Timer time-out.

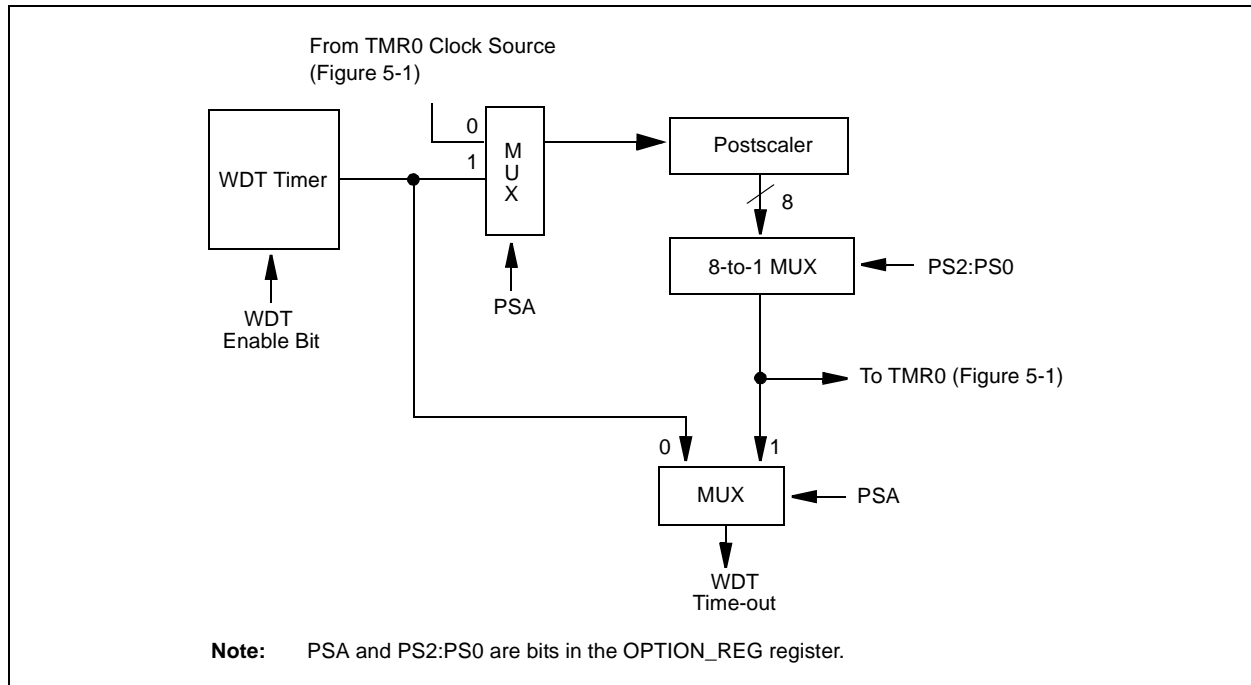
The WDT can be permanently disabled by clearing configuration bit, WDTE (Section 14.1 “Configuration Bits”).

WDT time-out period values may be found in Section 17.0 “Electrical Characteristics” under parameter #31. Values for the WDT prescaler (actually a postscaler but shared with the Timer0 prescaler) may be assigned using the OPTION\_REG register.

**Note 1:** The *CLRWDT* and *SLEEP* instructions clear the WDT and the postscaler, if assigned to the WDT and prevent it from timing out and generating a device Reset condition.

**2:** When a *CLRWDT* instruction is executed and the prescaler is assigned to the WDT, the prescaler count will be cleared but the prescaler assignment is not changed.

**FIGURE 14-11: WATCHDOG TIMER BLOCK DIAGRAM**



**TABLE 14-7: SUMMARY OF WATCHDOG TIMER REGISTERS**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2007h	Config. bits	(1)	BODEN <sup>(1)</sup>	CP1	CP0	$\overline{PWRTE}$ <sup>(1)</sup>	WDTE	Fosc1	Fosc0
81h, 181h	OPTION_REG	RBPV	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

**Legend:** Shaded cells are not used by the Watchdog Timer.

**Note 1:** See Register 14-1 for operation of these bits.

## 15.2 Instruction Descriptions

### ADDLW Add Literal and W

Syntax:	[ <i>label</i> ] ADDLW <i>k</i>
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

### ADDWF Add W and f

Syntax:	[ <i>label</i> ] ADDWF <i>f</i> , <i>d</i>
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### ANDLW AND Literal with W

Syntax:	[ <i>label</i> ] ANDLW <i>k</i>
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .\text{AND.} (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

### ANDWF AND W with f

Syntax:	[ <i>label</i> ] ANDWF <i>f</i> , <i>d</i>
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .\text{AND.} (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

### BCF Bit Clear f

Syntax:	[ <i>label</i> ] BCF <i>f</i> , <i>b</i>
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$0 \rightarrow (f<b>)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

### BSF Bit Set f

Syntax:	[ <i>label</i> ] BSF <i>f</i> , <i>b</i>
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$1 \rightarrow (f<b>)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

### BTFSS Bit Test f, Skip if Set

Syntax:	[ <i>label</i> ] BTFSS <i>f</i> , <i>b</i>
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$
Operation:	skip if $(f<b>) = 1$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2 Tcy instruction.

### BTFSC Bit Test, Skip if Clear

Syntax:	[ <i>label</i> ] BTFSC <i>f</i> , <i>b</i>
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f<b>) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b' in register 'f' is '0', the next instruction is discarded and a NOP is executed instead, making this a 2 Tcy instruction.

## **DECFSZ      Decrement f, Skip if 0**

**Syntax:**            [ *label* ] DECFSZ f,d

**Operands:**         $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**         $(f) - 1 \rightarrow (\text{destination});$   
skip if result = 0

**Status Affected:** None

**Description:**     The contents of register 'f' are decremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.  
If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2 Tcy instruction.

## **INCFSZ      Increment f, Skip if 0**

**Syntax:**            [ *label* ] INCFSZ f,d

**Operands:**         $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**         $(f) + 1 \rightarrow (\text{destination});$   
skip if result = 0

**Status Affected:** None

**Description:**     The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.  
If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2 Tcy instruction.

## **GOTO          Unconditional Branch**

**Syntax:**            [ *label* ] GOTO k

**Operands:**         $0 \leq k \leq 2047$

**Operation:**         $k \rightarrow \text{PC}<10:0>$   
 $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$

**Status Affected:** None

**Description:**     GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

## **IORLW        Inclusive OR Literal with W**

**Syntax:**            [ *label* ] IORLW k

**Operands:**         $0 \leq k \leq 255$

**Operation:**         $(W) .OR. k \rightarrow (W)$

**Status Affected:** Z

**Description:**     The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

## **INCF          Increment f**

**Syntax:**            [ *label* ] INCF f,d

**Operands:**         $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**         $(f) + 1 \rightarrow (\text{destination})$

**Status Affected:** Z

**Description:**     The contents of register 'f' are incremented. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

## **IORWF        Inclusive OR W with f**

**Syntax:**            [ *label* ] IORWF f,d

**Operands:**         $0 \leq f \leq 127$   
 $d \in [0,1]$

**Operation:**         $(W) .OR. (f) \rightarrow (\text{destination})$

**Status Affected:** Z

**Description:**     Inclusive OR the W register with register 'f'. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.

## 16.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

## 16.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

## 16.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

## 16.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

## 16.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PIC series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

## 16.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.



# PIC16F87XA

**TABLE 17-1: COMPARATOR SPECIFICATIONS**

<b>Operating Conditions:</b> 3.0V < V <sub>DD</sub> < 5.5V, -40°C < T <sub>A</sub> < +85°C (unless otherwise stated) 4.0V < V <sub>DD</sub> < 5.5V, -40°C < T <sub>A</sub> < +125°C (unless otherwise stated)							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D300	V <sub>IOFF</sub>	Input Offset Voltage	—	± 5.0	± 10	mV	
D301	V <sub>ICM</sub>	Input Common Mode Voltage*	0	-	V <sub>DD</sub> - 1.5	V	
D302	CMRR	Common Mode Rejection Ratio*	55	-	—	dB	
300 300A	T <sub>RESP</sub>	Response Time <sup>(1)</sup>	—	150	400 600	ns ns	PIC16F87XA PIC16LF87XA
301	T <sub>MC2OV</sub>	Comparator Mode Change to Output Valid*	—	—	10	μs	

\* These parameters are characterized but not tested.

**Note 1:** Response time measured with one comparator input at (V<sub>DD</sub> - 1.5)/2 while the other input transitions from V<sub>SS</sub> to V<sub>DD</sub>.

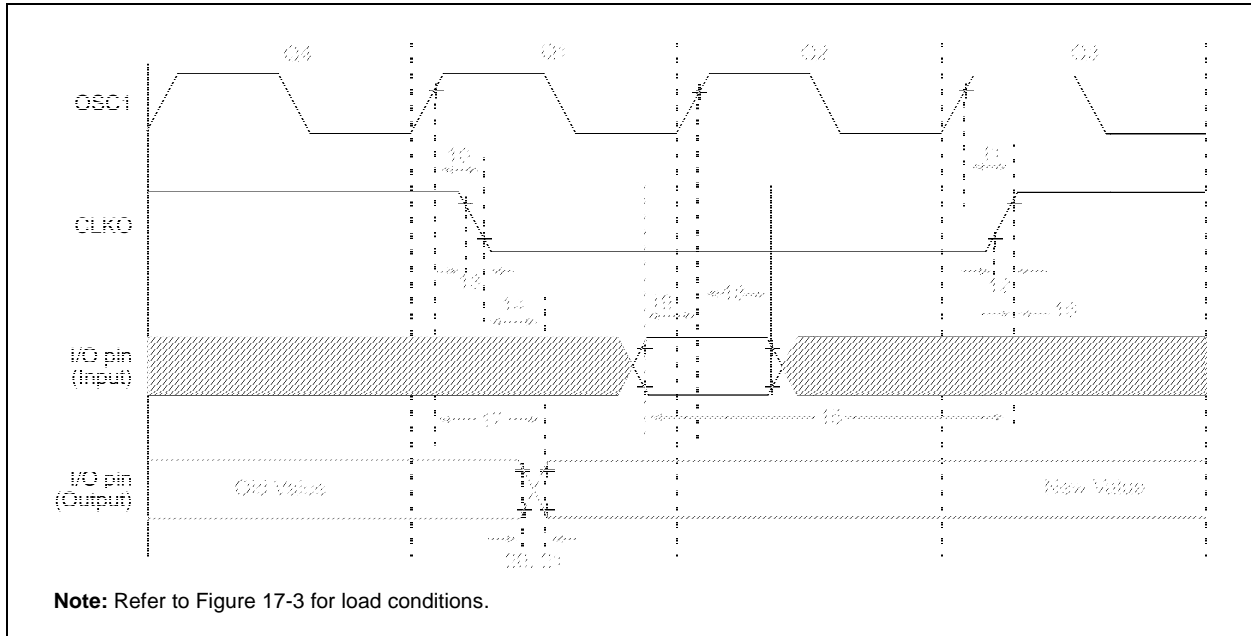
**TABLE 17-2: VOLTAGE REFERENCE SPECIFICATIONS**

<b>Operating Conditions:</b> 3.0V < V <sub>DD</sub> < 5.5V, -40°C < T <sub>A</sub> < +85°C (unless otherwise stated) 4.0V < V <sub>DD</sub> < 5.5V, -40°C < T <sub>A</sub> < +125°C (unless otherwise stated)							
Spec No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D310	V <sub>RES</sub>	Resolution	V <sub>DD</sub> /24	—	V <sub>DD</sub> /32	LSb	
D311	V <sub>RAA</sub>	Absolute Accuracy	— —	— —	1/2 1/2	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
D312	V <sub>RUR</sub>	Unit Resistor Value (R)*	—	2k	—	Ω	
310	T <sub>SET</sub>	Settling Time <sup>(1)</sup>	—	—	10	μs	

\* These parameters are characterized but not tested.

**Note 1:** Settling time measured while VRR = 1 and VR<3:0> transitions from '0000' to '1111'.

**FIGURE 17-5: CLKO AND I/O TIMING**



**TABLE 17-4: CLKO AND I/O TIMING REQUIREMENTS**

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1 ↑ to CLKO ↓	—	75	200	ns	(Note 1)
11*	TosH2ckH	OSC1 ↑ to CLKO ↑	—	75	200	ns	(Note 1)
12*	TckR	CLKO Rise Time	—	35	100	ns	(Note 1)
13*	TckF	CLKO Fall Time	—	35	100	ns	(Note 1)
14*	TckL2ioV	CLKO ↓ to Port Out Valid	—	—	0.5 T <sub>CY</sub> + 20	ns	(Note 1)
15*	TioV2ckH	Port In Valid before CLKO ↑	T <sub>OSC</sub> + 200	—	—	ns	(Note 1)
16*	TckH2ioI	Port In Hold after CLKO ↑	0	—	—	ns	(Note 1)
17*	TosH2ioV	OSC1 ↑ (Q1 cycle) to Port Out Valid	—	100	255	ns	
18*	TosH2ioI	OSC1 ↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	Standard (F)	100	—	ns	
			Extended (LF)	200	—	ns	
19*	TioV2osH	Port Input Valid to OSC1 ↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port Output Rise Time	Standard (F)	—	10	ns	
			Extended (LF)	—	145	ns	
21*	TioF	Port Output Fall Time	Standard (F)	—	10	ns	
			Extended (LF)	—	145	ns	
22††	TINP	INT pin High or Low Time	T <sub>CY</sub>	—	—	ns	
23††	TRBP	RB7:RB4 Change INT High or Low Time	T <sub>CY</sub>	—	—	ns	

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

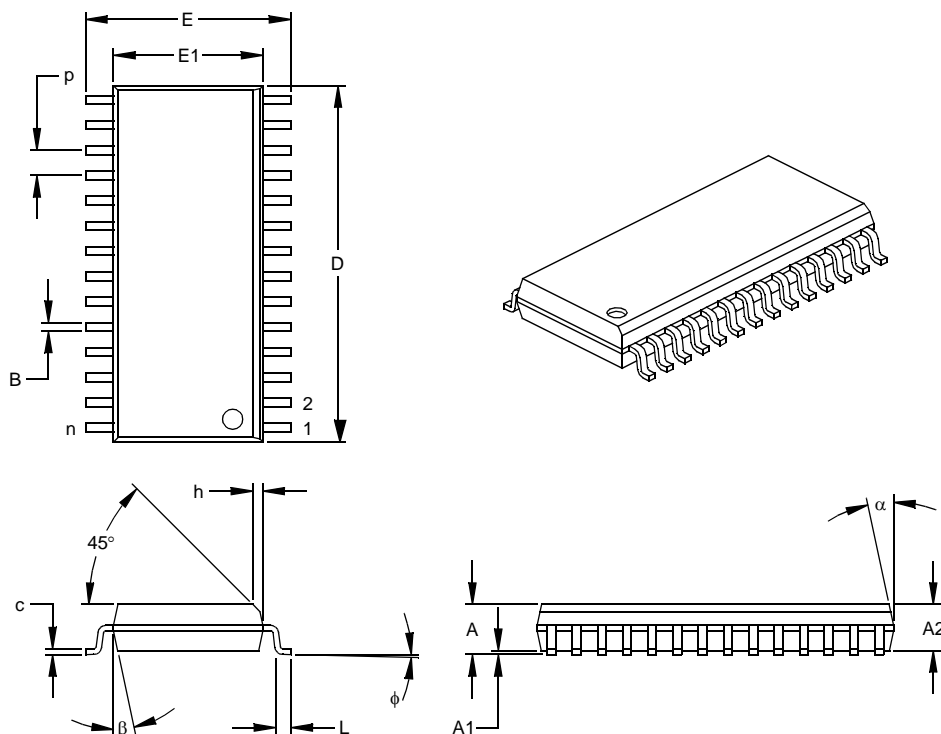
†† These parameters are asynchronous events not related to any internal clock edges.

**Note 1:** Measurements are taken in RC mode where CLKO output is 4 x T<sub>OSC</sub>.

# PIC16F87XA

## 28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	φ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

\* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

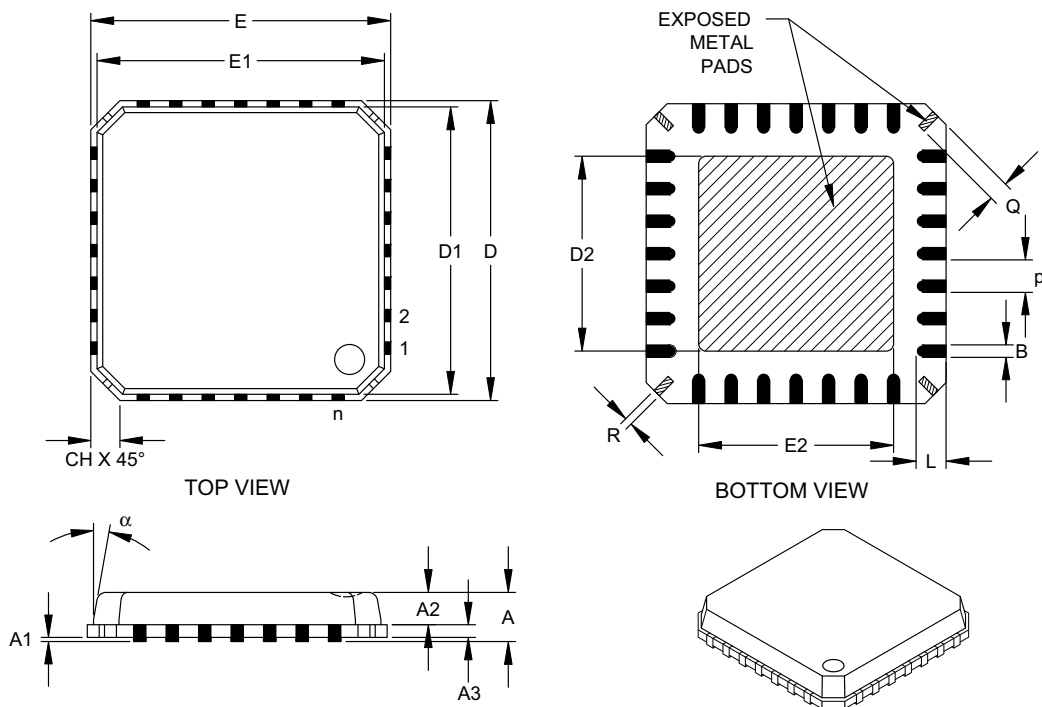
JEDEC Equivalent: MS-013

Drawing No. C04-052

# PIC16F87XA

## 28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body, Punch Singulated (QFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A		.033	.039		0.85	1.00
Molded Package Thickness	A2		.026	.031		0.65	0.80
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3		.008 REF			0.20 REF	
Overall Width	E		.236 BSC			6.00 BSC	
Molded Package Width	E1		.226 BSC			5.75 BSC	
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85
Overall Length	D		.236 BSC			6.00 BSC	
Molded Package Length	D1		.226 BSC			5.75 BSC	
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85
Lead Width	B	.009	.011	.014	0.23	0.28	0.35
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65
Chamfer	CH	.009	.017	.024	0.24	0.42	0.60
Mold Draft Angle Top	α			12°			12°

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: mMO-220

Drawing No. C04-114

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