



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f873a-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## **Pin Diagrams (Continued)**



## 4.4 PORTD and TRISD Registers

Note:	PORTD and TRISD are not implemented
	on the 28-pin devices.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

PORTD can be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit, PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.

### FIGURE 4-8: PORTD BLOCK DIAGRAM (IN I/O PORT MODE)



Name	Bit#	Buffer Type	Function
RD0/PSP0	bit 0	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 0.
RD1/PSP1	bit 1	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 1.
RD2/PSP2	bit2	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 2.
RD3/PSP3	bit 3	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 3.
RD4/PSP4	bit 4	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 4.
RD5/PSP5	bit 5	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 5.
RD6/PSP6	bit 6	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 6.
RD7/PSP7	bit 7	ST/TTL <sup>(1)</sup>	Input/output port pin or Parallel Slave Port bit 7.

## TABLE 4-7:PORTD FUNCTIONS

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in Parallel Slave Port mode.

TABLE 4-0. JUNIMANT OF REGISTERS ASSOCIATED WITH FORT	TABLE 4-8:	SUMMARY OF REGISTERS ASSOCIATED WITH PORTD
---	------------	--

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on: BOR	Valu all o Res	e on ther sets
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx	xxxx	uuuu	uuuu
88h	TRISD	PORT	PORTD Data Direction Register							1111	1111	1111	1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE		PORTE I	Data Dire	ction Bits	0000	-111	0000	-111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

	TABLE 5-1:	<b>REGISTERS ASSOCIATED WITH TIMERO</b>
--	------------	---

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR, E	on: BOR	Valu all o Res	e on ther sets
01h,101h	TMR0	Timer0 N	/lodule Regi	ister						XXXX X	xxxx	uuuu	uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 (	000x	0000	000u
81h,181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 3	1111	1111	1111

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by Timer0.

REGISTER 8-1:	CCP1CON	I REGISTE	ER/CCP2C	ON REGIS	STER (ADDF	RESS 17h	/1Dh)		
	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
	—	—	CCPxX	CCPxY	CCPxM3	CCPxM2	CCPxM1	CCPxM0	
	bit 7							bit 0	
bit 7-6	Unimplem	ented: Roa	d as '0'						
bit 5-4	CCPvX·CC		Least Sign	ificant hits					
511 5 4	<u>Capture mode:</u> Unused. <u>Compare mode:</u>								
	Unused.								
	<u>PWM mode</u> These bits	<u>e:</u> are the two	LSbs of the	PWM duty	cycle. The eig	ht MSbs ar	e found in C	CPRxL.	
bit 3-0	CCPxM3:C	CPxM0: C	CPx Mode S	Select bits					
	<ul> <li>0000 = Capture/Compare/PWM disabled (resets CCPx module)</li> <li>0100 = Capture mode, every falling edge</li> <li>0101 = Capture mode, every thrising edge</li> <li>0111 = Capture mode, every 16th rising edge</li> <li>1000 = Compare mode, set output on match (CCPxIF bit is set)</li> <li>1001 = Compare mode, clear output on match (CCPxIF bit is set)</li> <li>1010 = Compare mode, generate software interrupt on match (CCPxIF bit is set, CCPx pin is unaffected)</li> <li>1011 = Compare mode, trigger special event (CCPxIF bit is set, CCPx pin is unaffected); CCP<sup>-</sup> resets TMR1; CCP2 resets TMR1 and starts an A/D conversion (if A/D module is enabled)</li> <li>11xx = PWM mode</li> </ul>							CCPx pin is ted); CCP1 module is	
	Legend:								
	R = Reada	ble bit	VV = V	Vritable bit	U = Unimp	plemented b	oit, read as	0'	
	- n = Value	at POR	'1' = E	Bit is set	'0' = Bit is	cleared	x = Bit is u	nknown	

## 9.4.4.5 Clock Synchronization and the CKP Bit

When the CKP bit is cleared, the SCL output is forced to '0'; however, setting the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external  $I^2C$  master device has already asserted the SCL line. The SCL output will remain low until the CKP bit is set and all other devices on the  $I^2C$  bus have deasserted SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 9-12).





NOTES:

## 10.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit, CSRC (TXSTA<7>).

### 10.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 10-6. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit, TXIF (PIR1<4>), is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a readonly bit which is set when the TSR is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit, TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 10-9). The transmission can also be started by first loading the TXREG register and then setting bit TXEN (Figure 10-10). This is advantageous when slow baud rates are selected since the BRG is kept in Reset when bits TXEN, CREN and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally, when transmission is first started, the TSR register is empty so a transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to highimpedance. If either bit CREN or bit SREN is set during a transmission, the transmission is aborted and the DT pin reverts to a high-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic, however, is not reset, although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting since bit TXEN is still set. The DT line will immediately switch from High-Impedance Receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 10.1 "USART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- 8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

#### CONFIGURATION WORD (ADDRESS 2007h)<sup>(1)</sup> REGISTER 14-1: R/P-1 U-0 **R/P-1** R/P-1 R/P-1 R/P-1 R/P-1 **R/P-1** U-0 U-0 **R/P-1** R/P-1 **R/P-1** R/P-1 CP DEBUG WRT1 WRT0 CPD PWRTEN WDTEN Fosc1 LVP BOREN Fosc0 bit 13 bit0 bit 13 CP: Flash Program Memory Code Protection bit 1 = Code protection off0 = All program memory code-protected bit 12 Unimplemented: Read as '1' DEBUG: In-Circuit Debugger Mode bit bit 11 1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins 0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger bit 10-9 WRT1:WRT0 Flash Program Memory Write Enable bits For PIC16F876A/877A: 11 = Write protection off; all program memory may be written to by EECON control 10 = 0000h to 00FFh write-protected; 0100h to 1FFFh may be written to by EECON control 01 = 0000h to 07FFh write-protected; 0800h to 1FFFh may be written to by EECON control 00 = 0000h to 0FFFh write-protected; 1000h to 1FFFh may be written to by EECON control For PIC16F873A/874A: 11 = Write protection off; all program memory may be written to by EECON control 10 = 0000h to 00FFh write-protected; 0100h to 0FFFh may be written to by EECON control 01 = 0000h to 03FFh write-protected; 0400h to 0FFFh may be written to by EECON control 00 = 0000h to 07FFh write-protected; 0800h to 0FFFh may be written to by EECON control bit 8 CPD: Data EEPROM Memory Code Protection bit 1 = Data EEPROM code protection off 0 = Data EEPROM code-protected bit 7 LVP: Low-Voltage (Single-Supply) In-Circuit Serial Programming Enable bit 1 = RB3/PGM pin has PGM function; low-voltage programming enabled 0 = RB3 is digital I/O, HV on MCLR must be used for programming bit 6 BOREN: Brown-out Reset Enable bit 1 = BOR enabled0 = BOR disabled Unimplemented: Read as '1' bit 5-4 **PWRTEN:** Power-up Timer Enable bit bit 3 1 = PWRT disabled 0 = PWRT enabled bit 2 WDTEN: Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled Fosc1:Fosc0: Oscillator Selection bits bit 1-0 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator Legend:

R = Readable bit P = Programmable bit

U = Unimplemented bit, read as '0'

n = Value when device is unprogrammed

u = Unchanged from programmed state

**Note 1:** The erased (unprogrammed) value of the Configuration Word is 3FFFh.

## 14.3 Reset

The PIC16F87XA differentiates between various kinds of Reset:

- Power-on Reset (POR)
- MCLR Reset during normal operation
- MCLR Reset during Sleep
- WDT Reset (during normal operation)
- WDT Wake-up (during Sleep)
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition. Their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on Power-on Reset (POR), on the MCLR and WDT Reset, on MCLR Reset during Sleep and Brownout Reset (BOR). They are not affected by a WDT wake-up which is viewed as the resumption of normal operation. The TO and PD bits are set or cleared differently in different Reset situations as indicated in Table 14-4. These bits are used in software to determine the nature of the Reset. See Table 14-6 for a full description of Reset states of all registers.

A simplified block diagram of the on-chip Reset circuit is shown in Figure 14-4.

### FIGURE 14-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Register		Dev	ices		Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset	Wake-up via WDT or Interrupt
TRISD	73A	74A	76A	77A	1111 1111	1111 1111	uuuu uuuu
TRISE	73A	74A	76A	77A	0000 -111	0000 -111	uuuu -uuu
	73A	74A	76A	77A	r000 0000	r000 0000	ruuu uuuu
	73A	74A	76A	77A	0000 0000	0000 0000	uuuu uuuu
PIE2	73A	74A	76A	77A	-0-0 00	-0-0 00	-u-u uu
PCON	73A	74A	76A	77A	dd	uu	uu
SSPCON2	73A	74A	76A	77A	0000 0000	0000 0000	uuuu uuuu
PR2	73A	74A	76A	77A	1111 1111	1111 1111	1111 1111
SSPADD	73A	74A	76A	77A	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	73A	74A	76A	77A	00 0000	00 0000	uu uuuu
TXSTA	73A	74A	76A	77A	0000 -010	0000 -010	uuuu -uuu
SPBRG	73A	74A	76A	77A	0000 0000	0000 0000	uuuu uuuu
CMCON	73A	974	76A	77A	0000 0111	0000 0111	uuuu uuuu
CVRCON	73A	74A	76A	77A	000- 0000	000- 0000	uuu- uuuu
ADRESL	73A	74A	76A	77A	xxxx xxxx	սսսս սսսս	սսսս սսսս
ADCON1	73A	74A	76A	77A	00 0000	00 0000	uu uuuu
EEDATA	73A	74A	76A	77A	xxxx xxxx	սսսս սսսս	uuuu uuuu
EEADR	73A	74A	76A	77A	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATH	73A	74A	76A	77A	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADRH	73A	74A	76A	77A	XXXX XXXX	uuuu uuuu	uuuu uuuu
EECON1	73A	74A	76A	77A	x x000	u u000	u uuuu
EECON2	73A	74A	76A	77A			

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition, r = reserved, maintain clear. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 14-5 for Reset value for specific condition.

### FIGURE 14-6: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD VIA RC NETWORK)



© 2001-2013 Microchip Technology Inc.



## FIGURE 14-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



## FIGURE 14-9: SLOW RISE TIME (MCLR TIED TO VDD VIA RC NETWORK)



## 15.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories:

- Byte-oriented operations
- Bit-oriented operations
- Literal and control operations

Each PIC16 instruction is a 14-bit word divided into an **opcode** which specifies the instruction type and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 15-1, while the various opcode fields are summarized in Table 15-1.

Table 15-2 lists the instructions recognized by the MPASM<sup>™</sup> Assembler. A complete description of each instruction is also available in the PIC<sup>®</sup> Mid-Range MCU Family Reference Manual (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or eleven-bit constant or literal value

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1  $\mu$ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles with the second cycle executed as a NOP.

Note:	To maintain upward compatibility with
	future PIC16F87XA products, do not use
	the OPTION and TRIS instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

## 15.1 READ-MODIFY-WRITE OPERATIONS

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register. For example, a "CLRF PORTB" instruction will read PORTB, clear all the data bits, then write the result back to PORTB. This example would have the unintended result that the condition that sets the RBIF flag would be cleared.

## TABLE 15-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= $0$ or $1$ ). The assembler will generate code with x = $0$ . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; $d = 0$ : store result in W, d = 1: store result in file register f. Default is $d = 1$ .
PC	Program Counter
ТО	Time-out bit
PD	Power-down bit

## FIGURE 15-1: GENERAL FORMAT FOR INSTRUCTIONS



SWAPF	Swap Nibbles in f		
Syntax:	[ label ] SWAPF f,d		
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$		
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$		
Status Affected:	None		
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.		

XORWF	Exclusive OR W with f				
Syntax:	[ label ] XORWF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d  \in  [0,1] \end{array}$				
Operation:	(W) .XOR. (f) $\rightarrow$ (destination)				
Status Affected:	Z				
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.				

XORLW	Exclusive OR Literal with W
Syntax:	[ <i>label</i> ] XORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .XOR. $k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

NOTES:

## 16.0 DEVELOPMENT SUPPORT

The PIC<sup>®</sup> microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB<sup>®</sup> IDE Software
- Assemblers/Compilers/Linkers
  - MPASM<sup>™</sup> Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK<sup>™</sup> Object Linker/
  - MPLIB<sup>™</sup> Object Librarian
  - MPLAB C30 C Compiler
  - MPLAB ASM30 Assembler/Linker/Library
- Simulators
  - MPLAB SIM Software Simulator
- MPLAB dsPIC30 Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
  - PRO MATE<sup>®</sup> II Universal Device Programmer
  - PICSTART<sup>®</sup> Plus Development Programmer
- Low Cost Demonstration Boards
  - PICDEM<sup>™</sup> 1 Demonstration Board
  - PICDEM.net<sup>™</sup> Demonstration Board
  - PICDEM 2 Plus Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 4 Demonstration Board
  - PICDEM 17 Demonstration Board
  - PICDEM 18R Demonstration Board
  - PICDEM LIN Demonstration Board
  - PICDEM USB Demonstration Board
- Evaluation Kits
  - KEELOQ<sup>®</sup>
  - PICDEM MSC
  - microID<sup>®</sup>
  - CAN
  - PowerSmart<sup>®</sup>
  - Analog

## 16.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows<sup>®</sup> based application that contains:

- · An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help
- The MPLAB IDE allows you to:
- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files (assembly or C)
  - absolute listing file (mixed assembly and C)
  - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

## 16.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel<sup>®</sup> standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
70*	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK $\downarrow$ or SCK $\uparrow$ Input		Тсү	_	—	ns	
71*	TscH	SCK Input High Time (Slave mode)		TCY + 20	_	_	ns	
72*	TscL	SCK Input Low Time (Slave mode)		TCY + 20	_	-	ns	
73*	TDIV2SCH, TDIV2SCL	Setup Time of SDI Data Input to SCI	K Edge	100	_	—	ns	
74*	TSCH2DIL, TSCL2DIL	Hold Time of SDI Data Input to SCK	100	_	—	ns		
75*	TDOR	SDO Data Output Rise Time	Standard( <b>F</b> ) Extended( <b>LF</b> )	_	10 25	25 50	ns ns	
76*	TDOF	SDO Data Output Fall Time	_	10	25	ns		
77*	TssH2doZ	SS ↑ to SDO Output High-Impedanc	10	_	50	ns		
78*	TSCR	SCK Output Rise Time (Master mode)	Standard( <b>F</b> ) Extended( <b>LF</b> )		10 25	25 50	ns ns	
79*	TscF	SCK Output Fall Time (Master mode	)	—	10	25	ns	
80*	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge	Standard( <b>F</b> ) Extended( <b>LF</b> )	_		50 145	ns	
81*	TDOV2scH, TDOV2scL	SDO Data Output Setup to SCK Edg	Тсү		—	ns		
82*	TssL2doV	SDO Data Output Valid after $\overline{SS} \downarrow E$	_	_	50	ns		
83*	TscH2ssH, TscL2ssH	SS ↑ after SCK Edge	1.5 TCY + 40	—	—	ns		

### TABLE 17-9: SPI MODE REQUIREMENTS

\* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



## FIGURE 17-15: I<sup>2</sup>C BUS START/STOP BITS TIMING

## 44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES			MILLIMETERS*		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	р		.031			0.80	
Pins per Side	n1		11			11	
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039		1.00		
Foot Angle	¢	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20
Lead Width	В	.012	.015	.017	0.30	0.38	0.44
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

\* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-026 Drawing No. C04-076

## 28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body, Punch Singulated (QFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES		MILLIMETERS*				
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р	.026 BSC			0.65 BSC			
Overall Height	Α		.033	.039		0.85	1.00	
Molded Package Thickness	A2		.026	.031		0.65	0.80	
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05	
Base Thickness	A3	.008 REF			0.20 REF			
Overall Width	E		.236 BSC		6.00 BSC			
Molded Package Width	E1		.226 BSC		5.75 BSC			
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85	
Overall Length	D	.236 BSC			6.00 BSC			
Molded Package Length	D1	.226 BSC			5.75 BSC			
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85	
Lead Width	В	.009	.011	.014	0.23	0.28	0.35	
Lead Length	L	.020	.024	.030	0.50	0.60	0.75	
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23	
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65	
Chamfer	СН	.009	.017	.024	0.24	0.42	0.60	
Mold Draft Angle Top	α			12°			12°	

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC equivalent: mMO-220

Drawing No. C04-114

## READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

TO: RE:	Technical Publications Manager Reader Response	Total Pages Sent
From	n: Name	
	Company	
	Address	
	City / State / ZIP / Country	
	Telephone: ()	FAX: ()
Appli	ication (optional):	
Wou	ld you like a reply?YN	
Devi	ce: PIC16F87XA	Literature Number: DS39582C
Ques	stions:	
1. V	What are the best features of this document?	
-		
2. H	How does this document meet your hardware and software	re development needs?
_		
- 3. E	Do you find the organization of this document easy to follo	ow? If not, why?
_		
-		
4. V	What additions to the document do you think would enhar	nce the structure and subject?
-		
5. V	What deletions from the document could be made without	affecting the overall usefulness?
6. l	s there any incorrect or misleading information (what and	where)?
-		
7. H	How would you improve this document?	
-		

DS39582C-page 230

### Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

## QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV = ISO/TS 16949=

#### Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rfPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. & KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2001-2013, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 9781620769621

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEEL0Q® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and mulfacture of development systems is ISO 9001:2000 certified.