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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f874a-e-pt

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3.0 DATA EEPROM AND FLASH PROGRAM MEMORY

The data EEPROM and Flash program memory is readable and writable during normal operation (over the full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. These devices have 128 or 256 bytes of data EEPROM (depending on the device), with an address range from 00h to FFh. On devices with 128 bytes, addresses from 80h to FFh are unimplemented and will wraparound to the beginning of data EEPROM memory. When writing to unimplemented locations, the on-chip charge pump will be turned off.

When interfacing the program memory block, the EEDATA and EEDATH registers form a two-byte word that holds the 14-bit data for read/write and the EEADR and EEADRH registers form a two-byte word that holds the 13-bit address of the program memory location being accessed. These devices have 4 or 8K words of program Flash, with an address range from 0000h to 0FFFh for the PIC16F873A/874A and 0000h to 1FFFh for the PIC16F876A/877A. Addresses above the range of the respective device will wraparound to the beginning of program memory.

The EEPROM data memory allows single-byte read and write. The Flash program memory allows single-word reads and four-word block writes. Program memory write operations automatically perform an erase-before-write on blocks of four words. A byte write in data EEPROM memory automatically erases the location and writes the new data (erase-before-write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the data EEPROM memory. Depending on the settings of the write-protect bits, the device may or may not be able to write certain blocks of the program memory; however, reads of the program memory are allowed. When code-protected, the device programmer can no longer access data or program memory; this does NOT inhibit internal reads or writes.

3.1 EEADR and EEADRH

The EEADRH:EEADR register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 8K words of program EEPROM. When selecting a data address value, only the LSByte of the address is written to the EEADR register. When selecting a program address value, the MSByte of the address is written to the EEADRH register and the LSByte is written to the EEADR register.

If the device contains less memory than the full address reach of the address register pair, the Most Significant bits of the registers are not implemented. For example, if the device has 128 bytes of data EEPROM, the Most Significant bit of EEADR is not implemented on access to data EEPROM.

3.2 EECON1 and EECON2 Registers

EECON1 is the control register for memory accesses.

Control bit, EEPGD, determines if the access will be a program or data memory access. When clear, as it is when reset, any subsequent operations will operate on the data memory. When set, any subsequent operations will operate on the program memory.

Control bits, RD and WR, initiate read and write or erase, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write or erase operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write (or erase) operation is interrupted by a $\overline{\text{MCLR}}$ or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit, EEIF in the PIR2 register, is set when the write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the EEPROM write sequence.

Note: The self-programming mechanism for Flash program memory has been changed. On previous PIC16F87X devices, Flash programming was done in single-word erase/ write cycles. The newer PIC18F87XA devices use a four-word erase/write cycle. See Section 3.6 "Writing to Flash Program Memory" for more information.

PIC16F87XA

An example of the complete four-word write sequence is shown in Example 3-4. The initial address is loaded into the EEADRH:EEADR register pair; the four words of data are loaded using indirect addressing.

EXAMPLE 3-4: WRITING TO FLASH PROGRAM MEMORY

; This write routine assumes the following: ; 1. A valid starting address (the least significant bits = '00') is loaded in ADDRH:ADDRL ; 2. The 8 bytes of data are loaded, starting at the address in DATADDR ; 3. ADDRH, ADDRL and DATADDR are all located in shared data memory 0x70 - 0x7f ; BSF STATUS, RP1 ; ; Bank 2 BCF STATUS, RPO ; Load initial address MOVF ADDRH,W MOVWF EEADRH MOVF ADDRL,W ; MOVWF EEADR MOVF DATAADDR,W ; Load initial data address MOVWF FSR ; Load first data byte into lower LOOP MOVF INDF,W MOVWF EEDATA ; INCF FSR,F ; Next byte INDF,W MOVE ; Load second data byte into upper MOVWF EEDATH : INCF FSR,F ; ; Bank 3 STATUS, RPO BSF EECON1, EEPGD BSF ; Point to program memory ; Enable writes BSF EECON1,WREN BCF INTCON, GIE ; Disable interrupts (if using) MOVLW 55h ; Start of required write sequence: MOVWF EECON2 ; Write 55h MOVLW AAh ; Write AAh MOVWF EECON2 BSF EECON1,WR ; Set WR bit to begin write NOP ; Any instructions here are ignored as processor ; halts to begin write sequence NOP ; processor will stop here and wait for write complete ; after write processor continues with 3rd instruction EECON1,WREN BCF ; Disable writes INTCON, GIE ; Enable interrupts (if using) BSF BCF STATUS, RPO ; Bank 2 INCF EEADR, F ; Increment address ; Check if lower two bits of address are `00' MOVF EEADR,W ANDLW ; Indicates when four words have been programmed 0x03 XORLW 0x03 ; BTFSC STATUS,Z ; Exit if more than four words, GOTO ; Continue if less than four words LOOP

4.6 Parallel Slave Port

The Parallel Slave Port (PSP) is not implemented on the PIC16F873A or PIC16F876A.

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port, when control bit PSPMODE (TRISE<4>) is set. In Slave mode, it is asynchronously readable and writable by the external world through RD control input pin, RE0/RD/AN5, and WR control input pin, RE1/WR/AN6.

The PSP can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD/AN5 to be the RD input, RE1/WR/AN6 to be the WR input and RE2/CS/AN7 to be the CS (Chip Select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set). The A/D port configuration bits, PCFG3:PCFG0 (ADCON1<3:0>), must be set to configure pins RE2:RE0 as digital I/O.

There are actually two 8-bit latches: one for data output and one for data input. The user writes 8-bit data to the PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the external device is controlling the direction of data flow.

A write to the PSP occurs when both the \overline{CS} and \overline{WR} lines are first detected low. When either the \overline{CS} or \overline{WR} lines become high (level triggered), the Input Buffer Full (IBF) status flag bit (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 4-11). The interrupt flag bit, PSPIF (PIR1<7>), is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The Input Buffer Overflow (IBOV) status flag bit (TRISE<5>) is set if a second write to the PSP is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the CS and RD lines are first detected low. The Output Buffer Full (OBF) status flag bit (TRISE<6>) is cleared immediately (Figure 4-12), indicating that the PORTD latch is waiting to be read by the external bus. When either the CS or RD pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware. When not in PSP mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).





6.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit, TMR1IE (PIE1<0>).

Timer1 can operate in one of two modes:

- As a Timer
- As a Counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit, TMR1ON (T1CON<0>).

Timer1 also has an internal "Reset input". This Reset can be generated by either of the two CCP modules (Section 8.0 "Capture/Compare/PWM Modules"). Register 6-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI/CCP2 and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the PIC[®] Mid-Range MCU Family Reference Manual (DS33023).

V-1.				LOIDIEN	ADDICESS I	011)					
	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	—	_	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N			
	bit 7							bit 0			
	Unimplem	ented: Rea	ad as '0'								
	T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits										
	11 = 1:8 pr	escale valu	le								
	10 = 1.4 pr 01 = 1.2 pr	escale valu escale valu	ie Ie								
	00 = 1:1 pr	escale valu	ie								
	T10SCEN:	Timer1 Os	scillator Enal	ble Control b	it						
	1 = Oscillat	or is enable	ed								
	0 = Oscillat	or is shut-o	off (the oscill	ator inverter	is turned off to	eliminate p	ower drain)			
	T1SYNC: T	ïmer1 Exte	ernal Clock I	nput Synchro	onization Contro	ol bit					
	<u>When TMR</u>	When TMR1CS = 1:									
	1 = Do not	1 = Do not synchronize external clock input									
	0 = Synchronic	onize exter	nai ciock inp	but							
	This bit is it	$\frac{105 = 0}{100}$	ner1 uses th	e internal clo	ck when TMR1	ICS = 0.					
	TMR1CS: 1	- Fimer1 Cloo	ck Source S	elect bit							
	1 = Externa	al clock fror	n pin RC0/T	10SO/T1CK	I (on the rising	edge)					
	0 = Internal	l clock (Fos	sc/4)								
	TMR1ON:	Timer1 On	bit								
	1 = Enables	s Timer1									
	0 = Stops T	ïmer1									
	Legend:										
	R = Readal	ble bit	VV = V	Vritable bit	U = Unimple	emented b	it, read as '	0'			
	- n = Value	at POR	'1' = E	Bit is set	'0' = Bit is c	leared	x = Bit is u	nknown			

REGISTER 6-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

8.3.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 register.
- 2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
- 3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
- 4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
- 5. Configure the CCP1 module for PWM operation.

TABLE 8-3:	EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFFh	0xFFh	0xFFh	0x3Fh	0x1Fh	0x17h
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 8-4:	REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on: BOR	Valu all o Res	e on other sets
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
0Dh	PIR2	_	_	—	—		_		CCP2IF		0		0
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
8Dh	PIE2		_	—	—	-	—	_	CCP2IE		0		0
87h	TRISC	PORTC D	PORTC Data Direction Register										1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register									xxxx	uuuu	uuuu
0Fh	TMR1H	Holding R	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register									uuuu	uuuu
10h	T1CON		—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)									xxxx	uuuu	uuuu
16h	CCPR1H	Capture/C	Capture/Compare/PWM Register 1 (MSB)								xxxx	uuuu	uuuu
17h	CCP1CON	_		CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	00	0000	00	0000
1Bh	CCPR2L	Capture/Compare/PWM Register 2 (LSB)									xxxx	uuuu	uuuu
1Ch	CCPR2H	Capture/C	Compare/F	PWM Regis	ter 2 (MSB)					xxxx	xxxx	uuuu	uuuu
1Dh	CCP2CON		—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	00	0000	00	0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

Note 1: The PSP is not implemented on 28-pin devices; always maintain these bits clear.

9.3.3 ENABLING SPI I/O

To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON registers and then set the SSPEN bit. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed. That is:

- SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> bit cleared
- SCK (Master mode) must have TRISC<3> bit cleared
- SCK (Slave mode) must have TRISC<3> bit set
- SS must have TRISC<4> bit set

Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

9.3.4 TYPICAL CONNECTION

Figure 9-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data Slave sends dummy data
- Master sends data Slave sends data
- Master sends dummy data Slave sends data



FIGURE 9-2: SPI MASTER/SLAVE CONNECTION

9.3.5 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 9-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "Line Activity Monitor" mode.

The clock polarity is selected by appropriately programming the CKP bit (SSPCON<4>). This then, would give waveforms for SPI communication as shown in Figure 9-3, Figure 9-5 and Figure 9-6, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum data rate (at 40 MHz) of 10.00 Mbps.

Figure 9-3 shows the waveforms for Master mode. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.



FIGURE 9-3: SPI MODE WAVEFORM (MASTER MODE)

9.4.3.2 Reception

When the R/\overline{W} bit of the address byte is clear and an address match occurs, the R/\overline{W} bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and the SDA line is held low (ACK).

When the address byte overflow condition exists, then the No Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set or bit SSPOV (SSPCON<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPCON<0> = 1), RC3/SCK/SCL will be held low (clock stretch) following each data transfer. The clock must be released by setting bit CKP (SSPCON<4>). See **Section 9.4.4** "**Clock Stretching**" for more detail.

9.4.3.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and pin RC3/SCK/SCL is held low regardless of SEN (see **Section 9.4.4 "Clock Stretching"** for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 9-9).

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not ACK), then the data transfer is complete. In this case, when the ACK is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the Start bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSPBUF register. Again, pin RC3/SCK/SCL must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

9.4.10 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the Buffer Full flag bit, BF, and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time specification, parameter #106). SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time specification, parameter #107). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time, if an address match occurred or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPIF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 9-21).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL, until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will deassert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

9.4.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all eight bits are shifted out.

9.4.10.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

9.4.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge $(\overline{ACK} = 0)$ and is set when the slave does Not Acknowledge $(\overline{ACK} = 1)$. A slave sends an Acknowledge when it has recognized its address (including a general call) or when the slave has properly received its data.

9.4.11 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN (SSPCON2<3>).

Note: The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high to low/ low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state, awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable bit, ACKEN (SSPCON2<4>).

9.4.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

9.4.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

9.4.11.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

10.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit, SYNC (TXSTA<4>). In addition, enable bit, SPEN (RCSTA<7>), is set in order to configure the RC6/TX/CK and RC7/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit, CSRC (TXSTA<7>).

10.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 10-6. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit, TXIF (PIR1<4>), is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a readonly bit which is set when the TSR is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory so it is not available to the user.

Transmission is enabled by setting enable bit, TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 10-9). The transmission can also be started by first loading the TXREG register and then setting bit TXEN (Figure 10-10). This is advantageous when slow baud rates are selected since the BRG is kept in Reset when bits TXEN, CREN and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally, when transmission is first started, the TSR register is empty so a transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to highimpedance. If either bit CREN or bit SREN is set during a transmission, the transmission is aborted and the DT pin reverts to a high-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic, however, is not reset, although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting since bit TXEN is still set. The DT line will immediately switch from High-Impedance Receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the "new" TX9D, the "present" value of bit TX9D is loaded.

Steps to follow when setting up a Synchronous Master Transmission:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 10.1 "USART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. If interrupts are desired, set enable bit TXIE.
- 4. If 9-bit transmission is desired, set bit TX9.
- 5. Enable the transmission by setting bit TXEN.
- 6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- 7. Start transmission by loading data to the TXREG register.
- 8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

11.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 11-2. The source impedance (Rs) and the internal sampling switch impedance (Rss) directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD); see Figure 11-2. The maximum recommended impedance for analog sources is 2.5 k Ω . As the impedance is decreased, the acquisition time may be

EQUATION 11-1: ACQUISITION TIME

decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 11-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the PIC[®] Mid-Range MCU Family Reference Manual (DS33023).

	TACQ	= Amplifier Settling Time + Hold Capacitor Charging Time + Temperature Coefficient
= TAMP + TC + TCOFF = 2 µs + TC + [(Temperature - 25°C)(0.05 µs/°C)] TC = CHOLD (RIC + RSS + RS) In(1/2047) = - 120 pF (1 kΩ + 7 kΩ + 10 kΩ) In(0.0004885) = 16.47 µs TACQ = 2 µs + 16.47 µs + [(50°C - 25°C)(0.05 µs/°C) = 19.72 µs	TC Tacq	= TAMP + TC + TCOFF = $2 \mu s + TC + [(Temperature - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ = CHOLD (RIC + RSS + RS) In(1/2047) = $-120 \text{ pF} (1 \text{ k}\Omega + 7 \text{ k}\Omega + 10 \text{ k}\Omega) \text{ In}(0.0004885)$ = $16.47 \mu s$ = $2 \mu s + 16.47 \mu s + [(50^{\circ}C - 25^{\circ}C)(0.05 \mu s/^{\circ}C)]$ = $19.72 \mu s$

Note 1: The reference voltage (VREF) has no effect on the equation since it cancels itself out.

- 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.
- **3:** The maximum recommended impedance for analog sources is 2.5 k Ω . This is required to meet the pin leakage specification.





PIC16F87XA

CONFIGURATION WORD (ADDRESS 2007h)⁽¹⁾ REGISTER 14-1: R/P-1 U-0 **R/P-1** R/P-1 R/P-1 R/P-1 R/P-1 **R/P-1** U-0 U-0 **R/P-1** R/P-1 **R/P-1** R/P-1 CP DEBUG WRT1 WRT0 CPD PWRTEN WDTEN Fosc1 LVP BOREN Fosc0 bit 13 bit0 bit 13 CP: Flash Program Memory Code Protection bit 1 = Code protection off0 = All program memory code-protected bit 12 Unimplemented: Read as '1' DEBUG: In-Circuit Debugger Mode bit bit 11 1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins 0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger bit 10-9 WRT1:WRT0 Flash Program Memory Write Enable bits For PIC16F876A/877A: 11 = Write protection off; all program memory may be written to by EECON control 10 = 0000h to 00FFh write-protected; 0100h to 1FFFh may be written to by EECON control 01 = 0000h to 07FFh write-protected; 0800h to 1FFFh may be written to by EECON control 00 = 0000h to 0FFFh write-protected; 1000h to 1FFFh may be written to by EECON control For PIC16F873A/874A: 11 = Write protection off; all program memory may be written to by EECON control 10 = 0000h to 00FFh write-protected; 0100h to 0FFFh may be written to by EECON control 01 = 0000h to 03FFh write-protected; 0400h to 0FFFh may be written to by EECON control 00 = 0000h to 07FFh write-protected; 0800h to 0FFFh may be written to by EECON control bit 8 CPD: Data EEPROM Memory Code Protection bit 1 = Data EEPROM code protection off 0 = Data EEPROM code-protected bit 7 LVP: Low-Voltage (Single-Supply) In-Circuit Serial Programming Enable bit 1 = RB3/PGM pin has PGM function; low-voltage programming enabled 0 = RB3 is digital I/O, HV on MCLR must be used for programming bit 6 BOREN: Brown-out Reset Enable bit 1 = BOR enabled0 = BOR disabled Unimplemented: Read as '1' bit 5-4 **PWRTEN:** Power-up Timer Enable bit bit 3 1 = PWRT disabled 0 = PWRT enabled bit 2 WDTEN: Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled Fosc1:Fosc0: Oscillator Selection bits bit 1-0 11 = RC oscillator 10 = HS oscillator 01 = XT oscillator 00 = LP oscillator Legend:

R = Readable bit P = Programmable bit

U = Unimplemented bit, read as '0'

n = Value when device is unprogrammed

u = Unchanged from programmed state

Note 1: The erased (unprogrammed) value of the Configuration Word is 3FFFh.

14.4 MCLR

PIC16F87XA devices have a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

The behavior of the ESD protection on the MCLR pin differs from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both Resets and current consumption outside of device specification during the Reset event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RCR network, as shown in Figure 14-5, is suggested.

FIGURE 14-5: RECOMMENDED MCLR CIRCUIT



14.5 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected (in the range of <u>1.2V-1.7V</u>). To take advantage of the POR, tie the MCLR pin to VDD through an RC network, as described in **Section 14.4** "**MCLR**". A maximum rise time for VDD is specified. See **Section 17.0** "**Electrical Characteristics**" for details.

When the device starts normal operation (exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. Brown-out Reset may be used to meet the start-up conditions. For additional information, refer to application note, *AN607, "Power-up Trouble Shooting*" (DS00607).

14.6 Power-up Timer (PWRT)

The Power-up Timer provides a fixed 72 ms nominal time-out on power-up only from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in Reset as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable or disable the PWRT.

The power-up time delay will vary from chip to chip due to VDD, temperature and process variation. See **Section 17.0 "Electrical Characteristics"** for details (TPWRT, parameter #33).

14.7 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a delay of 1024 oscillator cycles (from OSC1 input) after the PWRT delay is over (if PWRT is enabled). This helps to ensure that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from Sleep.

14.8 Brown-out Reset (BOR)

The configuration bit, BODEN, can enable or disable the Brown-out Reset circuit. If VDD falls below VBOR (parameter D005, about 4V) for longer than TBOR (parameter #35, about 100 μ S), the brown-out situation will reset the device. If VDD falls below VBOR for less than TBOR, a Reset may not occur.

Once the brown-out occurs, the device will remain in Brown-out Reset until VDD rises above VBOR. The Power-up Timer then keeps the device in Reset for TPWRT (parameter #33, about 72 mS). If VDD should fall below VBOR during TPWRT, the Brown-out Reset process will restart when VDD rises above VBOR with the Power-up Timer Reset. The Power-up Timer is always enabled when the Brown-out Reset circuit is enabled, regardless of the state of the PWRT configuration bit.

14.9 Time-out Sequence

On power-up, the time-out sequence is as follows: the PWRT delay starts (if enabled) when a POR Reset occurs. Then, OST starts counting 1024 oscillator cycles when PWRT ends (LP, XT, HS). When the OST ends, the device comes out of Reset.

If MCLR is kept low long enough, the time-outs will expire. Bringing MCLR high will begin execution immediately. This is useful for testing purposes or to synchronize more than one PIC16F87XA device operating in parallel.

Table 14-5 shows the Reset conditions for the Status, PCON and PC registers, while Table 14-6 shows the Reset conditions for all the registers.

SWAPF	Swap Nibbles in f
Syntax:	[label] SWAPF f,d
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in register 'f'.

XORWF	Exclusive OR W with f						
Syntax:	[label] XORWF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$						
Operation:	(W) .XOR. (f) \rightarrow (destination)						
Status Affected:	Z						
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.						

XORLW	Exclusive OR Literal with W						
Syntax:	[<i>label</i>] XORLW k						
Operands:	$0 \leq k \leq 255$						
Operation:	(W) .XOR. $k \rightarrow (W)$						
Status Affected:	Z						
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.						

16.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/
 - MPLIB[™] Object Librarian
 - MPLAB C30 C Compiler
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- MPLAB dsPIC30 Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
 - PICSTART[®] Plus Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™] 1 Demonstration Board
 - PICDEM.net[™] Demonstration Board
 - PICDEM 2 Plus Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 4 Demonstration Board
 - PICDEM 17 Demonstration Board
 - PICDEM 18R Demonstration Board
 - PICDEM LIN Demonstration Board
 - PICDEM USB Demonstration Board
- Evaluation Kits
 - KEELOQ[®]
 - PICDEM MSC
 - microID[®]
 - CAN
 - PowerSmart[®]
 - Analog

16.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows[®] based application that contains:

- · An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help
- The MPLAB IDE allows you to:
- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files (assembly or C)
 - absolute listing file (mixed assembly and C)
 - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

16.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

PIC16F87XA

NOTES:

17.1 DC Characteristics: PIC16F873A/874A/876A/877A (Industrial, Extended) PIC16LF873A/874A/876A/877A (Industrial) (Continued)

PIC16LF8 (Indust	73A/874A trial)	/876A/877A	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial						
PIC16F873A/874A/876A/877A (Industrial, Extended)			Standa Opera	Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for extended					
Param No.	Symbol	Characteristic/ Device	Min	Тур†	Max	Units	Conditions		
-	IDD	Supply Current ^(2,5)							
D010		16LF87XA	—	0.6	2.0	mA	XT, RC osc configurations, Fosc = 4 MHz, VDD = 3.0V		
D010		16F87XA		1.6	4	mA	XT, RC osc configurations, FOSC = 4 MHz, VDD = 5.5V		
D010A		16LF87XA	_	20	35	μA	LP osc configuration, Fosc = 32 kHz, VDD = 3.0V, WDT disabled		
D013		16F87XA	—	7	15	mA	HS osc configuration, Fosc = 20 MHz, VDD = 5.5V		
D015	Δ IBOR	Brown-out Reset Current ⁽⁶⁾	_	85	200	μA	BOR enabled, VDD = 5.0V		

Legend: Rows with standard voltage device data only are shaded for improved readability.

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

- **Note 1:** This is the limit to which VDD can be lowered without losing RAM data.
 - 2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading, switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.
 - The test conditions for all IDD measurements in active operation mode are:
 - OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
 - \overline{MCLR} = VDD; WDT enabled/disabled as specified.
 - **3:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD and Vss.
 - 4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.
 - **5:** Timer1 oscillator (when enabled) adds approximately 20 μA to the specification. This value is from characterization and is for design guidance only. This is not tested.
 - 6: The ∆ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.
 - 7: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.





Param No.	Symbol	Characteristic			Min	Тур†	Max	Units	Conditions	
40*	TT0H	T0CKI High Pulse Width		No Prescaler	0.5 Tcy + 20	—	_	ns	Must also meet	
				With Prescaler	10	_	—	ns	parameter 42	
41*	TT0L T0CKI Low Pulse		Width	No Prescaler	0.5 Tcy + 20	_	—	ns	Must also meet	
				With Prescaler	10	_	—	ns	parameter 42	
42*	Тт0Р	T0CKI Period		No Prescaler	Tcy + 40	—	—	ns		
				With Prescaler	Greater of:	—	—	ns	N = prescale value	
					20 or <u>Tcy + 40</u> N				(2, 4,, 256)	
45*	T⊤1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5 TCY + 20		_	ns	Must also meet	
			Synchronous, Prescaler = 2, 4, 8	Standard(F)	15		_	ns	parameter 47	
				Extended(LF)	25	Ι	—	ns		
			Asynchronous	Standard(F)	30	—	—	ns		
				Extended(LF)	50	Ι	—	ns		
46*	TT1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5 TCY + 20			ns	Must also meet	
			Synchronous, Prescaler = 2, 4, 8	Standard(F)	15	—		ns	parameter 47	
1				Extended(LF)	25	—	—	ns		
			Asynchronous	Standard(F)	30	—	—	ns		
				Extended(LF)	50			ns		
47*	TT1P	T1CKI Input Period	Synchronous	Standard(F)	Greater of: 30 or <u>Tcʏ + 40</u> N	—	—	ns	N = prescale value (1, 2, 4, 8)	
				Extended(LF)	Greater of: 50 or <u>Tcʏ + 40</u> N				N = prescale value (1, 2, 4, 8)	
			Asynchronous	Standard(F)	60	—	_	ns		
				Extended(LF)	100		_	ns		
	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCE)			DC		200	kHz		
48	TCKEZTMR1	Delay from Extern	Delay from External Clock Edge to Timer Increment			—	7 Tosc	_		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	INCHES			MILLIMETERS*			
Dimension	MIN	NOM	MAX	MIN	NOM	MAX		
Number of Pins	n		44			44		
Pitch	р		.031			0.80		
Pins per Side	n1		11			11		
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20	
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05	
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15	
Foot Length	L	.018	.024	.030	0.45	0.60	0.75	
Footprint (Reference)	(F)		.039		1.00			
Foot Angle	¢	0	3.5	7	0	3.5	7	
Overall Width	E	.463	.472	.482	11.75	12.00	12.25	
Overall Length	D	.463	.472	.482	11.75	12.00	12.25	
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10	
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10	
Lead Thickness	С	.004	.006	.008	0.09	0.15	0.20	
Lead Width	В	.012	.015	.017	0.30	0.38	0.44	
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-026 Drawing No. C04-076

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RB5 Pin	
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RB7/PGD Pin	
RC0/T1OSO/T1CKI Pin	9, 12
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