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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	33
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	368 × 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f877a-i-l

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software
RB0/INT	21	18		TTI /ST(1)	
RB0	21	10	I/O	112/01	Digital I/O.
INT			I.		External interrupt.
RB1	22	19	I/O	TTL	Digital I/O.
RB2	23	20	I/O	TTL	Digital I/O.
RB3/PGM	24	21		TTL	
RB3			I/O		Digital I/O.
PGM			I		Low-voltage (single-supply) ICSP programming enable pin.
RB4	25	22	I/O	TTL	Digital I/O.
RB5	26	23	I/O	TTL	Digital I/O.
RB6/PGC	27	24		TTL/ST ⁽²⁾	
RB6			I/O		Digital I/O.
PGC			I		In-circuit debugger and ICSP programming clock.
RB7/PGD	28	25		TTL/ST ⁽²⁾	
RB7			I/O		Digital I/O.
PGD			I/O		In-circuit debugger and ICSP programming data.
					PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	11	8		ST	
RC0			1/0		Digital I/O.
TICKI					Timer1 oscillator output.
	12	0	'	ет	
RC1	12	3	1/0	51	Digital I/O
TIOSI			", U		Timer1 oscillator input.
CCP2			I/O		Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1	13	10		ST	
RC2			I/O		Digital I/O.
CCP1			I/O		Capture1 input, Compare1 output, PWM1 output.
RC3/SCK/SCL	14	11		ST	
RC3			1/0		Digital I/O.
SCI			1/0		Synchronous serial clock input/output for SPI mode.
	15	12	1/0	ST	Cynonionous senar block input output for 1 e mode.
RC4	15	12	I/O	01	Digital I/O.
SDI			I		SPI data in.
SDA			I/O		I ² C data I/O.
RC5/SDO	16	13		ST	
RC5			I/O		Digital I/O.
SDO			0		SPI data out.
RC6/TX/CK	17	14		ST	
RC6 TY			1/0		Digital I/O.
CK			1/0		USART1 synchronous clock.
RC7/RX/DT	18	15		ST	· · · · · · · · · · · · · · · · · · ·
RC7			I/O		Digital I/O.
RX			I		USART asynchronous receive.
DT			I/O		USART synchronous data.
Vss	8, 19	5, 6	Р	—	Ground reference for logic and I/O pins.
Vdd	20	17	Р	_	Positive supply for logic and I/O pins.
Legend: I = input — = Not u	O = ou used TTL =	itput TTL inp	I/O ut ST	= input/outpu = Schmitt Trig	t P = power gger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

2.0 MEMORY ORGANIZATION

There are three memory blocks in each of the PIC16F87XA devices. The program memory and data memory have separate buses so that concurrent access can occur and is detailed in this section. The EEPROM data memory block is detailed in **Section 3.0 "Data EEPROM and Flash Program Memory"**.

Additional information on device memory may be found in the PIC[®] Mid-Range MCU Family Reference Manual (DS33023).



FIGURE 2-1: PIC16F876A/877A PROGRAM MEMORY MAP AND STACK

2.1 Program Memory Organization

The PIC16F87XA devices have a 13-bit program counter capable of addressing an 8K word x 14 bit program memory space. The PIC16F876A/877A devices have 8K words x 14 bits of Flash program memory, while PIC16F873A/874A devices have 4K words x 14 bits. Accessing a location above the physically implemented address will cause a wraparound.

The Reset vector is at 0000h and the interrupt vector is at 0004h.



2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains various enable and flag bits for the TMR0 register overflow, RB port change and external RB0/INT pin interrupts. Note: Interrupt flag bits are set when an interrupt condition occurs regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

	R/W-0	R/W-0	、 R/W-0	R/W-0	R/W-0	, R/W-0	R/W-0	R/W-x			
	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF			
	bit 7							bit 0			
bit 7	GIE: Globa	al Interrupt E	Enable bit								
	1 = Enable 0 = Disable	s all unmas s all interru	ked interrupt pts	S							
bit 6	PEIE: Perip	oheral Interi	upt Enable b	bit							
	1 = Enable 0 = Disable	s all unmas s all periph	ked peripher eral interrupt	al interrupts ts	i						
bit 5	TMR0IE: T	MR0 Overfl	ow Interrupt	Enable bit							
	1 = Enable 0 = Disable	s the TMR0 es the TMR0	interrupt) interrupt								
bit 4	INTE: RB0	/INT Extern	al Interrupt E	nable bit							
	1 = Enable 0 = Disable	s the RB0/I es the RB0/I	NT external i NT external	nterrupt interrupt							
bit 3	RBIE: RB I	Port Change	e Interrupt Er	nable bit							
	1 = Enable 0 = Disable	s the RB po the RB po	ort change in ort change in	terrupt iterrupt							
bit 2	TMR0IF: TMR0 Overflow Interrupt Flag bit										
	1 = TMR0 0 = TMR0	register has register did	overflowed not overflow	(must be cle	eared in soft	ware)					
bit 1	INTF: RB0/	/INT Externa	al Interrupt F	lag bit							
	1 = The RE 0 = The RE	30/INT exter 30/INT exter	rnal interrupt rnal interrupt	occurred (n did not occ	nust be clea ur	red in softwa	are)				
bit 0	RBIF: RB F	Port Change	e Interrupt Fla	ag bit							
	 1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software). 										
	0 = None (of the RB7:I	RB4 pins hav	ve changed	state						
	D Doodo	hla hit	10/ 10/	ritable bit	منمال ا	aplomented	hit road oo	·^'			

3						
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'				
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown			

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
09h	PORTE		—	_	—	—	RE2	RE1	RE0	xxx	uuu
89h	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction bits		0000 -111	0000 -111	
9Fh	ADCON1	ADFM	ADCS2		—	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	00 0000

TABLE 4-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

REGISTER 4-1: TRISE REGISTER (ADDRESS 89h)

R-0	R-0	R/W-0	R/W-0	U-0	R/W-1	R/W-1	R/W-1
IBF	OBF	IBOV	PSPMODE	—	Bit 2	Bit 1	Bit 0
bit 7							bit 0

Parallel Slave Port Status/Control Bits:

bit 7	IBF: Input Buffer Full Sta	atus bit		
	1 = A word has been red	ceived and is waiting to	be read by the CPU	
	0 = No word has been re	eceived		
bit 6	OBF : Output Buffer Full	Status bit		
	1 = The output buffer sti	ll holds a previously wr	itten word	
	0 = The output buffer ha	s been read		
bit 5	IBOV: Input Buffer Over	flow Detect bit (in Micr	oprocessor mode)	
	1 = A write occurred w software)	hen a previously input	word has not been re	ead (must be cleared in
	0 = No overflow occurre	ed		
bit 4	PSPMODE: Parallel Sla	ve Port Mode Select bi	t	
	1 = PORTD functions in	Parallel Slave Port mo	de	
	0 = PORTD functions in	general purpose I/O m	ode	
bit 3	Unimplemented: Read	as '0'		
	PORTE Data Direction	Bits:		
bit 2	Bit 2: Direction Control b	oit for pin RE2/CS/AN7		
	1 = Input			
	0 = Output			
bit 1	Bit 1: Direction Control b	pit for pin RE1/WR/AN6	6	
	1 = Input			
	0 = Output			
bit 0	Bit 0: Direction Control b	oit for pin RE0/RD/AN5		
	1 = Input			
	0 = Output			
	Legend:			
	R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
	- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.6 Parallel Slave Port

The Parallel Slave Port (PSP) is not implemented on the PIC16F873A or PIC16F876A.

PORTD operates as an 8-bit wide Parallel Slave Port, or microprocessor port, when control bit PSPMODE (TRISE<4>) is set. In Slave mode, it is asynchronously readable and writable by the external world through RD control input pin, RE0/RD/AN5, and WR control input pin, RE1/WR/AN6.

The PSP can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD/AN5 to be the RD input, RE1/WR/AN6 to be the WR input and RE2/CS/AN7 to be the CS (Chip Select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set). The A/D port configuration bits, PCFG3:PCFG0 (ADCON1<3:0>), must be set to configure pins RE2:RE0 as digital I/O.

There are actually two 8-bit latches: one for data output and one for data input. The user writes 8-bit data to the PORTD data latch and reads data from the port pin latch (note that they have the same address). In this mode, the TRISD register is ignored since the external device is controlling the direction of data flow.

A write to the PSP occurs when both the \overline{CS} and \overline{WR} lines are first detected low. When either the \overline{CS} or \overline{WR} lines become high (level triggered), the Input Buffer Full (IBF) status flag bit (TRISE<7>) is set on the Q4 clock cycle, following the next Q2 cycle, to signal the write is complete (Figure 4-11). The interrupt flag bit, PSPIF (PIR1<7>), is also set on the same Q4 clock cycle. IBF can only be cleared by reading the PORTD input latch. The Input Buffer Overflow (IBOV) status flag bit (TRISE<5>) is set if a second write to the PSP is attempted when the previous byte has not been read out of the buffer.

A read from the PSP occurs when both the CS and RD lines are first detected low. The Output Buffer Full (OBF) status flag bit (TRISE<6>) is cleared immediately (Figure 4-12), indicating that the PORTD latch is waiting to be read by the external bus. When either the CS or RD pin becomes high (level triggered), the interrupt flag bit PSPIF is set on the Q4 clock cycle, following the next Q2 cycle, indicating that the read is complete. OBF remains low until data is written to PORTD by the user firmware. When not in PSP mode, the IBF and OBF bits are held clear. However, if flag bit IBOV was previously set, it must be cleared in firmware.

An interrupt is generated and latched into flag bit PSPIF when a read or write operation is completed. PSPIF must be cleared by the user in firmware and the interrupt can be disabled by clearing the interrupt enable bit PSPIE (PIE1<7>).





7.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time base for the PWM mode of the CCP module(s). The TMR2 register is readable and writable and is cleared on any device Reset.

The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit, TMR2IF (PIR1<1>)).

Timer2 can be shut-off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

Register 7-1 shows the Timer2 Control register.

Additional information on timer modules is available in the PIC[®] Mid-Range MCU Family Reference Manual (DS33023).

FIGURE 7-1: TIMER2 BLOCK DIAGRAM



REGISTER 7-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

\ <i>1</i> -1.	120011.1			EGISTER	ADDRESS	, 1211)					
	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0			
	bit 7							bit 0			
bit 7	Unimplen	n ented: Rea	d as '0'								
bit 6-3	TOUTPS3	:TOUTPS0:	Timer2 Out	put Postscal	e Select bits	5					
	0000 = 1: 0001 = 1: 0010 = 1:	0000 = 1:1 postscale 0001 = 1:2 postscale 0010 = 1:3 postscale									
	•	•									
	•										
	• 1111 = 1:	16 postscale	J								
bit 2	TMR2ON:	Timer2 On I	bit								
	1 = Timer2 0 = Timer2	2 is on 2 is off									
bit 1-0	T2CKPS1	:T2CKPS0:	Timer2 Cloc	k Prescale S	Select bits						
	00 = Pres 01 = Pres 1x = Pres	caler is 1 caler is 4 caler is 16									
	Legend:										
	R = Reada	able bit	W = V	Vritable bit	U = Unim	nplemented	bit, read as	'0'			
	- n = Value	e at POR	'1' = E	Bit is set	'0' = Bit i	s cleared	x = Bit is u	Inknown			

9.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

9.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C)
 - Full Master mode
 - Slave mode (with general address call)

The I²C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode

9.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON and SSPCON2). The use of these registers and their individual configuration bits differ significantly, depending on whether the MSSP module is operated in SPI or I^2C mode.

Additional details are provided under the individual sections.

9.3 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RC5/SDO
- Serial Data In (SDI) RC4/SDI/SDA
- Serial Clock (SCK) RC3/SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

Slave Select (SS) – RA5/AN4/SS/C2OUT

Figure 9-1 shows the block diagram of the MSSP module when operating in SPI mode.

FIGURE 9-1:

MSSP BLOCK DIAGRAM (SPI MODE)



Note:	When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = 0100), the state of the \overline{SS} pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP mod- ule in PORTC controls the state that is read back from the TRISC<5> bit (see Section 4.3 "PORTC and the TRISC
	Register" for information on PORTC). If
	BSF, are performed on the TRISC register
	while the \overline{SS} pin is high, this will cause the
	TRISC<5> bit to be set, thus disabling the
	SDO output.

R/W-0R-0R-0R-0R-0R-0R-0R-0R-0SMPC/RED/APSR/WUABFbit 7bit 7bit 0bit 7SMP: Slew Rate Control bitInMaster or Slave mode:1 = Slew rate control disabled for high-speed mode (100 kHz and 1 MHz)0 = Slew rate control enabled for high-speed mode (400 kHz)bit 6CKE: SMBus Select bit1 = Enable SMBus specific inputs0 = Disable SMBus specific inputs0 = Disable SMBus specific inputs0 = Disable SMBus specific inputs1 = Enable SMBus specific inputs0 = Dicate/SMBus specific inputs0 = Dicate/SMBus specific inputs0 = Dicate/SMBus specific inputs0 = Dicate/SMBus specific inputs1 = Indicates that the last byte received or transmitted was data1 = Indicates that a last byte received or transmitted was addressbit 4P: Stop bit1 = Indicates that a Stop bit has been detected last0 = Sicp bit was not detected lastNote:Note:1 = Read1 = Read0 = WriteNote:1 = Fransmit is in progressNote:1 = Transmit is not in progressNote:1 = Readver mode:1 = Readver mode:1 = Receive nonplete, SSPBUF is full0 = Roceive not complete, SSPBUF is full<	REGISTER 9-3:	SSPSTAT:	: MSSP STA	STATUS REGISTER (I ² C MODE) (ADDRESS 94h)						
SMP CKE D/A P S R/W UA BF bit 7 bit 7 bit 0 bit 0 bit 0 bit 7 SMP: Slew Rate Control bit In Master or Slave mode: 1 = Slew rate control disabled for standard speed mode (400 kHz and 1 MHz) 0 = Slew rate control disabled for high-speed mode (400 kHz) bit 0 bit 6 CKE: SMBus Select bit In Master or Slave mode: 1 = Indicates that support of the specific inputs 0 = Disable SMBus specific inputs 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that a Stop bit has been detected last 0 = Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last 0 = Start bit was not detected last 0 = Write Note: This bit is bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not ACK bit. InMaster mode: 1 = Transmit is not in progress 0 = Transmit is not in progress 0 = Transmit set on the regress (10-bit Stave mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated bit address in the SSPADD register 0 = Address does not need to be update the ad		R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	
bit 7 bit 0 bit 7 SMP: Slew Rate Control bit In Master or Slave mode: 1 = Slave mode: 1 = Slew rate control enabled for high-speed mode (400 kHz) 0 = Slew rate control enabled for high-speed mode (400 kHz) 0 = Slew rate control enabled for high-speed mode (400 kHz) bit 6 CKE: SMBus Select bit In Master or Slave mode: 1 = Enable SMBus specific inputs 0 = Disable SMBus specific inputs 0 = Disable SMBus specific inputs 1 = Indicates bit In Master mode: Reserved. In Slave mode: 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was address bit 4 bit 7 P: Stop bit 1 = Indicates that the last byte received or transmitted was address 0 = Jondo at the last byte received or transmitted was address 0 = Jondo at the last byte received or transmitted was address 0 = Start bit 1 = Indicates that a Stop bit has been detected last 0 = Start bit 1 = Indicates that a Start bit has been detected last 0 = Start bit 1 = Indicates that a Start bit has been detected last 0 = Start bit was not detected last Note: This bit is cleared on Reset and when SSPEN is cleared. bit 2 bit 2 RWF: Read/Wittle bit information (I ² C mode only) In Slave mode: 1 = Read 0 = Write Note: This bit holds the RW bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not AGK bit. In Master mode: 1 = Transmit is not in progress 0 = Transmit is not in progress 0 = Transmit is not in progress 0 = Address does not need to buydated bit 0 bit 1 US: Ubit Slave mode only) 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to buydated bit 0 bit 1 US: Ubit Slave bit In Transmit mode: 1 = Receive n		SMP	CKE	D/A	Р	S	R/W	UA	BF	
bit 7 SMP: Slew Rate Control bit In Master or Slave mode: 1 = Slew rate control enabled for high-speed mode (100 kHz and 1 MHz) 0 = Slew rate control enabled for high-speed mode (400 kHz) bit 6 CKE: SMBus Select bit In Master of Slave mode: 1 = Enable SMBus specific inputs 0 = Disable SMBus specific inputs 0 = Dinable SMBus specific inputs 0 = Dindicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that a Stop bit has been detected last 1 = Indicates that a Stop bit has been detected last 1 = Indicates that a Start bit has been detected last 1 = Indicates that a Start bit has been detected last 1 = Indicates that a Start bit has been detected last 1 = Read 0 = SWrite Note: This bit is cleared on Reset and when SSPEN is cleared. bit 2 RWR: Read/Write bit information (I ² C mode only) In Slave mode: 1 = Read 0 = Write Note: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in India mode: 1 = Transmit is not in progress Note: ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in India mode: 1 = Receive not complete, SSPBUF is full 0 = Receive not complete, SSPBUF is full 0 = Receive not complete, SSPBUF is full 0 = Receive not complete, SSPBUF is menty In Receive mode: 1 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0		bit 7							bit 0	
In Master or Silver mode: 1 = Silver rate control enabled for high-speed mode (100 kHz and 1 MHz) 0 = Silver rate control enabled for high-speed mode (400 kHz) bit 6 CKE: SMBus Select bit In Master or Silver mode: 1 = Enable SMBus specific inputs 0 = Disable SMBus specific inputs 0 = Disable SMBus specific inputs 0 = Disable SMBus specific inputs 1 = Endicates bit the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last Note: This bit is cleared on Reset and when SSPEN is cleared. bit 3 S: Start bit 1 = Indicates that a Start bit has been detected last Note: This bit is cleared on Reset and when SSPEN is cleared. bit 3 S: Start bit was not detected last Note: This bit is cleared on Reset and when SSPEN is cleared. bit 4 RW: Read/Withe bit information (I ² C mode only) In <u>Slave mode:</u> 1 = Read 0 = Write Note: This bit holds the R/W bit information following the last address match. This bit is 0 = Transmit is in progress 0 = Transmit is in progress 0 = Transmit is in progress 1 = Transmit is in progress 1 = Transmit is not in progress 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated bit 0 BF: Euffer Full Status bit In <u>Transmit mode</u> 1 = Neetive complete, SSPBUF is full 0 = Receive complete, SSPBUF is full 0 = Receive complete, SSPBUF is full 0 = Data Transmit in progress (does not include the <u>ACK</u> and Stop bits), SSPBUF is full 0 = Data Transmit in progress (does not include the <u>ACK</u> and Stop bits), SSPBUF is full 0 = Data Transmit in progress (does not include the <u>ACK</u> and Stop bits), SSPBUF is full 0 = Data Transmit in progress (does not include the <u>ACK</u> and	bit 7	SMP: Slew	v Rate Contro	ol bit						
 1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz) 0 = Slew rate control enabled for high-speed mode (400 kHz) bit 6 CKE: SMBus Select bit In Master or Slave mode: 1 = Enable SMBus specific inputs 0 = Disable SMBus specific inputs bit 5 D/A: Data/Address bit In Master mode: In Slave mode: 1 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that the last byte received or transmitted was data 0 = Indicates that a Stop bit perceived or transmitted was address bit 4 P: Stop bit 1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last 0 = Start bit 1 = Indicates that a Start bit has been detected last 0 = Start bit was not detected last 1 = Indicates that a Start bit has been detected last 0 = Start bit was not detected last Note: This bit is cleared on Reset and when SSPEN is cleared. bit 2 RWF Read/Write bit information (I²C mode only) In Slave mode: 1 = Transmit is not nprogress 0 = Transmit is not in progress 0 = Transmit is not in progress 0 = Transmit is not in progress (Adress on the ot be updated bit 0 BF: Buffer Full Status bit In Transmit mode: 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not ne		In Master of	or Slave mode	<u>e:</u>						
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 1 = Indicates that the user needs to update the address in the SSPADD register 0 = Address does not need to be updated bit 0 BF: Buffer Full Status bit In Transmit mode: 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty In Receive mode: 1 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the ACK and Stop bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR (1' = Bit is set (0' = Bit is cleared X = Bit is unknown 	bit 1	UA: Updat	e Address (1	0-bit Slave	mode only)					
bit 0 BF: Buffer Full Status bit In Transmit mode: 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty In Receive mode: 1 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the ACK and Stop bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown		1 = Indicat 0 = Addres	es that the us ss does not no	ser needs to eed to be u	o update the pdated	address in	the SSPADI	D register		
In Transmit mode: 1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty In Receive mode: 1 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the ACK and Stop bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown	bit 0	BF: Buffer	Full Status bi	it						
$1 = \text{Receive complete, SSPBUF is full}$ $0 = \text{Receive not complete, SSPBUF is empty}$ In Receive mode: $1 = \text{Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full}$ $0 = \text{Data Transmit complete (does not include the ACK and Stop bits), SSPBUF is empty}$ Legend: $R = \text{Readable bit} \qquad W = \text{Writable bit} \qquad U = \text{Unimplemented bit, read as '0'}$ $R = \text{Readable bit} \qquad W = \text{Writable bit} \qquad U = \text{Unimplemented bit, read as '0'}$		In Transmit mode:								
In Receive mode: 1 = Data Transmit in progress (does not include the ACK and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the ACK and Stop bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR '1' = Bit is set '0' = Bit is cleared		1 = Receive complete, SSPBUF is full 0 = Receive not complete, SSPBUF is empty								
1 = Data Transmit in progress (does not include the \overline{ACK} and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the \overline{ACK} and Stop bits), SSPBUF is empty Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'		U = Receive not complete, SSPBUE IS empty								
Legend: R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' r = Value at POR (1' = Rit is set (0' = Rit is cleared x = Rit is unknown)		1 = Data T 0 = Data T	1 = Data Transmit in progress (does not include the \overline{ACK} and Stop bits), SSPBUF is full 0 = Data Transmit complete (does not include the \overline{ACK} and Stop bits). SSPBUF is empty							
R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' n = Value at POR (1' = Rit is set (0' = Rit is cleared x = Rit is unknown)		Locard					. ,,		-	
$11 - 12$ readable bit $12 - 12$ with able bit $0 = 0$ in the prediction of the set $0^2 - 12$ bit is cleared $x - 12$ bit is unknown		R - Reada	ble bit	\\/ _ \\/	ritable bit	– Inim	nlamented	hit read as '	' ∩'	
L = V O U C O U V O V C = D U S S O V = D U S CIERCEO V = D U S U S U O K O W O V C = D U S CIERCEO V = D U S U O K O W O		-n = Value	at POR	1' = Ri	t is set	0' = Bit i	s cleared	x = Bit is u	nknown	

9.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON and by setting the SSPEN bit. In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I^2C bus may be taken when the P bit is set or the bus is Idle, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I^2C bus operations based on Start and Stop bit conditions.

Once Master mode is enabled, the user has six options.

- 1. Assert a Start condition on SDA and SCL.
- 2. Assert a Repeated Start condition on SDA and SCL.
- 3. Write to the SSPBUF register, initiating transmission of data/address.
- 4. Configure the I²C port to receive data.
- 5. Generate an Acknowledge condition at the end of a received byte of data.
- 6. Generate a Stop condition on SDA and SCL.

Note: The MSSP module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

The following events will cause SSP Interrupt Flag bit, SSPIF, to be set (SSP interrupt if enabled):

- · Start condition
- Stop condition
- Data transfer byte transmitted/received
- Acknowledge transmit
- Repeated Start



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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR, I	on: BOR	Valu all o Res	e on ther sets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	R0IF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000	x000	0000	000x
19h	TXREG	USART Tr	JSART Transmit Register							0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	_	BRGH	TRMT	TX9D	0000	-010	0000	-010
99h	SPBRG	Baud Rate	3aud Rate Generator Register							0000	0000	0000	0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

10.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the Sleep mode. Bit SREN is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during Sleep. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

When setting up a Synchronous Slave Reception, follow these steps:

- Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If 9-bit reception is desired, set bit RX9.
- 4. To enable reception, set enable bit CREN.
- Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading the RCREG register.
- 8. If any error occurred, clear the error by clearing bit CREN.
- 9. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value o POR, BO	n: DR	Valu all c Res	ie on other sets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	R0IF	0000 00	0x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 00	000	0000	0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 00	0x	0000	2000 x
1Ah	RCREG	USART R	JSART Receive Register							0000 00	00	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 00	00	0000	0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -0	10	0000	-010
99h	SPBRG	Baud Rate	3aud Rate Generator Register						0000 00	000	0000	0000	

TABLE 10-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception.

Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices, always maintain these bits clear.

NOTES:

11.5 A/D Operation During Sleep

The A/D module can operate during Sleep mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is completed, the GO/DONE bit will be cleared and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Not	e:	For the A/D module to operate in Sleep,
		the A/D clock source must be set to RC
		(ADCS1:ADCS0 = 11). To allow the con-
		version to occur during Sleep, ensure the
		SLEEP instruction immediately follows the
		instruction that sets the GO/DONE bit.

11.6 Effects of a Reset

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion is aborted. All A/D input pins are configured as analog inputs.

The value that is in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	<u>Valu</u> e on MCLR, WDT
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
1Eh	ADRESH	A/D Resu	VD Result Register High Byte							xxxx xxxx	uuuu uuuu
9Eh	ADRESL	A/D Resu	A/D Result Register Low Byte							xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	_	ADON	0000 00-0	0000 00-0
9Fh	ADCON1	ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0	00 0000	00 0000
85h	TRISA	—	_	PORTA D	PORTA Data Direction Register				11 1111	11 1111	
05h	PORTA	—	_	PORTA D	PORTA Data Latch when written: PORTA pins when read				0x 0000	0u 0000	
89h ⁽¹⁾	TRISE	IBF	OBF	IBOV	PSPMODE	_	PORTE Dat	a Direction	n bits	0000 -111	0000 -111
09h ⁽¹⁾	PORTE	—	_	_	—	_	RE2	RE1	RE0	xxx	uuu

TABLE 11-2: REGISTERS/BITS ASSOCIATED WITH A/D

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: These registers are not available on 28-pin devices.

14.10 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has up to two bits depending upon the device.

Bit 0 is the Brown-out Reset Status bit, BOR. The BOR bit is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if it has been cleared, indicating that a BOR has occurred.

When the Brown-out Reset is disabled, the state of the BOR bit is unpredictable and is, therefore, not valid at any time.

Bit 1 is the Power-on Reset Status bit, $\overline{\text{POR}}$. It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS
--

Oscillator Configuration	Power	-up	Prown out	Wake-up from	
	PWRTE = 0 PWRTE = 1		Brown-out	Sleep	
XT, HS, LP	72 ms + 1024 Tosc	1024 Tosc	72 ms + 1024 Tosc	1024 Tosc	
RC	72 ms		72 ms		

TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE

POR	BOR	то	PD	Condition
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, TO is set on POR
0	x	х	0	Illegal, PD is set on POR
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	MCLR Reset during normal operation
1	1	1	0	MCLR Reset during Sleep or Interrupt Wake-up from Sleep

Legend: x = don't care, u = unchanged

TABLE 14-5: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	Program Counter	Status Register	PCON Register
Power-on Reset	000h	0001 1xxx	0x
MCLR Reset during normal operation	000h	000u uuuu	uu
MCLR Reset during Sleep	000h	0001 0uuu	uu
WDT Reset	000h	0000 luuu	uu
WDT Wake-up	PC + 1	uuu0 0uuu	uu
Brown-out Reset	000h	0001 luuu	u0
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuul Ouuu	uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RLF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	See description below
Status Affected:	С
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.
	C Register f

Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow WDT \text{ prescaler}, \\ 1 \rightarrow \overline{TO}, \\ 0 \rightarrow \overline{PD} \end{array}$
Status Affected:	TO, PD
Description:	The power-down status bit, \overline{PD} , is cleared. Time-out status bit, \overline{TO} , is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

RETURN	Return from Subroutine
Syntax:	[label] RETURN
Operands:	None
Operation:	$TOS \to PC$
Status Affected:	None
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

SUBLW	Subtract W from Literal		
Syntax:	[<i>label</i>] SUBLW k		
Operands:	$0 \leq k \leq 255$		
Operation:	$k \text{ - } (W) \to (W)$		
Status Affected:	C, DC, Z		
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.		

RRF	Rotate Right f through Carry				
Syntax:	[<i>label</i>] RRF f,d				
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$				
Operation:	See description below				
Status Affected:	С				
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.				



SUBWF	Subtract W from f
Syntax:	[<i>label</i>] SUBWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(f) - (W) \rightarrow (destination)
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

FIGURE 17-9: CAPTURE/COMPARE/PWM TIMINGS (CCP1 AND CCP2)



TABLE 17-7: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1 AND CCP2)

Param No.	Symbol	Characteristic			Min	Тур†	Max	Units	Conditions
50*	TCCL	CCP1 and CCP2	No Prescaler		0.5 Tcy + 20	—	—	ns	
		Input Low Time		Standard(F)	10	_	_	ns	
			with Prescaler	Extended(LF)	20	_	_	ns	
51*	ТссН	CCP1 and CCP2	No Prescaler		0.5 TCY + 20		_	ns	
		Input High Time	With Dresseler	Standard(F)	10	-		ns	
			with Prescaler	Extended(LF)	20	_	_	ns	
52*	TCCP	CCP1 and CCP2 Inp	CP1 and CCP2 Input Period			—	_	ns	N = prescale value (1, 4 or 16)
53* TCCR	TccR	CR CCP1 and CCP2 Output Rise Time Standard(F) Extended(LF)		—	10	25	ns		
				Extended(LF)	—	25	50	ns	
54*	54* TCCF CCP1 and CCP2 Output Fa		tput Fall Time	Standard(F)	—	10	25	ns	
				Extended(LF)	_	25	45	ns	
	* These	parameters are chara	eterized but not t	ostod					

These parameters are characterized but not tested.

t Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

18.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum" or "minimum" represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over the whole temperature range.













FIGURE 18-8: AVERAGE Fosc vs. VDD FOR VARIOUS VALUES OF R (RC MODE, C = 100 pF, +25°C)











19.0 PACKAGING INFORMATION

19.1 Package Marking Information

40-Lead PDIP



44-Lead TQFP



44-Lead PLCC



Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:	In the ever be carried characters	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available a for customer-specific information.

I ² C Pue Data	1
1^{2} C Due Ctart/Ctar Dita	י ^
	J
I ² C Master Mode (Reception, 7-bit Address)	3
I ² C Master Mode (Transmission,	
7 or 10-bit Address)102	2
I ² C Slave Mode (Transmission, 10-bit Address) 89	9
I ² C Slave Mode (Transmission, 7-bit Address)87	7
I^2C Slave Mode with SEN = 1 (Reception.	
10-bit Address)	3
I^2 C Slave Mode with SEN = 0 (Recention	-
10-bit Address	ρ
I^2 C Slove Mede with SEN = 0 (Percention	5
T C Slave Mode with SEN = 0 (Reception,	~
	D
I ² C Slave Mode with SEN = 1 (Reception,	_
7-bit Address)	2
Parallel Slave Port (PIC16F874A/877A Only)	7
Parallel Slave Port (PSP) Read52	2
Parallel Slave Port (PSP) Write	2
Repeat Start Condition	0
Reset. Watchdog Timer. Start-up Timer	
and Power-up Timer 184	4
Slave Mode General Call Address Sequence	
(7 or 10 bit Address Mode)	4
	+
	(
Slow Rise Time (MCLR Tied to VDD Via	_
RC Network)152	2
SPI Master Mode (CKE = 0, SMP = 0)	8
SPI Master Mode (CKE = 1, SMP = 1)	В
SPI Mode (Master Mode)76	ô
SPI Mode (Slave Mode with CKE = 0)78	8
SPI Mode (Slave Mode with CKE = 1)	8
SPI Slave Mode (CKE = 0) 189	9
SPI Slave Mode (CKE = 1) 189	9
Stop Condition Receive or Transmit Mode	1
Superconduct Reception	Ŧ
(Master Made ODEN)	
(Master Mode, SREN) 122	4
Synchronous Transmission	2
Synchronous Transmission (Through TXEN)	2
Time- <u>out Se</u> quence on Power-up	
(MCLR Not Tied to VDD)	
Case 1 152	2
Case 2 152	2
Time-out Sequence on Power-up (MCLR Tied	
to VDD via RC Network)	1
Timer0 and Timer1 External Clock 185	5
USART Synchronous Receive	
(Master/Slave) 103	R
LISART Synchronous Transmission	0
(Meeter/Slove)	0
	2
wake-up from Sleep via Interrupt	
Timing Parameter Symbology	1
IMR0 Register	9
TMR1CS Bit57	7
TMR1H Register19	9
TMR1L Register	9
TMR1ON Bit	7
TMR2 Register	9
TMR2ON Bit	1
TMRO Register	1
TOUTPS0 Bit	1
TOLITPS1 Bit	1
TOUTPS2 Bit	1
	1
TDICA Degister	1 0
	J

TRISB Register	20
TRISC Register	
TRISD Register	
TRISE Register	20
IBF Bit	50
IBOV Bit	50
OBF Bit	50
PSPMODE Bit	48, 49, 50, 51
TXREG Register	19
TXSTA Register	
BRGH Bit	111
CSRC Bit	111
SYNC Bit	111
TRMT Bit	111
TX9 Bit	111
TX9D Bit	111
TXEN Bit	111

U

USART 1	11
Address Detect Enable (ADDEN Bit) 1	12
Asynchronous Mode 1	15
Asynchronous Receive (9-bit Mode) 1	19
Asynchronous Receive with Address Detect.	
See Asynchronous Receive (9-bit Mode).	
Asynchronous Receiver	17
Asynchronous Reception1	18
Asvnchronous Transmitter1	15
Baud Rate Generator (BRG) 1	13
Baud Rate Formula1	13
Baud Rates, Asynchronous Mode	-
(BRGH = 0)	14
Baud Rates, Asynchronous Mode	
(BRGH = 1) 1	14
High Baud Rate Select (BRGH Bit) 1	11
Sampling 1	13
Clock Source Select (CSRC Bit) 1	11
Continuous Receive Enable (CREN Bit)	12
Framing Error (FERR Bit) 1	12
Mode Select (SYNC Bit) 1	11
Overrun Error (OERR Bit) 1	12
Receive Data, 9th Bit (RX9D Bit)	12
Receive Enable, 9-bit (RX9 Bit) 1	12
Serial Port Enable (SPEN Bit)111, 1	12
Single Receive Enable (SREN Bit) 1	12
Synchronous Master Mode1	21
Synchronous Master Reception 1	23
Synchronous Master Transmission1	21
Synchronous Slave Mode1	24
Synchronous Slave Reception 1	25
Synchronous Slave Transmit	24
Transmit Data. 9th Bit (TX9D)1	11
Transmit Enable (TXEN Bit) 1	11
Transmit Enable. 9-bit (TX9 Bit)	11
Transmit Shift Register Status (TRMT Bit)1	11
USART Synchronous Receive Requirements	93
V	
V	

VDD Pin	
Voltage Reference Specifications	180
Vss Pin	