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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	10MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	192 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf873a-i-ml

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3.0 DATA EEPROM AND FLASH PROGRAM MEMORY

The data EEPROM and Flash program memory is readable and writable during normal operation (over the full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. These devices have 128 or 256 bytes of data EEPROM (depending on the device), with an address range from 00h to FFh. On devices with 128 bytes, addresses from 80h to FFh are unimplemented and will wraparound to the beginning of data EEPROM memory. When writing to unimplemented locations, the on-chip charge pump will be turned off.

When interfacing the program memory block, the EEDATA and EEDATH registers form a two-byte word that holds the 14-bit data for read/write and the EEADR and EEADRH registers form a two-byte word that holds the 13-bit address of the program memory location being accessed. These devices have 4 or 8K words of program Flash, with an address range from 0000h to 0FFFh for the PIC16F873A/874A and 0000h to 1FFFh for the PIC16F876A/877A. Addresses above the range of the respective device will wraparound to the beginning of program memory.

The EEPROM data memory allows single-byte read and write. The Flash program memory allows single-word reads and four-word block writes. Program memory write operations automatically perform an erase-before-write on blocks of four words. A byte write in data EEPROM memory automatically erases the location and writes the new data (erase-before-write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the data EEPROM memory. Depending on the settings of the write-protect bits, the device may or may not be able to write certain blocks of the program memory; however, reads of the program memory are allowed. When code-protected, the device programmer can no longer access data or program memory; this does NOT inhibit internal reads or writes.

3.1 EEADR and EEADRH

The EEADRH:EEADR register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 8K words of program EEPROM. When selecting a data address value, only the LSByte of the address is written to the EEADR register. When selecting a program address value, the MSByte of the address is written to the EEADRH register and the LSByte is written to the EEADR register.

If the device contains less memory than the full address reach of the address register pair, the Most Significant bits of the registers are not implemented. For example, if the device has 128 bytes of data EEPROM, the Most Significant bit of EEADR is not implemented on access to data EEPROM.

3.2 EECON1 and EECON2 Registers

EECON1 is the control register for memory accesses.

Control bit, EEPGD, determines if the access will be a program or data memory access. When clear, as it is when reset, any subsequent operations will operate on the data memory. When set, any subsequent operations will operate on the program memory.

Control bits, RD and WR, initiate read and write or erase, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write or erase operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write (or erase) operation is interrupted by a $\overline{\text{MCLR}}$ or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit, EEIF in the PIR2 register, is set when the write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the EEPROM write sequence.

Note: The self-programming mechanism for Flash program memory has been changed. On previous PIC16F87X devices, Flash programming was done in single-word erase/ write cycles. The newer PIC18F87XA devices use a four-word erase/write cycle. See Section 3.6 "Writing to Flash Program Memory" for more information.

3.5 Reading Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the EEADR and EEADRH registers, set the EEPGD control bit (EECON1<7>) and then set control bit RD (EECON1<0>). Once the read control bit is set, the program memory Flash controller will use the next two instruction cycles to read the data. This causes these two instructions immediately following the "BSF EECON1, RD" instruction to be ignored. The data is available in the very next cycle in the EEDATA and EEDATH registers; therefore, it can be read as two bytes in the following instructions. EEDATA and EEDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-3	FI ASH	PROGRAM	RFAD
$L \land \land \square$		INCONAM	ILAD

		BSF	STATUS, RP1	-	;	
		BCF	STATUS, RPO)	;	Bank 2
		MOVLW	MS_PROG_EE	ADDR	;	
		MOVWF	EEADRH		;	MS Byte of Program Address to read
		MOVLW	LS PROG EE	ADDR	;	
		MOVWF	EEADR		;	LS Byte of Program Address to read
		BSF	STATUS, RPO)	;	Bank 3
		BSF	EECON1, EEF	GD	;	Point to PROGRAM memory
		BSF	EECON1, RD		;	EE Read
eq	eg ;					
quin	nen	NOP				
Rec	ed	NOP			;	Any instructions here are ignored as program
`					;	memory is read in second cycle after BSF EECON1,RD
	;					
		BCF	STATUS, RPO)	;	Bank 2
		MOVF	EEDATA, W		;	W = LS Byte of Program EEDATA
		MOVWF	DATAL		;	
		MOVF	EEDATH, W		;	W = MS Byte of Program EEDATA
		MOVWF	DATAH		;	

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T1CKI	bit 0	ST	Input/output port pin or Timer1 oscillator output/Timer1 clock input.
RC1/T1OSI/CCP2	bit 1	ST	Input/output port pin or Timer1 oscillator input or Capture2 input/ Compare2 output/PWM2 output.
RC2/CCP1	bit 2	ST	Input/output port pin or Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	bit 3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit 4	ST	RC4 can also be the SPI data in (SPI mode) or data I/O (I ² C mode).
RC5/SDO	bit 5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX/CK	bit 6	ST	Input/output port pin or USART asynchronous transmit or synchronous clock.
RC7/RX/DT	bit 7	ST	Input/output port pin or USART asynchronous receive or synchronous data.

TABLE 4-5:PORTC FUNCTIONS

Legend: ST = Schmitt Trigger input

TABLE 4-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	XXXX XXXX	uuuu uuuu
87h	TRISC	PORTC	Data Dire	ection Re	gister					1111 1111	1111 1111

Legend: x = unknown, u = unchanged

5.2 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 Tosc (and a small RC delay of 20 ns) and low for at least 2 Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

5.3 Prescaler

REGISTER 5-1:

There is only one prescaler available which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the

OPTION REG REGISTER

Timer0 module means that there is no prescaler for the Watchdog Timer and vice versa. This prescaler is not readable or writable (see Figure 5-1).

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF1, MOVWF1, BSF1, x....etc.) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

		_										
	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1				
	RBPU	INTEDG	TOCS	T0SE	PSA	PS2	R/W-1 PS1	PS0				
	bit 7							bit				
t 7	RBPU											
t 6	INTEDG											
t 5	TOCS: TMR0 Clock Source Select bit											
	1 = Transit 0 = Interna	ion on T0CK al instruction	íl pin cycle clock	(CLKO)								
t 4	TOSE: TMI	R0 Source E	dge Select	bit								
	1 = Increm 0 = Increm	ient on high-f	to-low trans	sition on TOC sition on TOC	CKI pin CKI pin							
t 3	PSA: Prescaler Assignment bit											
	1 = Presca 0 = Presca	aler is assign aler is assign	ed to the W ed to the Ti	/DT mer0 modul	e							
t 2-0	PS2:PS0: Prescaler Rate Select bits											
	Bit Value	TMR0 Rate	WDT Rate									
	000 001 010 011 100 101 110 111	1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128 1 : 256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128									
	Legend:											
	R = Reada	able bit	VV = V	Vritable bit	U = Unimp	plemented b	it, read as '	0'				
						ماممتعما		- 1				

be followed even if the WDT is disabled.

6.7 Resetting of Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other Reset, except by the CCP1 and CCP2 special event triggers.

T1CON register is reset to 00h on a Power-on Reset, or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other Resets, the register is unaffected.

6.8 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

TABLE 6-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value POR,	e on: BOR	Valu all c Res	e on other sets
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF	0000	000x	0000	000u
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000	0000	0000	0000
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000	0000	0000	0000
0Eh	TMR1L	Holding F	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx	uuuu	uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx	xxxx	uuuu	uuuu
10h	T1CON	_		T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	00	0000	uu	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: Bits PSPIE and PSPIF are reserved on the 28-pin devices; always maintain these bits clear.

8.3 PWM Mode (PWM)

In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force
	the CCP1 PWM output latch to the default
	low level. This is not the PORTC I/O data
	latch.

Figure 8-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 8.3.3 "Setup for PWM Operation**".

FIGURE 8-3:	SIMPLIFIED PWM BLOCK
	DIAGRAM



A PWM output (Figure 8-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).





8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

 $PWM Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet$ (TMR2 Prescale Value)

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.1
	"Timer2 Prescaler and Postscaler") is
	not used in the determination of the PWM
	frequency. The postscaler could be used
	to have a servo update rate at a different
	frequency than the PWM output.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

PWM Duty Cycle =(CCPR1L:CCP1CON<5:4>)• Tosc • (TMR2 Prescale Value)

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitch-free PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the following formula.

EQUATION 8-1:



Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

9.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all '0's with R/W = 0.

The general call address is recognized when the General Call Enable bit (GCEN) is enabled (SSPCON2<7> set). Following a Start bit detect, 8 bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit) and on the falling edge of the ninth bit (ACK bit), the SSPIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-bit Address mode, then the second half of the address is not necessary, the UA bit will not be set and the slave will begin receiving data after the Acknowledge (Figure 9-15).





9.4.8 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition, the user sets the Start condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the Baud Rate Generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low, while SCL is high, is the Start condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the Baud Rate Generator is suspended, leaving the SDA line held low and the Start condition is complete.

Note: If at the beginning of the Start condition, the SDA and SCL pins are already sampled low, or if during the Start condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag (BCLIF) is set, the Start condition is aborted and the I²C module is reset into its Idle state.

9.4.8.1 WCOL Status Flag

If the user writes the SSPBUF when a Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the Start condition is complete.

FIGURE 9-19: FIRST START BIT TIMING



10.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial Communications Interface or SCI.) The USART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers, or it can be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc. The USART can be configured in the following modes:

- Asynchronous (full-duplex)
- Synchronous Master (half-duplex)
- Synchronous Slave (half-duplex)

Bit SPEN (RCSTA<7>) and bits TRISC<7:6> have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

The USART module also has a multi-processor communication capability using 9-bit address detection.

REGISTER 10-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0					
	CSRC	TX9	TXEN	SYNC		BRGH	TRMT	TX9D					
	bit 7							bit 0					
bit 7	CSRC: Cloc	k Source Se	elect bit										
	<u>Asynchronous mode:</u> Don't care.												
	<u>Synchronou</u> 1 = Master r 0 = Slave m	<u>Synchronous mode:</u> 1 = Master mode (clock generated internally from BRG) 0 = Slave mode (clock from external source)											
bit 6	TX9 : 9-bit Tr	ransmit Enal	ole bit										
	1 = Selects 0 = Selects	9-bit transmi 8-bit transmi	ssion ssion										
bit 5	TXEN: Trans	smit Enable	bit										
	1 = Transmit enabled 0 = Transmit disabled												
	Note:	SREN/CREM	v overrides	TXEN in Sy	nc mode.								
bit 4	SYNC: USA	SYNC: USART Mode Select bit											
	1 = Synchro	nous mode											
	0 = Asynchr	onous mode)										
bit 3	Unimpleme	nted: Read	as '0'										
bit 2	BRGH: High	BRGH: High Baud Rate Select bit											
	Asynchronous mode: 1 = High speed 0 = Low speed												
	<u>Synchronous mode:</u> Unused in this mode.												
bit 1	TRMT: Transmit Shift Register Status bit												
	1 = TSR em 0 = TSR full	1 = TSR empty 0 = TSR full											
bit 0	TX9D: 9th b	TX9D: 9th bit of Transmit Data, can be Parity bit											
	Legend:												
	R = Readab	le bit	VV = Wr	itable bit	U = Unimp	lemented b	it, read as '()´					
	- n = Value a	at POR	'1' = Bit	is set	'0' = Bit is o	cleared	x = Bit is ur	hknown					

10.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either enable bit, SREN (RCSTA<5>), or enable bit, CREN (RCSTA<4>). Data is sampled on the RC7/RX/DT pin on the falling edge of the clock. If enable bit SREN is set, then only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to the RCREG register (if it is empty). When the transfer is complete, interrupt flag bit, RCIF (PIR1<5>), is set. The actual interrupt can be enabled/ disabled by setting/clearing enable bit, RCIE (PIE1<5>). Flag bit RCIF is a read-only bit which is reset by the hardware. In this case, it is reset when the RCREG register has been read and is empty. The RCREG is a double-buffered register (i.e., it is a twodeep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR register. On the clocking of the last bit of the third byte, if the RCREG register is still full, then Overrun Error bit, OERR (RCSTA<1>), is set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Bit OERR has to be cleared in software (by clearing bit CREN). If bit OERR is set, transfers from the RSR to the RCREG are inhibited so it is essential to clear bit OERR if it is set. The ninth receive bit is buffered the same way as the receive

data. Reading the RCREG register will load bit RX9D with a new value, therefore, it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old RX9D information.

When setting up a Synchronous Master Reception:

- 1. Initialize the SPBRG register for the appropriate baud rate (Section 10.1 "USART Baud Rate Generator (BRG)").
- 2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 3. Ensure bits CREN and SREN are clear.
- 4. If interrupts are desired, then set enable bit RCIE.
- 5. If 9-bit reception is desired, then set bit RX9.
- 6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
- Interrupt flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- 8. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 9. Read the 8-bit received data by reading the RCREG register.
- 10. If any error occurred, clear the error by clearing bit CREN.
- 11. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets	
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	R0IF	0000 000x	0000 000u	
0Ch	PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000	
18h	RCSTA	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00x	
1Ah	RCREG	USART Re	eceive Re	gister						0000 0000	0000 0000	
8Ch	PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000	
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010	
99h	SPBRG	Baud Rate	Generato	or Register						0000 0000	0000 0000	

TABLE 10-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception. Note 1: Bits PSPIE and PSPIF are reserved on 28-pin devices; always maintain these bits clear.

PIC16F87XA





TABLE 13-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE	ABLE 13-1:	ABLE 1	3-1:	F	REGIST	ERS /	ASSO		ED	WITH	CON	IPAR	ATOR	VO	LTAG	E RI	EFER	ENCE	Ξ
--	------------	--------	------	---	--------	-------	------	--	----	------	-----	-------------	------	----	------	------	------	------	---

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Ch	CMCON	C2OUT	C10UT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used with the comparator voltage reference.

TABLE 14-2:CAPACITOR SELECTION FOR
CRYSTAL OSCILLATOR

Osc Type	Crystal Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15-33 pF	15-33 pF
	20 MHz	15-33 pF	15-33 pF

These values are for design guidance only. See notes following this table.

Crystals Used							
32 kHz	Epson C-001R32.768K-A	± 20 PPM					
200 kHz	STD XTL 200.000KHz	± 20 PPM					
1 MHz	ECS ECS-10-13-1	± 50 PPM					
4 MHz	ECS ECS-40-20-1	± 50 PPM					
8 MHz	EPSON CA-301 8.000M-C	± 30 PPM					
20 MHz	EPSON CA-301 20.000M-C	± 30 PPM					

- Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.
 - 2: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
 - **3:** *R*_s may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
 - When migrating from other PIC[®] devices, oscillator performance should be verified.

14.2.3 RC OSCILLATOR

For timing insensitive applications, the "RC" device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-3 shows how the R/C combination is connected to the PIC16F87XA.





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NOTES:

16.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB[®] IDE Software
- Assemblers/Compilers/Linkers
 - MPASM[™] Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK[™] Object Linker/
 - MPLIB[™] Object Librarian
 - MPLAB C30 C Compiler
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
- MPLAB dsPIC30 Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
- MPLAB ICD 2
- Device Programmers
 - PRO MATE[®] II Universal Device Programmer
 - PICSTART[®] Plus Development Programmer
- Low Cost Demonstration Boards
 - PICDEM[™] 1 Demonstration Board
 - PICDEM.net[™] Demonstration Board
 - PICDEM 2 Plus Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 4 Demonstration Board
 - PICDEM 17 Demonstration Board
 - PICDEM 18R Demonstration Board
 - PICDEM LIN Demonstration Board
 - PICDEM USB Demonstration Board
- Evaluation Kits
 - KEELOQ[®]
 - PICDEM MSC
 - microID[®]
 - CAN
 - PowerSmart[®]
 - Analog

16.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows[®] based application that contains:

- · An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- · A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help
- The MPLAB IDE allows you to:
- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files (assembly or C)
 - absolute listing file (mixed assembly and C)
 - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

16.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- · User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

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FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

FIGURE 17-7: BROWN-OUT RESET TIMING



TABLE 17-5:RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER
AND BROWN-OUT RESET REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2	_	_	μs	VDD = 5V, -40°C to +85°C
31*	Twdt	Watchdog Timer Time-out Period (no prescaler)	7	18	33	ms	VDD = 5V, -40°C to +85°C
32	Tost	Oscillation Start-up Timer Period	—	1024 Tosc		-	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28	72	132	ms	VDD = 5V, -40°C to +85°C
34	Tıoz	I/O High-Impedance from MCLR Low or Watchdog Timer Reset	_	_	2.1	μS	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	$VDD \leq VBOR (D005)$

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.



TABLE 17-8: PARALLEL SLAVE PORT REQUIREMENTS (PIC16F874A/877A ONLY)

Param No.	Symbol	Characteristic	Min	Тур†	Max	Units	Conditions	
62	TdtV2wrH	Data In Valid before $\overline{WR} \uparrow or \overline{CS} \uparrow (setup)$	20	_		ns		
63*	TwrH2dtl	\overline{WR} \uparrow or \overline{CS} \uparrow to Data–in Invalid	Standard(F)	20	-	—	ns	
		(hold time)	Extended(LF)	35	-		ns	
64	TrdL2dtV	$\overline{RD}\downarrow$ and $\overline{CS}\downarrow$ to Data–out Valid	—	—	80	ns		
65	TrdH2dtI	\overline{RD} \uparrow or \overline{CS} \downarrow to Data–out Invalid	10	_	30	ns		

These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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44-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		MILLIMETERS*			
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		44			44		
Pitch	р		.031			0.80		
Pins per Side	n1		11			11		
Overall Height	Α	.039	.043	.047	1.00	1.10	1.20	
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05	
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15	
Foot Length	L	.018	.024	.030	0.45	0.60	0.75	
Footprint (Reference)	(F)		.039		1.00			
Foot Angle	¢	0	3.5	7	0	3.5	7	
Overall Width	E	.463	.472	.482	11.75	12.00	12.25	
Overall Length	D	.463	.472	.482	11.75	12.00	12.25	
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10	
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10	
Lead Thickness	с	.004	.006	.008	0.09	0.15	0.20	
Lead Width	В	.012	.015	.017	0.30	0.38	0.44	
Pin 1 Corner Chamfer	СН	.025	.035	.045	0.64	0.89	1.14	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

* Controlling Parameter § Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC Equivalent: MS-026 Drawing No. C04-076

28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body, Punch Singulated (QFN)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		INCHES		MILLIMETERS*				
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		28			28		
Pitch	р		.026 BSC			0.65 BSC		
Overall Height	Α		.033	.039		0.85	1.00	
Molded Package Thickness	A2		.026	.031		0.65	0.80	
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05	
Base Thickness	A3		.008 REF		0.20 REF			
Overall Width	E		.236 BSC	3C 6.00 BSC				
Molded Package Width	E1		.226 BSC			5.75 BSC		
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85	
Overall Length	D		.236 BSC		6.00 BSC			
Molded Package Length	D1		.226 BSC			5.75 BSC		
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85	
Lead Width	В	.009	.011	.014	0.23	0.28	0.35	
Lead Length	L	.020	.024	.030	0.50	0.60	0.75	
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23	
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65	
Chamfer	СН	.009	.017	.024	0.24	0.42	0.60	
Mold Draft Angle Top	α			12°			12°	

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side. JEDEC equivalent: mMO-220

Drawing No. C04-114

APPENDIX A: REVISION HISTORY

Revision A (November 2001)

Original data sheet for PIC16F87XA devices. The devices presented are enhanced versions of the PIC16F87X microcontrollers discussed in the *"PIC16F87X Data Sheet"* (DS30292).

Revision B (October 2003)

This revision includes the DC and AC Characteristics Graphs and Tables. The Electrical Specifications in **Section 17.0 "Electrical Characteristics"** have been updated and there have been minor corrections to the data sheet text.

Revision C (January 2013)

Added a note to each package outline drawing.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices in this data sheet are listed in Table B-1.

TABLE B-1:	DIFFERENCES BETWEEN DEVICES IN THE PIC16F87XA FAMILY

	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Slave Port	No	Yes	No	Yes
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN