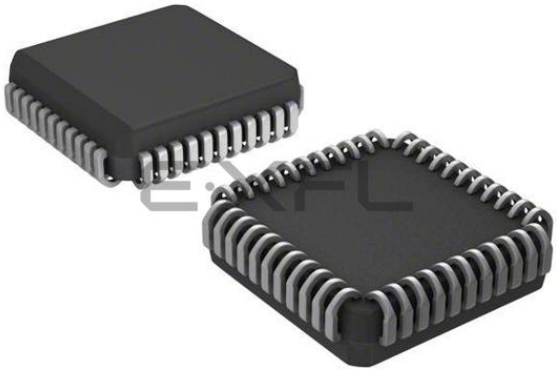

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 10MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 7KB (4K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | 128 x 8 |
| RAM Size | 192 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.59x16.59) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16lf874at-i-l |

**TABLE 1-3: PIC16F874A/877A PINOUT DESCRIPTION (CONTINUED)**

| Pin Name | PDIP Pin# | PLCC Pin# | TQFP Pin# | QFN Pin# | I/O/P Type | Buffer Type | Description |
|---|---|---|---|---|---|---|---|
| | | | | | | | PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. |
| RB0/INT | 33 | 36 | 8 | 9 | | TTL/ST(1) | |
| RB0 | | | | | I/O | | Digital I/O. |
| INT | | | | | I | | External interrupt. |
| RB1 | 34 | 37 | 9 | 10 | I/O | TTL | Digital I/O. |
| RB2 | 35 | 38 | 10 | 11 | I/O | TTL | Digital I/O. |
| RB3/PGM | 36 | 39 | 11 | 12 | | TTL | |
| RB3 | | | | | I/O | | Digital I/O. |
| PGM | | | | | I | | Low-voltage ICSP programming enable pin. |
| RB4 | 37 | 41 | 14 | 14 | I/O | TTL | Digital I/O. |
| RB5 | 38 | 42 | 15 | 15 | I/O | TTL | Digital I/O. |
| RB6/PGC | 39 | 43 | 16 | 16 | | TTL/ST(2) | |
| RB6 | | | | | I/O | | Digital I/O. |
| PGC | | | | | I | | In-circuit debugger and ICSP programming clock. |
| RB7/PGD | 40 | 44 | 17 | 17 | | TTL/ST(2) | |
| RB7 | | | | | I/O | | Digital I/O. |
| PGD | | | | | I/O | | In-circuit debugger and ICSP programming data. |

**Legend:** I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

**Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.
**2:** This buffer is a Schmitt Trigger input when used in Serial Programming mode.
**3:** This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

**NOTES:**

## 3.5 Reading Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the EEADR and EEADRH registers, set the EEPGD control bit (EECON1<7>) and then set control bit RD (EECON1<0>). Once the read control bit is set, the program memory Flash controller will use the next two instruction cycles to read the data. This causes these two instructions immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle in the EEDATA and EEDATH registers; therefore, it can be read as two bytes in the following instructions. EEDATA and EEDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

**EXAMPLE 3-3: FLASH PROGRAM READ**

```
        BSF     STATUS, RP1      ;
        BCF     STATUS, RP0      ; Bank 2
        MOVLW   MS_PROG_EE_ADDR  ;
        MOVWF   EEADRH           ; MS Byte of Program Address to read
        MOVLW   LS_PROG_EE_ADDR  ;
        MOVWF   EEADR            ; LS Byte of Program Address to read
        BSF     STATUS, RP0      ; Bank 3
        BSF     EECON1, EEPGD    ; Point to PROGRAM memory
        BSF     EECON1, RD       ; EE Read
;  Required Sequence
        NOP
        NOP                      ; Any instructions here are ignored as program
                                 ; memory is read in second cycle after BSF EECON1,RD
;
        BCF     STATUS, RP0      ; Bank 2
        MOVF    EEDATA, W        ; W = LS Byte of Program EEDATA
        MOVWF   DATAL            ;
        MOVF    EEDATH, W        ; W = MS Byte of Program EEDATA
        MOVWF   DATAH            ;
```

**TABLE 4-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on: POR, BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 09h | PORTE | — | — | — | — | — | RE2 | RE1 | RE0 | ---- -xxx | ---- -uuu |
| 89h | TRISE | IBF | OBF | IBOV | PSPMODE | — | PORTE Data Direction bits | | | 0000 -111 | 0000 -111 |
| 9Fh | ADCON1 | ADFM | ADCS2 | — | — | PCFG3 | PCFG2 | PCFG1 | PCFG0 | 00-- 0000 | 00-- 0000 |

**Legend:** x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTE.

**REGISTER 4-1: TRISE REGISTER (ADDRESS 89h)**

| R-0 | R-0 | R/W-0 | R/W-0 | U-0 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| IBF | OBF | IBOV | PSPMODE | — | Bit 2 | Bit 1 | Bit 0 |
| bit 7 | | | | | | | bit 0 |

**Parallel Slave Port Status/Control Bits:**

bit 7 **IBF:** Input Buffer Full Status bit
1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received

bit 6 **OBF**: Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5 **IBOV**: Input Buffer Overflow Detect bit (in Microprocessor mode)
1 = A write occurred when a previously input word has not been read (must be cleared in software)
0 = No overflow occurred

bit 4 **PSPMODE**: Parallel Slave Port Mode Select bit
1 = PORTD functions in Parallel Slave Port mode
0 = PORTD functions in general purpose I/O mode

bit 3 **Unimplemented**: Read as '0'

**PORTE Data Direction Bits:**

bit 2 **Bit 2**: Direction Control bit for pin RE2/$\overline{CS}$/AN7
1 = Input
0 = Output

bit 1 **Bit 1**: Direction Control bit for pin RE1/$\overline{WR}$/AN6
1 = Input
0 = Output

bit 0 **Bit 0**: Direction Control bit for pin RE0/$\overline{RD}$/AN5
1 = Input
0 = Output

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**REGISTER 9-3: SSPSTAT: MSSP STATUS REGISTER ($I^2C$ MODE) (ADDRESS 94h)**

| R/W-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| SMP | CKE | D/$\overline{A}$ | P | S | R/$\overline{W}$ | UA | BF |
| bit 7 | | | | | | | bit 0 |

bit 7 **SMP:** Slew Rate Control bit

In Master or Slave mode:

1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)

0 = Slew rate control enabled for high-speed mode (400 kHz)

bit 6 **CKE:** SMBus Select bit

In Master or Slave mode:

1 = Enable SMBus specific inputs

0 = Disable SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit

In Master mode:

Reserved.

In Slave mode:

1 = Indicates that the last byte received or transmitted was data

0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit

1 = Indicates that a Stop bit has been detected last

0 = Stop bit was not detected last

**Note:** This bit is cleared on Reset and when SSPEN is cleared.

bit 3 **S:** Start bit

1 = Indicates that a Start bit has been detected last

0 = Start bit was not detected last

**Note:** This bit is cleared on Reset and when SSPEN is cleared.

bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information ($I^2C$ mode only)

In Slave mode:

1 = Read

0 = Write

**Note:** This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.

In Master mode:

1 = Transmit is in progress

0 = Transmit is not in progress

**Note:** ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

bit 1 **UA:** Update Address (10-bit Slave mode only)

1 = Indicates that the user needs to update the address in the SSPADD register

0 = Address does not need to be updated

bit 0 **BF:** Buffer Full Status bit

In Transmit mode:

1 = Receive complete, SSPBUF is full

0 = Receive not complete, SSPBUF is empty

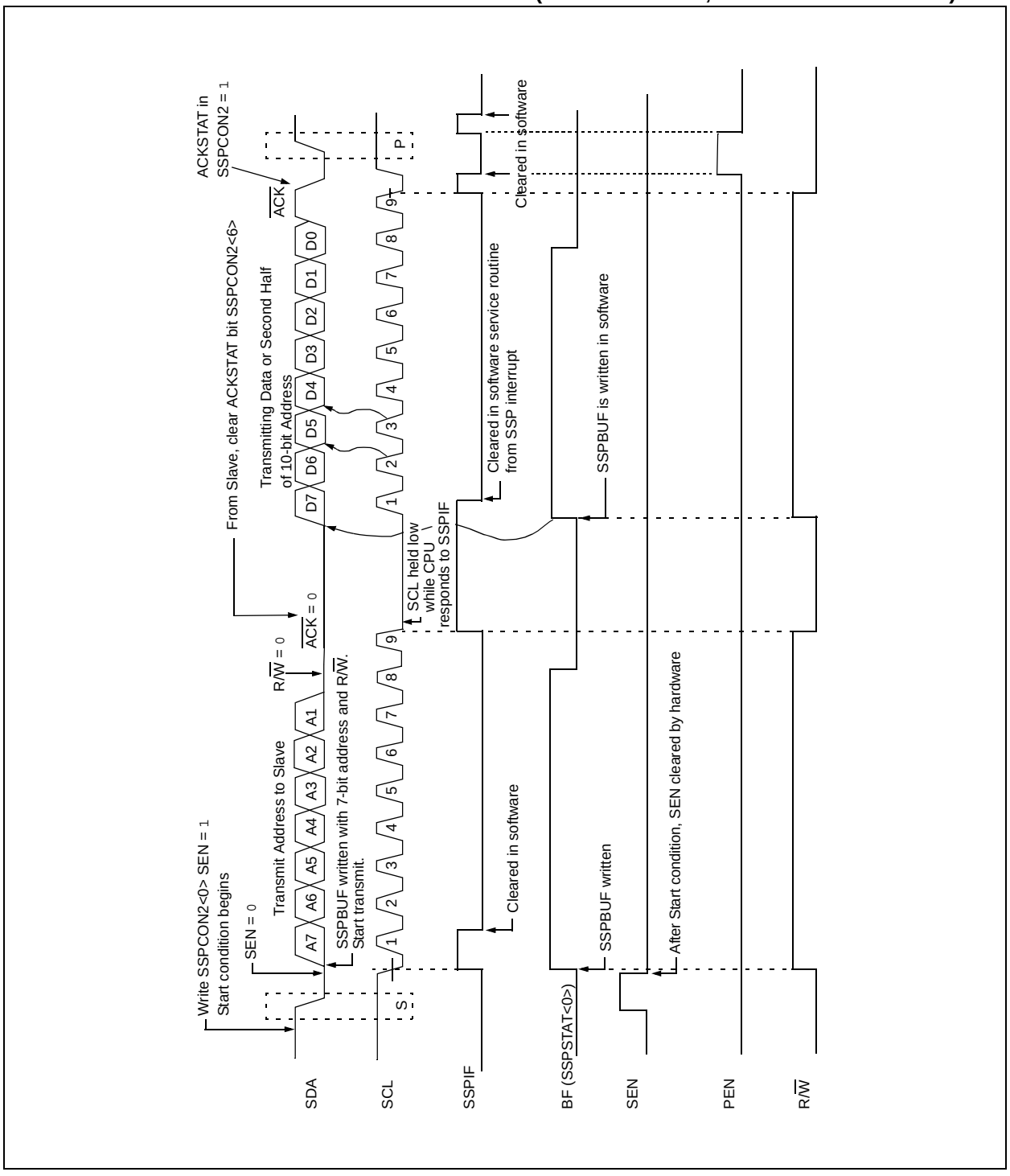
In Receive mode:

1 = Data Transmit in progress (does not include the $\overline{ACK}$ and Stop bits), SSPBUF is full

0 = Data Transmit complete (does not include the $\overline{ACK}$ and Stop bits), SSPBUF is empty

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| - n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**FIGURE 9-21: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)**



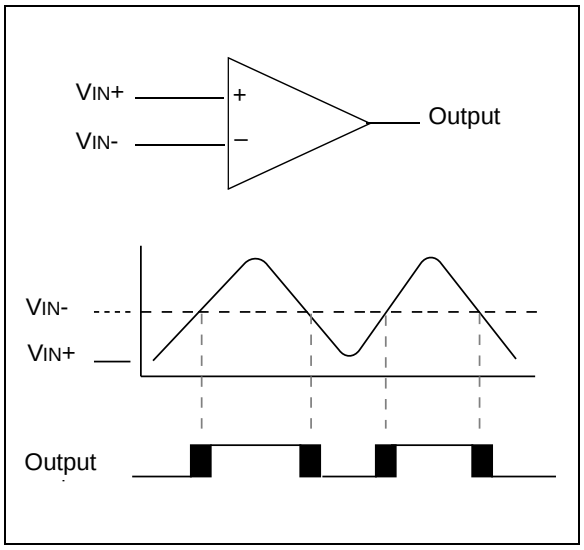
## 12.2 Comparator Operation

A single comparator is shown in Figure 12-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 12-2 represent the uncertainty due to input offsets and response time.

## 12.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 12-2).

**FIGURE 12-2: SINGLE COMPARATOR**




### 12.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between VSS and VDD and can be applied to either pin of the comparator(s).

### 12.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. **Section 13.0 "Comparator Voltage Reference Module"** contains a detailed description of the Comparator Voltage Reference module that provides this signal. The internal reference signal is used when comparators are in mode, CM<2:0> = 110 (Figure 12-1). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

## 12.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (**Section 17.0 "Electrical Characteristics"**).

## 12.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RA4 and RA5 I/O pins. When enabled, multiplexors in the output path of the RA4 and RA5 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 12-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/ disable for the RA4 and RA5 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<4:5>).

| | |
|---|---|
| **Note 1:** | When reading the Port register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification. |
| **2:** | Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified. |
| **3:** | RA4 is an open collector I/O pin. When used as an output, a pull-up resistor is required. |

## 13.0 COMPARATOR VOLTAGE REFERENCE MODULE

The Comparator Voltage Reference Generator is a 16-tap resistor ladder network that provides a fixed voltage reference when the comparators are in mode '110'. A programmable register controls the function of the reference generator. Register 13-1 lists the bit functions of the CVRCON register.

As shown in Figure 13-1, the resistor ladder is segmented to provide two ranges of $CV_{REF}$ values and has a power-down function to conserve power when the reference is not being used. The comparator reference supply voltage (also referred to as $CV_{RSRC}$) comes directly from $V_{DD}$. It should be noted, however, that the voltage at the top of the ladder is $CV_{RSRC} - V_{SAT}$, where $V_{SAT}$ is the saturation voltage of the power switch transistor. This reference will only be as accurate as the values of $CV_{RSRC}$ and $V_{SAT}$.

The output of the reference generator may be connected to the RA2/AN2/$V_{REF}$-/$CV_{REF}$ pin. This can be used as a simple D/A function by the user if a very high-impedance load is used. The primary purpose of this function is to provide a test path for testing the reference generator function.

**REGISTER 13-1: CVRCON CONTROL REGISTER (ADDRESS 9Dh)**

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CVREN | CVROE | CVRR | — | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

bit 7 **CVREN**: Comparator Voltage Reference Enable bit
1 = $CV_{REF}$ circuit powered on
0 = $CV_{REF}$ circuit powered down

bit 6 **CVROE:** Comparator $V_{REF}$ Output Enable bit
1 = $CV_{REF}$ voltage level is output on RA2/AN2/$V_{REF}$-/$CV_{REF}$ pin
0 = $CV_{REF}$ voltage level is disconnected from RA2/AN2/$V_{REF}$-/$CV_{REF}$ pin

bit 5 **CVRR**: Comparator $V_{REF}$ Range Selection bit
1 = 0 to 0.75 $CV_{RSRC}$, with $CV_{RSRC}$/24 step size
0 = 0.25 $CV_{RSRC}$ to 0.75 $CV_{RSRC}$, with $CV_{RSRC}$/32 step size

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **CVR3:CVR0:** Comparator $V_{REF}$ Value Selection bits $0 \le VR3:VR0 \le 15$
When CVRR = 1:
$CV_{REF} = (VR<3:0>/ 24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (VR3:VR0/ 32) \bullet (CV_{RSRC})$

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

**TABLE 14-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR**

| Osc Type | Crystal Freq. | Cap. Range C1 | Cap. Range C2 |
|---|---|---|---|
| LP | 32 kHz | 33 pF | 33 pF |
| | 200 kHz | 15 pF | 15 pF |
| XT | 200 kHz | 47-68 pF | 47-68 pF |
| | 1 MHz | 15 pF | 15 pF |
| | 4 MHz | 15 pF | 15 pF |
| HS | 4 MHz | 15 pF | 15 pF |
| | 8 MHz | 15-33 pF | 15-33 pF |
| | 20 MHz | 15-33 pF | 15-33 pF |
| **These values are for design guidance only.** See notes following this table. | | | |
| **Crystals Used** | | | |
| 32 kHz | Epson C-001R32.768K-A | ± 20 PPM | |
| 200 kHz | STD XTL 200.000KHz | ± 20 PPM | |
| 1 MHz | ECS ECS-10-13-1 | ± 50 PPM | |
| 4 MHz | ECS ECS-40-20-1 | ± 50 PPM | |
| 8 MHz | EPSON CA-301 8.000M-C | ± 30 PPM | |
| 20 MHz | EPSON CA-301 20.000M-C | ± 30 PPM | |

**Note 1:** Higher capacitance increases the stability of oscillator but also increases the start-up time.

**2:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

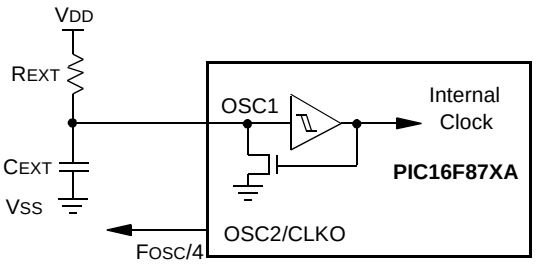
**3:** $R_S$ may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.

**4:** When migrating from other PIC® devices, oscillator performance should be verified.

### 14.2.3 RC OSCILLATOR

For timing insensitive applications, the “RC” device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 14-3 shows how the R/C combination is connected to the PIC16F87XA.

**FIGURE 14-3: RC OSCILLATOR MODE**




Recommended values: 3 kΩ ≤ REXT ≤ 100 kΩ
CEXT > 20 pF

## 14.3 Reset

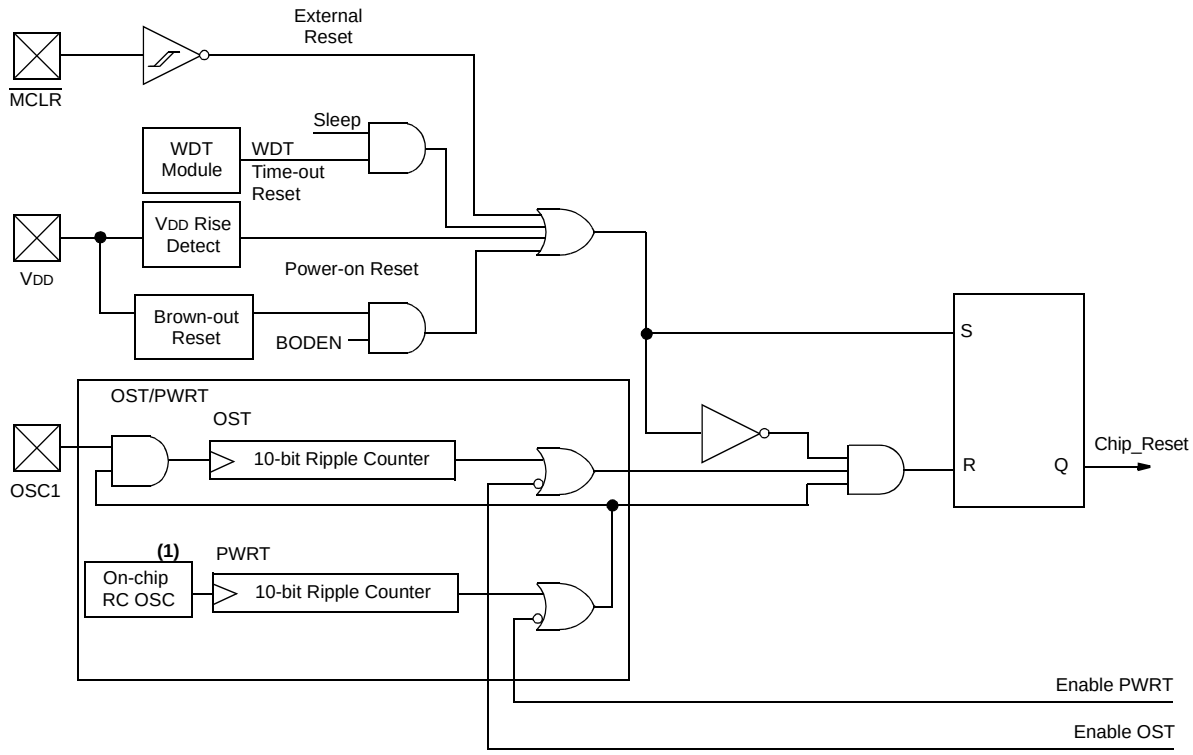
The PIC16F87XA differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset (during normal operation)
- WDT Wake-up (during Sleep)
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition. Their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on Power-on Reset (POR), on the $\overline{\text{MCLR}}$ and WDT Reset, on $\overline{\text{MCLR}}$ Reset during Sleep and Brown-out Reset (BOR). They are not affected by a WDT wake-up which is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations as indicated in Table 14-4. These bits are used in software to determine the nature of the Reset. See Table 14-6 for a full description of Reset states of all registers.

A simplified block diagram of the on-chip Reset circuit is shown in Figure 14-4.

**FIGURE 14-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT**




**Note 1:** This is a separate oscillator from the RC oscillator of the CLKI pin.

## 14.10 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has up to two bits depending upon the device.

Bit 0 is the Brown-out Reset Status bit, $\overline{BOR}$. The $\overline{BOR}$ bit is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if it has been cleared, indicating that a BOR has occurred. When the Brown-out Reset is disabled, the state of the $\overline{BOR}$ bit is unpredictable and is, therefore, not valid at any time.

Bit 1 is the Power-on Reset Status bit, $\overline{POR}$. It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

**TABLE 14-3: TIME-OUT IN VARIOUS SITUATIONS**

| Oscillator Configuration | Power-up | | Brown-out | Wake-up from Sleep |
|---|---|---|---|---|
| | $\overline{PWRTE}$ = 0 | $\overline{PWRTE}$ = 1 | | |
| XT, HS, LP | 72 ms + 1024 TOSC | 1024 TOSC | 72 ms + 1024 TOSC | 1024 TOSC |
| RC | 72 ms | — | 72 ms | — |

**TABLE 14-4: STATUS BITS AND THEIR SIGNIFICANCE**

| $\overline{POR}$ | $\overline{BOR}$ | $\overline{TO}$ | $\overline{PD}$ | Condition |
|---|---|---|---|---|
| 0 | x | 1 | 1 | Power-on Reset |
| 0 | x | 0 | x | Illegal, $\overline{TO}$ is set on $\overline{POR}$ |
| 0 | x | x | 0 | Illegal, $\overline{PD}$ is set on $\overline{POR}$ |
| 1 | 0 | 1 | 1 | Brown-out Reset |
| 1 | 1 | 0 | 1 | WDT Reset |
| 1 | 1 | 0 | 0 | WDT Wake-up |
| 1 | 1 | u | u | $\overline{MCLR}$ Reset during normal operation |
| 1 | 1 | 1 | 0 | $\overline{MCLR}$ Reset during Sleep or Interrupt Wake-up from Sleep |

**Legend:** x = don't care, u = unchanged

**TABLE 14-5: RESET CONDITIONS FOR SPECIAL REGISTERS**

| Condition | Program Counter | Status Register | PCON Register |
|---|---|---|---|
| Power-on Reset | 000h | 0001 1xxx | ---- --0x |
| $\overline{MCLR}$ Reset during normal operation | 000h | 000u uuuu | ---- --uu |
| $\overline{MCLR}$ Reset during Sleep | 000h | 0001 0uuu | ---- --uu |
| WDT Reset | 000h | 0000 1uuu | ---- --uu |
| WDT Wake-up | PC + 1 | uuu0 0uuu | ---- --uu |
| Brown-out Reset | 000h | 0001 1uuu | ---- --u0 |
| Interrupt Wake-up from Sleep | PC + 1(1) | uuu1 0uuu | ---- --uu |

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0'

**Note 1:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**TABLE 14-6: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)**

| Register | Devices | | | | Power-on Reset, Brown-out Reset | $\overline{MCLR}$ Resets, WDT Reset | Wake-up via WDT or Interrupt |
|---|---|---|---|---|---|---|---|
| TRISD | 73A | 74A | 76A | 77A | 1111 1111 | 1111 1111 | uuuu uuuu |
| TRISE | 73A | 74A | 76A | 77A | 0000 -111 | 0000 -111 | uuuu -uuu |
| PIE1 | 73A | 74A | 76A | 77A | r000 0000 | r000 0000 | ruuu uuuu |
| | 73A | 74A | 76A | 77A | 0000 0000 | 0000 0000 | uuuu uuuu |
| PIE2 | 73A | 74A | 76A | 77A | -0-0 0--0 | -0-0 0--0 | -u-u u--u |
| PCON | 73A | 74A | 76A | 77A | ---- --qq | ---- --uu | ---- --uu |
| SSPCON2 | 73A | 74A | 76A | 77A | 0000 0000 | 0000 0000 | uuuu uuuu |
| PR2 | 73A | 74A | 76A | 77A | 1111 1111 | 1111 1111 | 1111 1111 |
| SSPADD | 73A | 74A | 76A | 77A | 0000 0000 | 0000 0000 | uuuu uuuu |
| SSPSTAT | 73A | 74A | 76A | 77A | --00 0000 | --00 0000 | --uu uuuu |
| TXSTA | 73A | 74A | 76A | 77A | 0000 -010 | 0000 -010 | uuuu -uuu |
| SPBRG | 73A | 74A | 76A | 77A | 0000 0000 | 0000 0000 | uuuu uuuu |
| CMCON | 73A | 974 | 76A | 77A | 0000 0111 | 0000 0111 | uuuu uuuu |
| CVRCON | 73A | 74A | 76A | 77A | 000- 0000 | 000- 0000 | uuu- uuuu |
| ADRESL | 73A | 74A | 76A | 77A | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| ADCON1 | 73A | 74A | 76A | 77A | 00-- 0000 | 00-- 0000 | uu-- uuuu |
| EEDATA | 73A | 74A | 76A | 77A | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| EEADR | 73A | 74A | 76A | 77A | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| EEDATH | 73A | 74A | 76A | 77A | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| EEADRH | 73A | 74A | 76A | 77A | xxxx xxxx | uuuu uuuu | uuuu uuuu |
| EECON1 | 73A | 74A | 76A | 77A | x--- x000 | u--- u000 | u--- uuuu |
| EECON2 | 73A | 74A | 76A | 77A | ---- ---- | ---- ---- | ---- ---- |

**Legend:** u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition, r = reserved, maintain clear. Shaded cells indicate conditions do not apply for the designated device.

**Note 1:** One or more bits in INTCON, PIR1 and/or PIR2 will be affected (to cause wake-up).

**2:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

**3:** See Table 14-5 for Reset value for specific condition.

**FIGURE 14-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO $V_{DD}$ VIA RC NETWORK)**

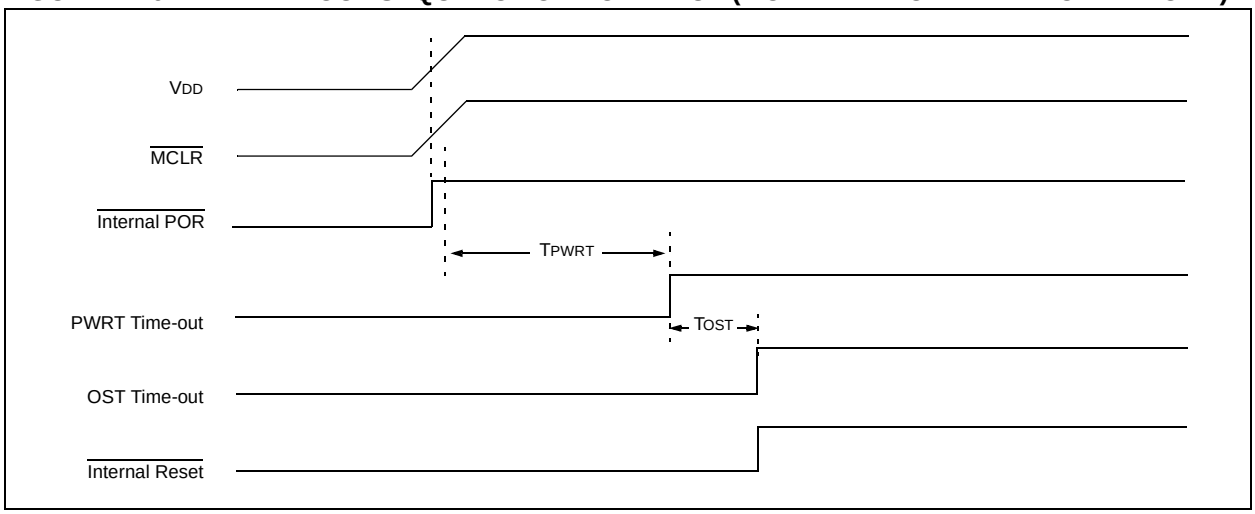


**FIGURE 17-1: PIC16F87XA VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL, EXTENDED)**

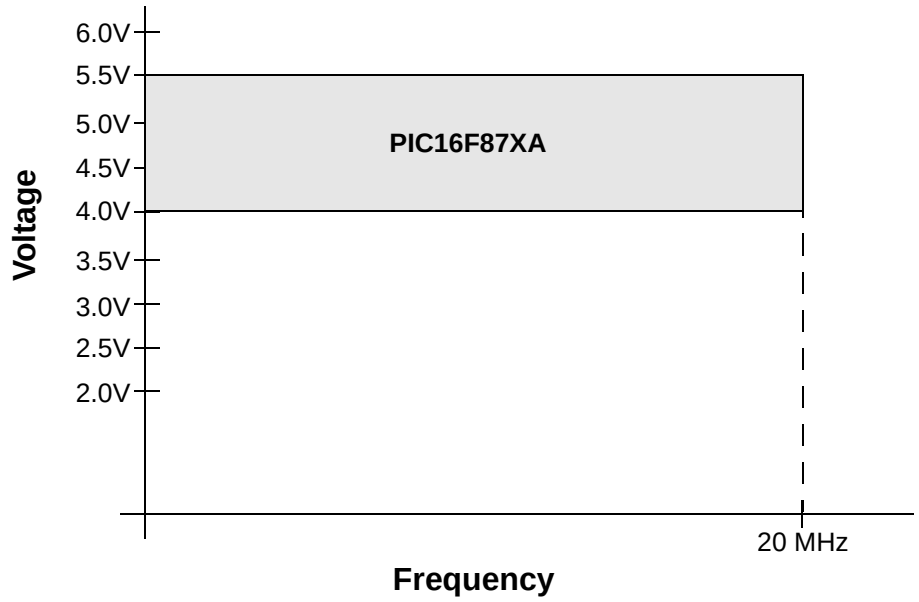
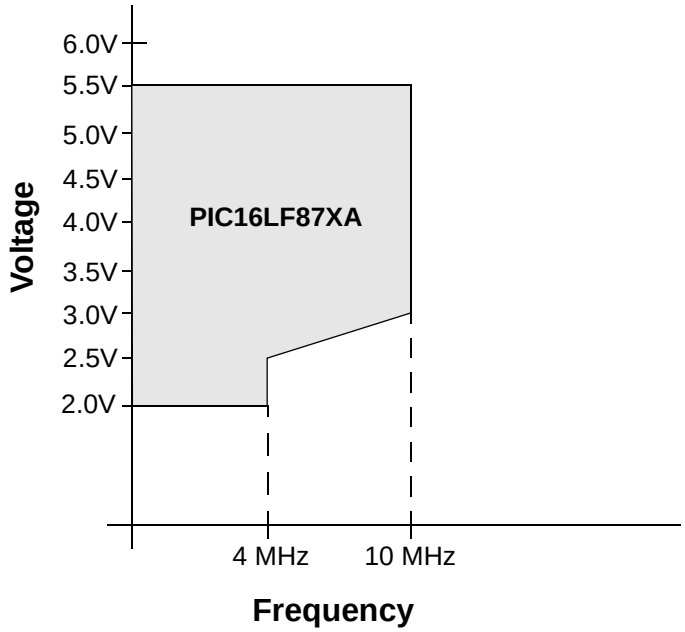



**FIGURE 17-2: PIC16LF87XA VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)**




FMAX = (6.0 MHz/V) (VDDAPPMIN – 2.0V) + 4 MHz

**Note 1:** VDDAPPMIN is the minimum voltage of the PIC® device in the application.

**2:** FMAX has a maximum frequency of 10 MHz.

## 17.3 Timing Parameter Symbology

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST ($I^2C$ specifications only)
4. Ts ($I^2C$ specifications only)

| | | | |
|---|---|---|---|
| **T** | | | |
| F | Frequency | T | Time |

Lowercase letters (pp) and their meanings:

| | | | |
|---|---|---|---|
| **pp** | | | |
| cc | CCP1 | osc | OSC1 |
| ck | CLKO | rd | $\overline{RD}$ |
| cs | $\overline{CS}$ | rw | $\overline{RD}$ or $\overline{WR}$ |
| di | SDI | sc | SCK |
| do | SDO | ss | $\overline{SS}$ |
| dt | Data in | t0 | T0CKI |
| io | I/O port | t1 | T1CKI |
| mc | $\overline{MCLR}$ | wr | $\overline{WR}$ |

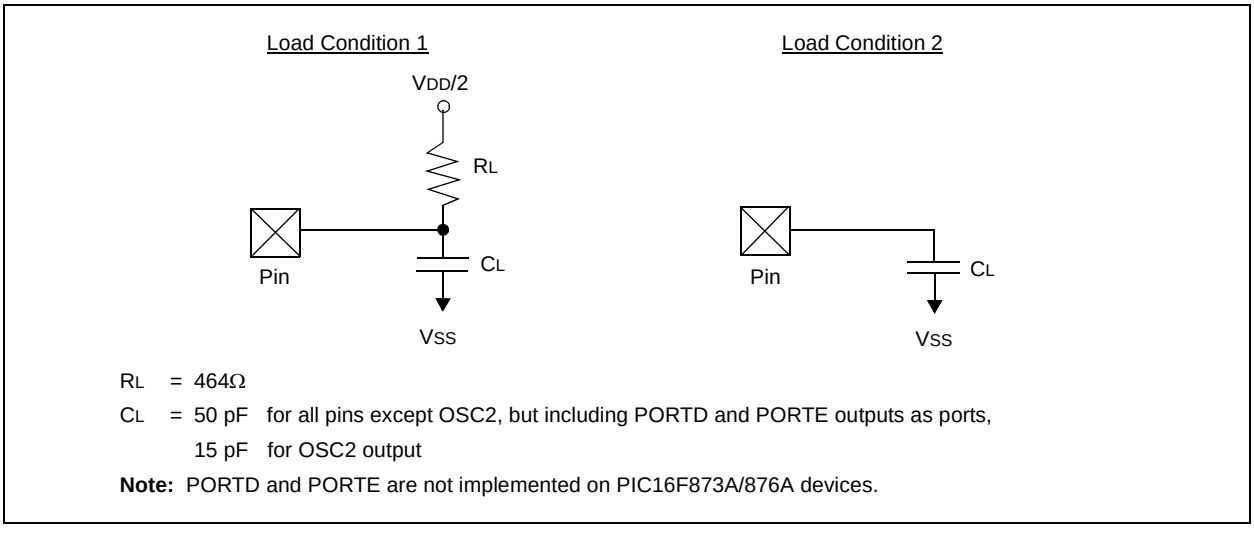
Uppercase letters and their meanings:

| | | | |
|---|---|---|---|
| **S** | | | |
| F | Fall | P | Period |
| H | High | R | Rise |
| I | Invalid (High-impedance) | V | Valid |
| L | Low | Z | High-impedance |
| **$I^2C$ only** | | | |
| AA | output access | High | High |
| BUF | Bus free | Low | Low |

TCC:ST ($I^2C$ specifications only)

| | | | |
|---|---|---|---|
| **CC** | | | |
| HD | Hold | SU | Setup |
| **ST** | | | |
| DAT | Data input hold | STO | Stop condition |
| STA | Start condition | | |

**FIGURE 17-3: LOAD CONDITIONS**

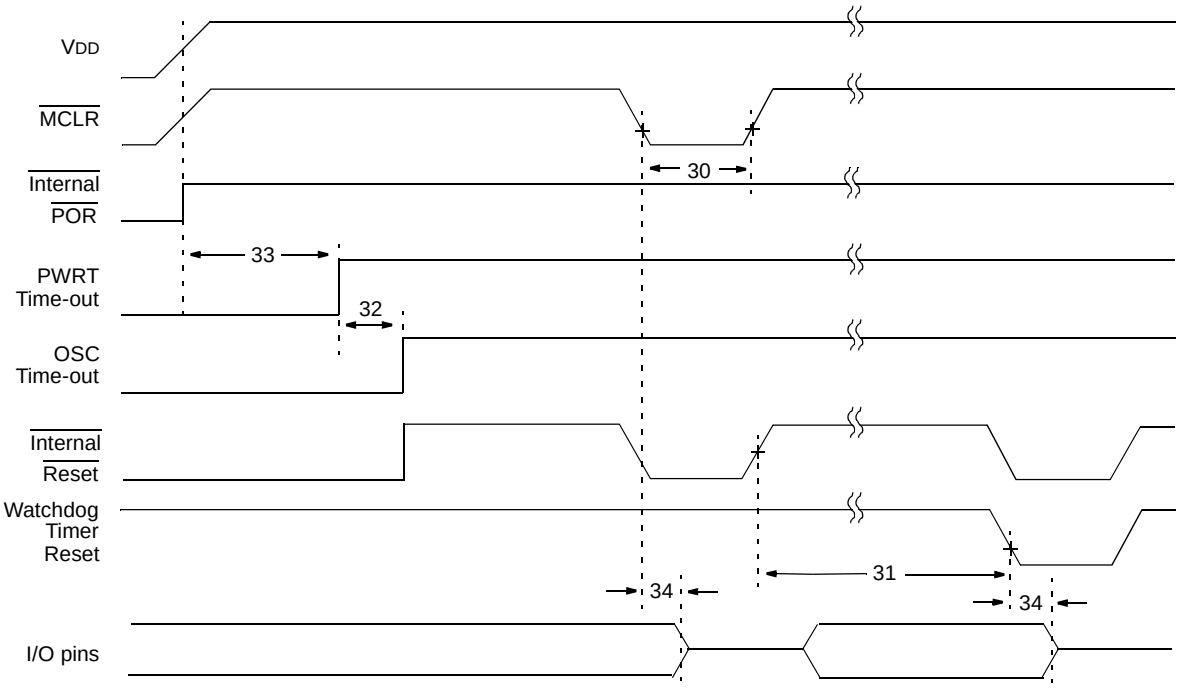



RL = 464Ω

CL = 50 pF for all pins except OSC2, but including PORTD and PORTE outputs as ports,
15 pF for OSC2 output

**Note:** PORTD and PORTE are not implemented on PIC16F873A/876A devices.

**FIGURE 17-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING**




**Note:** Refer to Figure 17-3 for load conditions.

**FIGURE 17-7: BROWN-OUT RESET TIMING**

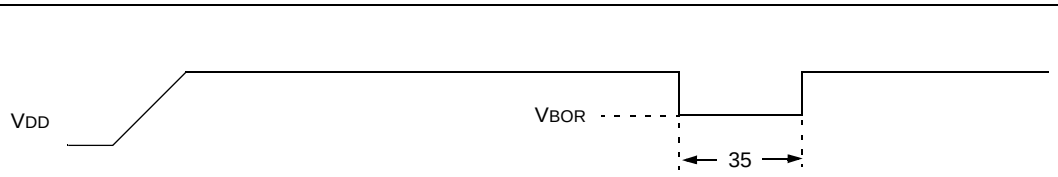



**TABLE 17-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS**

| Param No. | Symbol | Characteristic | Min | Typ† | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2 | — | — | µs | VDD = 5V, -40°C to +85°C |
| 31* | TWDT | Watchdog Timer Time-out Period (no prescaler) | 7 | 18 | 33 | ms | VDD = 5V, -40°C to +85°C |
| 32 | TOST | Oscillation Start-up Timer Period | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| 33* | TPWRT | Power-up Timer Period | 28 | 72 | 132 | ms | VDD = 5V, -40°C to +85°C |
| 34 | TIOZ | I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset | — | — | 2.1 | µs | |
| 35 | TBOR | Brown-out Reset Pulse Width | 100 | — | — | µs | VDD ≤ VBOR (D005) |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 18-3: TYPICAL IDD vs. FOSC OVER VDD (XT MODE)**

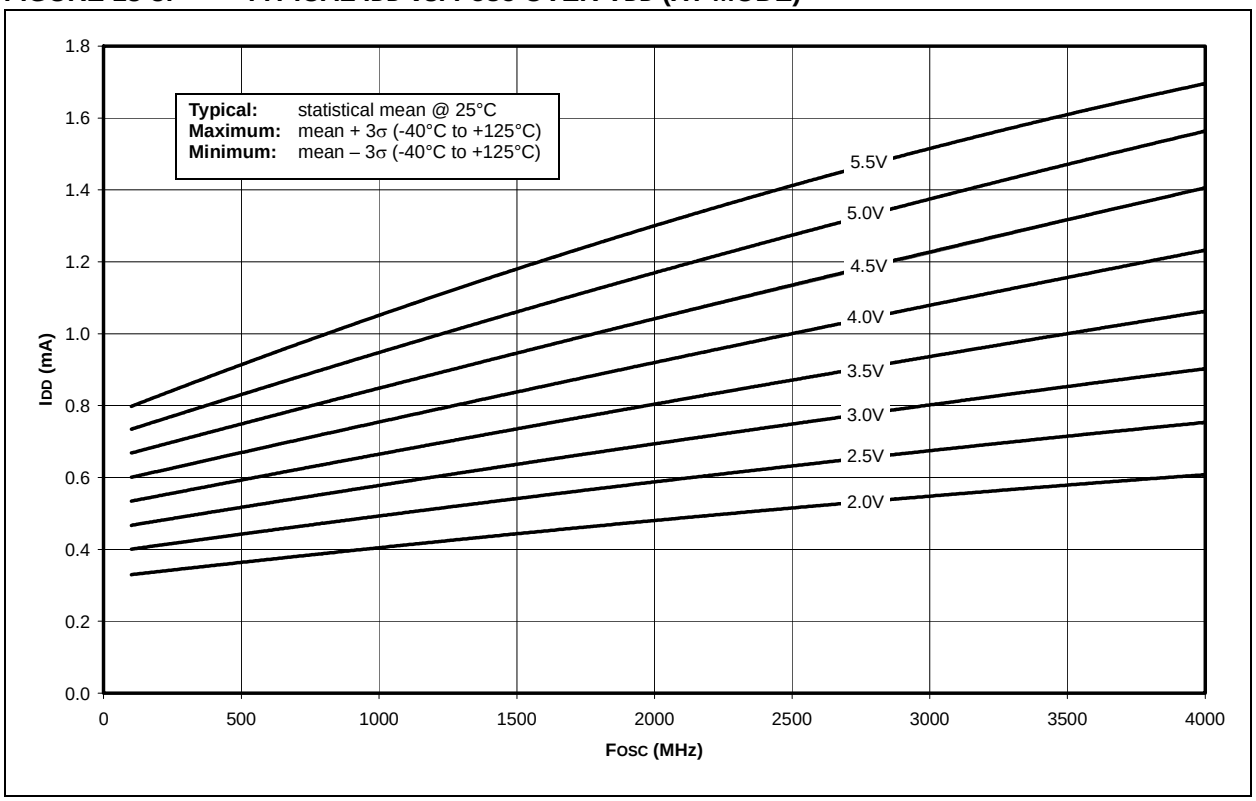



**FIGURE 18-4: MAXIMUM IDD vs. FOSC OVER VDD (XT MODE)**

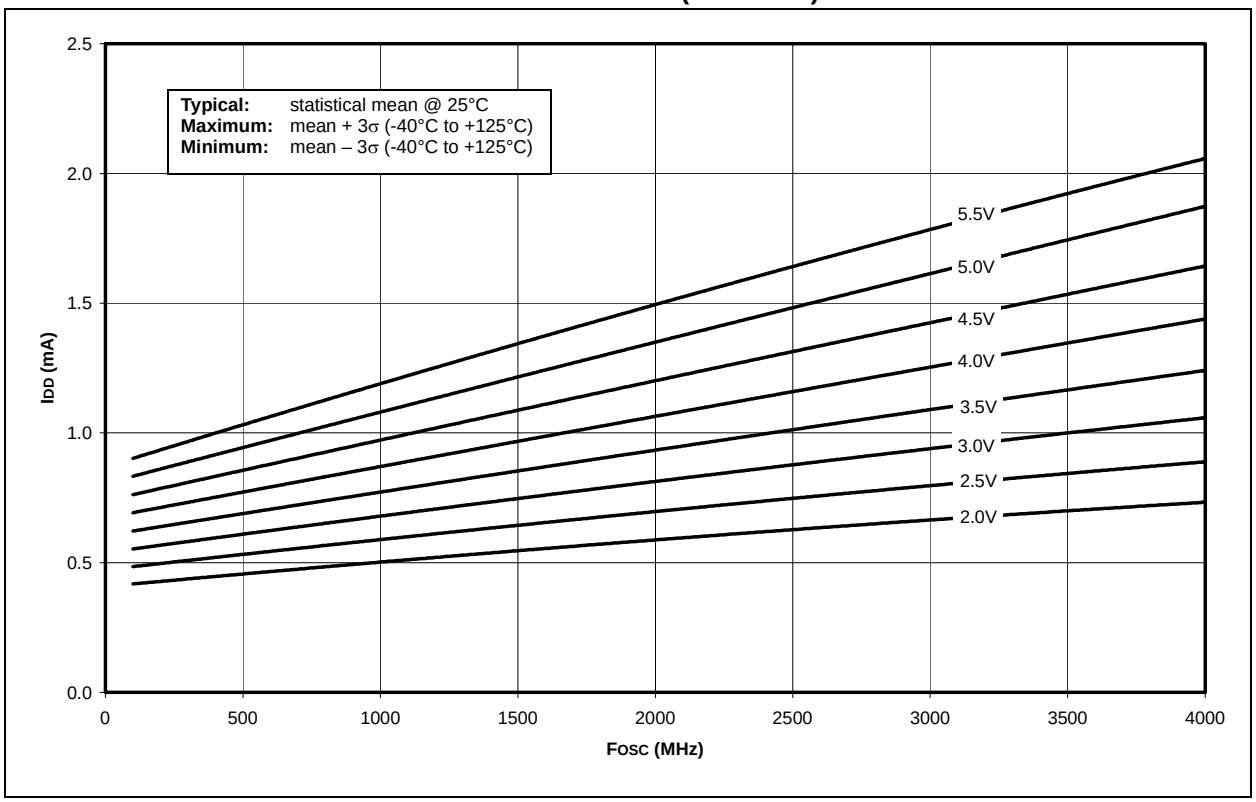


**FIGURE 18-11: TYPICAL AND MAXIMUM ΔITMR1 VS. VDD OVER TEMPERATURE (-10°C TO +70°C, TIMER1 WITH OSCILLATOR, XTAL = 32 kHz, C1 AND C2 = 47 pF)**

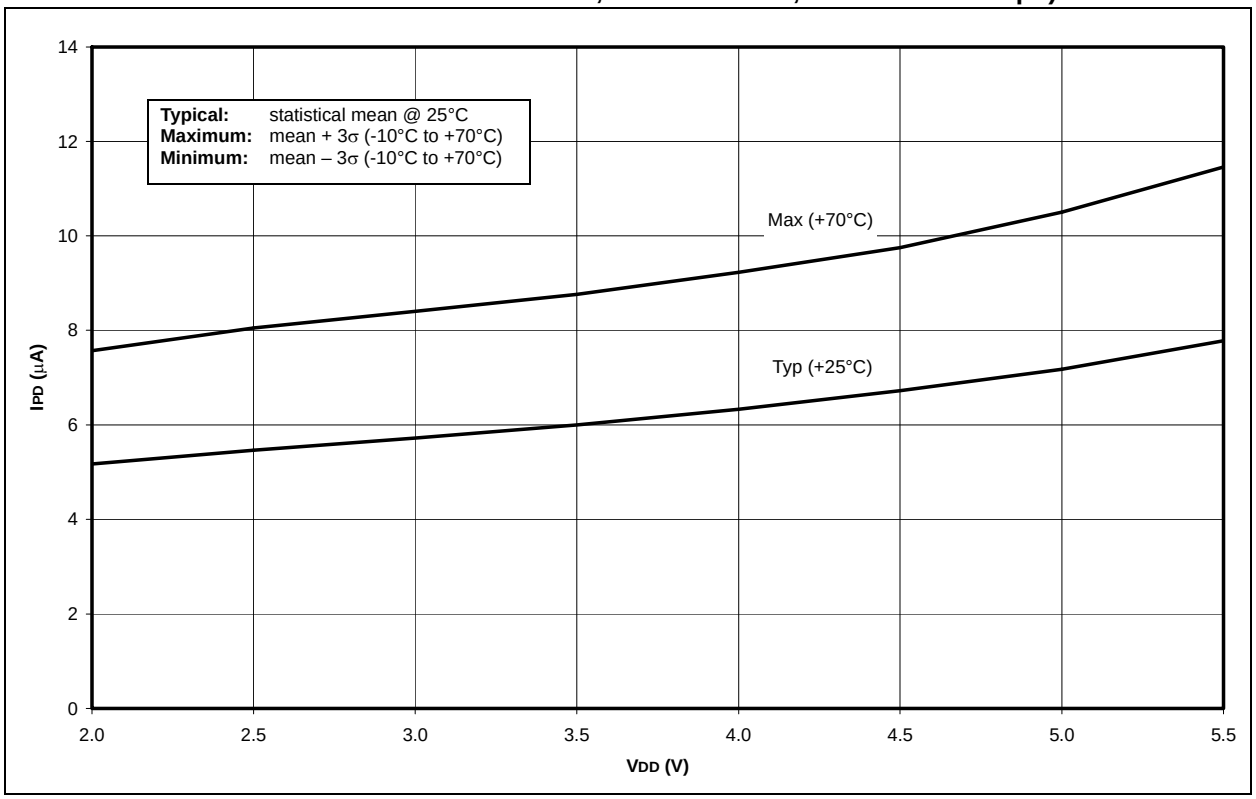
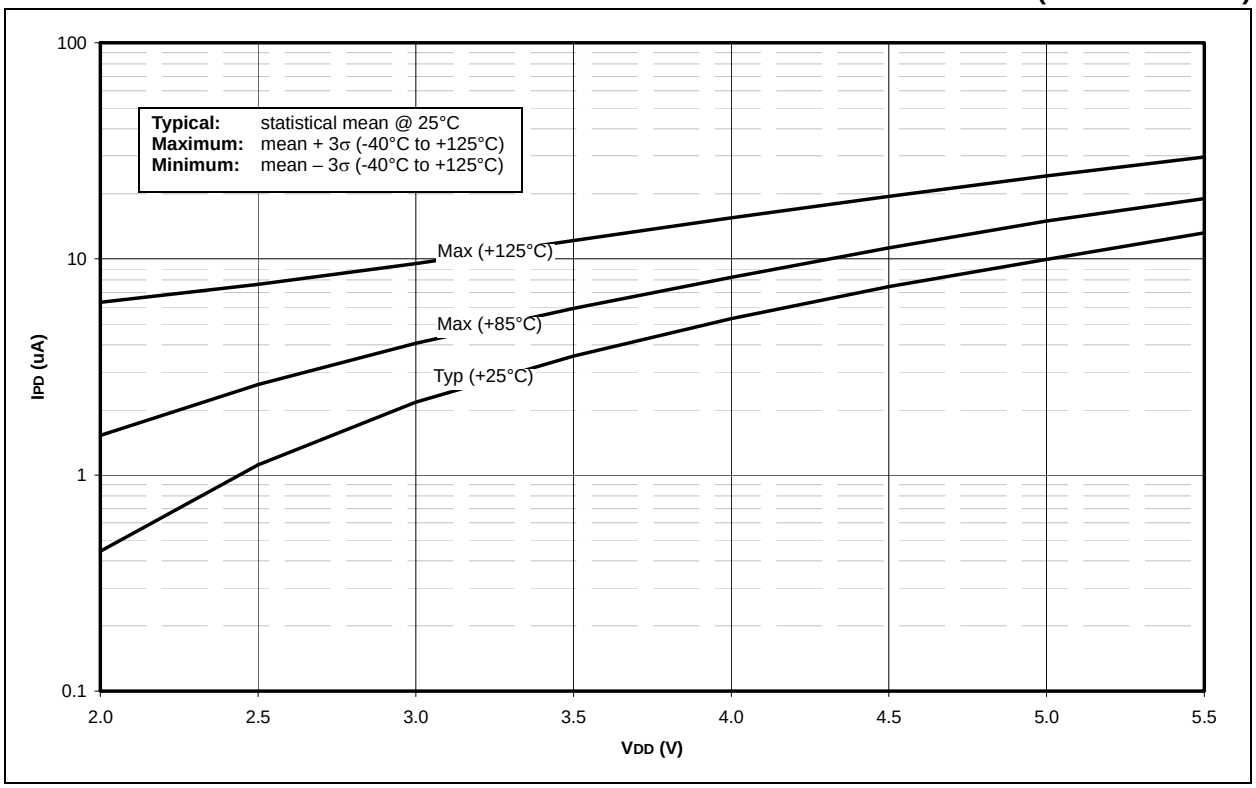
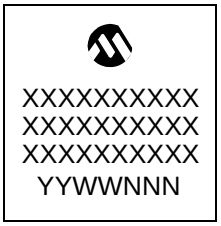



**FIGURE 18-12: TYPICAL AND MAXIMUM ΔIWDT VS. VDD OVER TEMPERATURE (WDT ENABLED)**



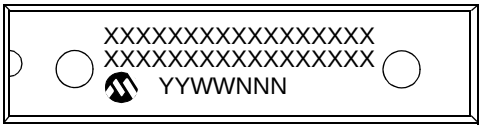
**Package Marking Information (Cont'd)**

44-Lead QFN

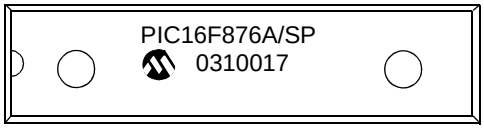



Example

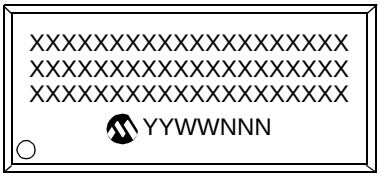

28-Lead PDIP (Skinny DIP)




Example




28-Lead SOIC

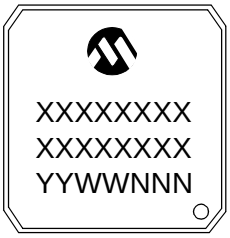



Example


28-Lead SSOP


Example


28-Lead QFN




Example

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