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Details

Product Status	Obsolete
Core Processor	HC11
Core Size	8-Bit
Speed	2MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	38
Program Memory Size	12KB (12K x 8)
Program Memory Type	OTP
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LCC (J-Lead)
Supplier Device Package	52-PLCC (19.1x19.1)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68s711e9cfn2

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<http://www.motorola.com/mcu/>

The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
May, 2001	3.1	4.4.3.1 System Configuration Register — Addition to NOCOP bit description	88
		Added 11.22 EPROM Characteristics	251
June, 2001	3.2	11.22 EPROM Characteristics — For clarity, addition to note 2 following the table	251

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There should be a single pullup resistor near the MCU interrupt input pin (typically 4.7 k Ω). There must also be an interlock mechanism at each interrupt source so that the source holds the interrupt line low until the MCU recognizes and acknowledges the interrupt request. If one or more interrupt sources are still pending after the MCU services a request, the interrupt line will still be held low and the MCU will be interrupted again as soon as the interrupt mask bit in the MCU is cleared (normally upon return from an interrupt). Refer to [Section 5. Resets and Interrupts](#).

V_{PPE} is the input for the 12-volt nominal programming voltage required for EPROM/OTPROM programming. On devices without EPROM/OTPROM, this pin is only an \overline{XIRQ} input.

2.9 MODA and MODB (MODA/ \overline{LIR} and MODB/ V_{STBY})

During reset, MODA and MODB select one of the four operating modes:

- Single-chip mode
- Expanded mode
- Test mode
- Bootstrap mode

Refer to [Section 4. Operating Modes and On-Chip Memory](#).

After the operating mode has been selected, the load instruction register (\overline{LIR}) pin provides an open-drain output to indicate that execution of an instruction has begun. A series of E-clock cycles occurs during execution of each instruction. The \overline{LIR} signal goes low during the first E-clock cycle of each instruction (opcode fetch). This output is provided for assistance in program debugging.

The V_{STBY} pin is used to input random-access memory (RAM) standby power. When the voltage on this pin is more than one MOS threshold (about 0.7 volts) above the V_{DD} voltage, the internal RAM and part of the reset logic are powered from this signal rather than the V_{DD} input. This allows RAM contents to be retained without V_{DD} power applied to the MCU. Reset must be driven low before V_{DD} is removed and must remain low until V_{DD} has been restored to a valid level.

Table 3-2. Instruction Set (Sheet 2 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BEQ (rel)	Branch if = Zero	? Z = 1	REL	27	rr	3	—	—	—	—	—	—	—	—
BGE (rel)	Branch if Δ Zero	? N \oplus V = 0	REL	2C	rr	3	—	—	—	—	—	—	—	—
BGT (rel)	Branch if > Zero	? Z + (N \oplus V) = 0	REL	2E	rr	3	—	—	—	—	—	—	—	—
BHI (rel)	Branch if Higher	? C + Z = 0	REL	22	rr	3	—	—	—	—	—	—	—	—
BHS (rel)	Branch if Higher or Same	? C = 0	REL	24	rr	3	—	—	—	—	—	—	—	—
BITA (opr)	Bit(s) Test A with Memory	A • M	A IMM	85	ii	2	—	—	—	—	Δ	Δ	0	—
			A DIR	95	dd	3								
			A EXT	B5	hh ll	4								
			A IND,X	A5	ff	4								
			A IND,Y	A5	ff	5								
BITB (opr)	Bit(s) Test B with Memory	B • M	B IMM	C5	ii	2	—	—	—	—	Δ	Δ	0	—
			B DIR	D5	dd	3								
			B EXT	F5	hh ll	4								
			B IND,X	E5	ff	4								
			B IND,Y	E5	ff	5								
BLE (rel)	Branch if Δ Zero	? Z + (N \oplus V) = 1	REL	2F	rr	3	—	—	—	—	—	—	—	—
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	3	—	—	—	—	—	—	—	—
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	3	—	—	—	—	—	—	—	—
BLT (rel)	Branch if < Zero	? N \oplus V = 1	REL	2D	rr	3	—	—	—	—	—	—	—	—
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	3	—	—	—	—	—	—	—	—
BNE (rel)	Branch if not = Zero	? Z = 0	REL	26	rr	3	—	—	—	—	—	—	—	—
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	3	—	—	—	—	—	—	—	—
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	3	—	—	—	—	—	—	—	—
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0	DIR	13	dd mm rr	6	—	—	—	—	—	—	—	—
			IND,X	1F	ff mm rr	7								
			IND,Y	1F	ff mm rr	8								
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	3	—	—	—	—	—	—	—	—
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? (M) • mm = 0	DIR	12	dd mm rr	6	—	—	—	—	—	—	—	—
			IND,X	1E	ff mm rr	7								
			IND,Y	1E	ff mm rr	8								
BSET (opr) (msk)	Set Bit(s)	M + mm \Rightarrow M	DIR	14	dd mm	6	—	—	—	—	Δ	Δ	0	—
			IND,X	1C	ff mm	7								
			IND,Y	1C	ff mm	8								
BSR (rel)	Branch to Subroutine	See Figure 3–2	REL	8D	rr	6	—	—	—	—	—	—	—	—
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	3	—	—	—	—	—	—	—	—
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	3	—	—	—	—	—	—	—	—
CBA	Compare A to B	A – B	INH	11	—	2	—	—	—	—	Δ	Δ	Δ	Δ
CLC	Clear Carry Bit	0 \Rightarrow C	INH	0C	—	2	—	—	—	—	—	—	—	0
CLI	Clear Interrupt Mask	0 \Rightarrow I	INH	0E	—	2	—	—	—	0	—	—	—	—
CLR (opr)	Clear Memory Byte	0 \Rightarrow M	EXT	7F	hh ll	6	—	—	—	—	0	1	0	0
			IND,X	6F	ff	6								
			IND,Y	6F	ff	7								
CLRA	Clear Accumulator A	0 \Rightarrow A	A INH	4F	—	2	—	—	—	—	0	1	0	0
CLRB	Clear Accumulator B	0 \Rightarrow B	B INH	5F	—	2	—	—	—	—	0	1	0	0
CLV	Clear Overflow Flag	0 \Rightarrow V	INH	0A	—	2	—	—	—	—	—	—	0	—
CMPA (opr)	Compare A to Memory	A – M	A IMM	81	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			A DIR	91	dd	3								
			A EXT	B1	hh ll	4								
			A IND,X	A1	ff	4								
			A IND,Y	A1	ff	5								

Table 3-2. Instruction Set (Sheet 3 of 7)

Mnemonic	Operation	Description	Addressing Mode	Instruction			Condition Codes							
				Opcode	Operand	Cycles	S	X	H	I	N	Z	V	C
CMPB (opr)	Compare B to Memory	B – M	B IMM	C1	ii	2	—	—	—	—	Δ	Δ	Δ	Δ
			B DIR	D1	dd	3								
			B EXT	F1	hh ll	4								
			B IND,X	E1	ff	4								
			B IND,Y	18 E1	ff	5								
COM (opr)	Ones Complement Memory Byte	\$FF – M ⇒ M	EXT IND,X IND,Y	73	hh ll	6	—	—	—	—	Δ	Δ	0	1
				63	ff	6								
				18 63	ff	7								
COMA	Ones Complement A	\$FF – A ⇒ A	A INH	43	—	2	—	—	—	—	Δ	Δ	0	1
COMB	Ones Complement B	\$FF – B ⇒ B	B INH	53	—	2	—	—	—	—	Δ	Δ	0	1
CPD (opr)	Compare D to Memory 16-Bit	D – M : M + 1	IMM DIR EXT IND,X IND,Y	1A 83	jj kk	5	—	—	—	—	Δ	Δ	Δ	Δ
				1A 93	dd	6								
				1A B3	hh ll	7								
				1A A3	ff	7								
				CD A3	ff	7								
CPX (opr)	Compare X to Memory 16-Bit	IX – M : M + 1	IMM DIR EXT IND,X IND,Y	8C	jj kk	4	—	—	—	—	Δ	Δ	Δ	Δ
				9C	dd	5								
				BC	hh ll	6								
				AC	ff	6								
				CD AC	ff	7								
CPY (opr)	Compare Y to Memory 16-Bit	IY – M : M + 1	IMM DIR EXT IND,X IND,Y	18 8C	jj kk	5	—	—	—	—	Δ	Δ	Δ	Δ
				18 9C	dd	6								
				18 BC	hh ll	7								
				1A AC	ff	7								
				18 AC	ff	7								
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19	—	2	—	—	—	—	Δ	Δ	Δ	Δ
DEC (opr)	Decrement Memory Byte	M – 1 ⇒ M	EXT IND,X IND,Y	7A	hh ll	6	—	—	—	—	Δ	Δ	Δ	—
				6A	ff	6								
				18 6A	ff	7								
DECA	Decrement Accumulator A	A – 1 ⇒ A	A INH	4A	—	2	—	—	—	—	Δ	Δ	Δ	—
DECB	Decrement Accumulator B	B – 1 ⇒ B	B INH	5A	—	2	—	—	—	—	Δ	Δ	Δ	—
DES	Decrement Stack Pointer	SP – 1 ⇒ SP	INH	34	—	3	—	—	—	—	—	—	—	—
DEX	Decrement Index Register X	IX – 1 ⇒ IX	INH	09	—	3	—	—	—	—	—	Δ	—	—
DEY	Decrement Index Register Y	IY – 1 ⇒ IY	INH	18 09	—	4	—	—	—	—	—	Δ	—	—
EORA (opr)	Exclusive OR A with Memory	A ⊕ M ⇒ A	A IMM A DIR A EXT A IND,X A IND,Y	88	ii	2	—	—	—	—	Δ	Δ	0	—
				98	dd	3								
				B8	hh ll	4								
				A8	ff	4								
				18 A8	ff	5								
EORB (opr)	Exclusive OR B with Memory	B ⊕ M ⇒ B	B IMM B DIR B EXT B IND,X B IND,Y	C8	ii	2	—	—	—	—	Δ	Δ	0	—
				D8	dd	3								
				F8	hh ll	4								
				E8	ff	4								
				18 E8	ff	5								
FDIV	Fractional Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	03	—	41	—	—	—	—	—	Δ	Δ	Δ
IDIV	Integer Divide 16 by 16	D / IX ⇒ IX; r ⇒ D	INH	02	—	41	—	—	—	—	—	Δ	0	Δ
INC (opr)	Increment Memory Byte	M + 1 ⇒ M	EXT IND,X IND,Y	7C	hh ll	6	—	—	—	—	Δ	Δ	Δ	—
				6C	ff	6								
				18 6C	ff	7								
INCA	Increment Accumulator A	A + 1 ⇒ A	A INH	4C	—	2	—	—	—	—	Δ	Δ	Δ	—

4.4.3.3 System Configuration Options Register

The 8-bit, special-purpose system configuration options register (OPTION) sets internal system configuration options during initialization. The time protected control bits, IRQE, DLY, and CR[1:0], can be written only once after a reset and then they become read-only. This minimizes the possibility of any accidental changes to the system configuration.

Address: \$1039

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	ADPU	CSEL	IRQE ⁽¹⁾	DLY ⁽¹⁾	CME		CR1 ⁽¹⁾	CR0 ⁽¹⁾
Write:								
Reset:	0	0	0	1	0	0	0	0

1. Can be written only once in first 64 cycles out of reset in normal modes or at any time during special modes.


 = Unimplemented

Figure 4-13. System Configuration Options Register (OPTION)

ADPU — Analog-to-Digital Converter Power-Up Bit

Refer to [Section 10. Analog-to-Digital \(A/D\) Converter](#).

CSEL — Clock Select Bit

Selects alternate clock source for on-chip EEPROM charge pump.

Refer to [4.6.1 EEPROM and CONFIG Programming and Erasure](#) for more information on EEPROM use.

CSEL also selects the clock source for the A/D converter, a function discussed in [Section 10. Analog-to-Digital \(A/D\) Converter](#).

IRQE — Configure $\overline{\text{IRQ}}$ for Edge-Sensitive Only Operation Bit

Refer to [Section 5. Resets and Interrupts](#).

DLY — Enable Oscillator Startup Delay Bit

0 = The oscillator startup delay coming out of stop mode is bypassed and the MCU resumes processing within about four bus cycles.

1 = A delay of approximately 4000 E-clock cycles is imposed as the MCU is started up from the stop power-saving mode. This delay allows the crystal oscillator to stabilize.

Address: \$1026

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	DDRA7	PAEWN	PAMOD	PEDGE	DDRA3	I4/O5	RTR1	RTR0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 6-2. Pulse Accumulator Control Register (PACTL)

DDRA7 — Data Direction for Port A Bit 7

Overridden if an output compare function is configured to control the PA7 pin

0 = Input

1 = Output

The pulse accumulator uses port A bit 7 as the PAI input, but the pin can also be used as general-purpose I/O or as an output compare.

NOTE: *Even when port A bit 7 is configured as an output, the pin still drives the input to the pulse accumulator.*

PAEN — Pulse Accumulator System Enable Bit

Refer to [Section 9. Timing System](#).

PAMOD — Pulse Accumulator Mode Bit

Refer to [Section 9. Timing System](#).

PEDGE — Pulse Accumulator Edge Control Bit

Refer to [Section 9. Timing System](#).

DDRA3 — Data Direction for Port A Bit 3

This bit is overridden if an output compare function is configured to control the PA3 pin.

0 = Input

1 = Output

I4/O5 — Input Capture 4/Output Compare 5 Bit

Refer to [Section 9. Timing System](#).

RTR[1:0] — RTI Interrupt Rate Select Bits

Refer to [Section 9. Timing System](#).

Full handshake modes use port C pins and the STRA and STRB lines. Input and output handshake modes are supported, and output handshake mode has a 3-stated variation. STRA is an edge-detecting input and STRB is a handshake output. Control and enable bits are located in the PIOC register.

In full input handshake mode, the MCU asserts STRB to signal an external system that it is ready to latch data. Port C logic levels are latched into PORTCL when the STRA line is asserted by the external system. The MCU then negates STRB. The MCU reasserts STRB after the PORTCL register is read. In this mode, a mix of latched inputs, static inputs, and static outputs is allowed on port C, differentiated by the data direction bits and use of the PORTC and PORTCL registers.

In full output handshake mode, the MCU writes data to PORTCL which, in turn, asserts the STRB output to indicate that data is ready. The external system reads port C data and asserts the STRA input to acknowledge that data has been received.

In the 3-state variation of output handshake mode, lines intended as 3-state handshake outputs are configured as inputs by clearing the corresponding DDRC bits. The MCU writes data to PORTCL and asserts STRB. The external system responds by activating the STRA input, which forces the MCU to drive the data in PORTC out on all of the port C lines. After the trailing edge of the active signal on STRA, the MCU negates the STRB signal. The 3-state mode variation does not allow part of port C to be used for static inputs while other port C pins are being used for handshake outputs. Refer to the [6.9 Parallel I/O Control Register](#) for further information.

there is a loss of efficiency because of the extra bit time for each character (address bit) required for all characters.

7.7 SCI Error Detection

Three error conditions – SCDR overrun, received bit noise, and framing – can occur during generation of SCI system interrupts. Three bits (OR, NF, and FE) in the serial communications status register (SCSR) indicate if one of these error conditions exists.

The overrun error (OR) bit is set when the next byte is ready to be transferred from the receive shift register to the SCDR and the SCDR is already full (RDRF bit is set). When an overrun error occurs, the data that caused the overrun is lost and the data that was already in SCDR is not disturbed. The OR is cleared when the SCSR is read (with OR set), followed by a read of the SCDR.

The noise flag (NF) bit is set if there is noise on any of the received bits, including the start and stop bits. The NF bit is not set until the RDRF flag is set. The NF bit is cleared when the SCSR is read (with FE equal to 1) followed by a read of the SCDR.

When no stop bit is detected in the received data character, the framing error (FE) bit is set. FE is set at the same time as the RDRF. If the byte received causes both framing and overrun errors, the processor only recognizes the overrun error. The framing error flag inhibits further transfer of data into the SCDR until it is cleared. The FE bit is cleared when the SCSR is read (with FE equal to 1) followed by a read of the SCDR.

interrupt mask for TDRE. When TIE is 0, TDRE must be polled. When TIE and TDRE are 1, an interrupt is requested.

The TC flag indicates the transmitter has completed the queue. The TCIE bit is the local interrupt mask for TC. When TCIE is 0, TC must be polled. When TCIE is 1 and TC is 1, an interrupt is requested.

Writing a 0 to TE requests that the transmitter stop when it can. The transmitter completes any transmission in progress before actually shutting down. Only an MCU reset can cause the transmitter to stop and shut down immediately. If TE is written to 0 when the transmitter is already idle, the pin reverts to its general-purpose I/O function (synchronized to the bit-rate clock). If anything is being transmitted when TE is written to 0, that character is completed before the pin reverts to general-purpose I/O, but any other characters waiting in the transmit queue are lost. The TC and TDRE flags are set at the completion of this last character, even though TE has been disabled.

7.10 Receiver Flags

The SCI receiver has five status flags, three of which can generate interrupt requests. The status flags are set by the SCI logic in response to specific conditions in the receiver. These flags can be read (polled) at any time by software. Refer to [Figure 7-10](#), which shows SCI interrupt arbitration.

When an overrun takes place, the new character is lost, and the character that was in its way in the parallel RDR is undisturbed. RDRF is set when a character has been received and transferred into the parallel RDR. The OR flag is set instead of RDRF if overrun occurs. A new character is ready to be transferred into RDR before a previous character is read from RDR.

The NF and FE flags provide additional information about the character in the RDR, but do not generate interrupt requests.

The last receiver status flag and interrupt source come from the IDLE flag. The RxD line is idle if it has constantly been at logic 1 for a full character time. The IDLE flag is set only after the RxD line has been

8.5 Clock Phase and Polarity Controls

Software can select one of four combinations of serial clock phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock, and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements.

When CPHA equals 0, the \overline{SS} line must be negated and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while \overline{SS} is low, a write collision error results.

When CPHA equals 1, the \overline{SS} line can remain low between successive transfers.

8.6 SPI Signals

This subsection contains descriptions of the four SPI signals:

- Master in/slave out (MISO)
- Master out/slave in (MOSI)
- Serial clock (SCK)
- Slave select (\overline{SS})

Any SPI output line must have its corresponding data direction bit in DDRD register set. If the DDR bit is clear, that line is disconnected from the SPI logic and becomes a general-purpose input. All SPI input lines are forced to act as inputs regardless of the state of the corresponding DDR bits in DDRD register.

8.8.3 Serial Peripheral Data I/O Register

The SPDR is used when transmitting or receiving data on the serial bus. Only a write to this register initiates transmission or reception of a byte, and this only occurs in the master device. At the completion of transferring a byte of data, the SPIF status bit is set in both the master and slave devices.

A read of the SPDR is actually a read of a buffer. To prevent an overrun and the loss of the byte that caused the overrun, the first SPIF must be cleared by the time a second transfer of data from the shift register to the read buffer is initiated.

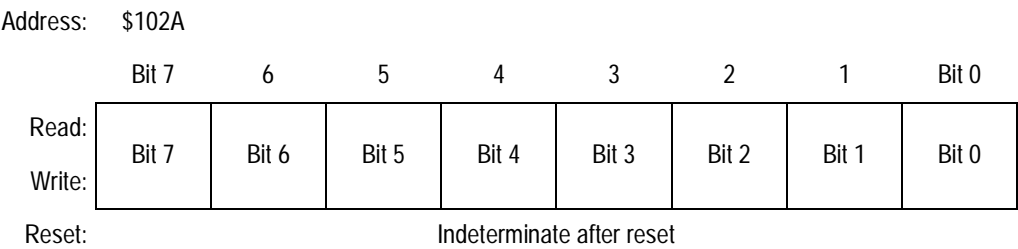


Figure 8-5. Serial Peripheral Data I/O Register (SPDR)

SPI is double buffered in and single buffered out.

9.7 Computer Operating Properly (COP) Watchdog Function

The clocking chain for the COP function, tapped off of the main timer divider chain, is only superficially related to the main timer system. The CR[1:0] bits in the OPTION register and the NOCOP bit in the CONFIG register determine the status of the COP function. One additional register, COPRST, is used to arm and clear the COP watchdog reset system. Refer to [Section 5. Resets and Interrupts](#) for a more detailed discussion of the COP function.

9.8 Pulse Accumulator

The M68HC11 Family of MCUs has an 8-bit counter that can be configured to operate either as a simple event counter or for gated time accumulation, depending on the state of the PAMOD bit in the PACTL register. Refer to the pulse accumulator block diagram, [Figure 9-24](#). In the event counting mode, the 8-bit counter is clocked to increasing values by an external pin. The maximum clocking rate for the external event counting mode is the E clock divided by two. In gated time accumulation mode, a free-running E-clock divide-by-64 signal drives the 8-bit counter, but only while the external PAI pin is activated. Refer to [Table 9-6](#). The pulse accumulator counter can be read or written at any time.

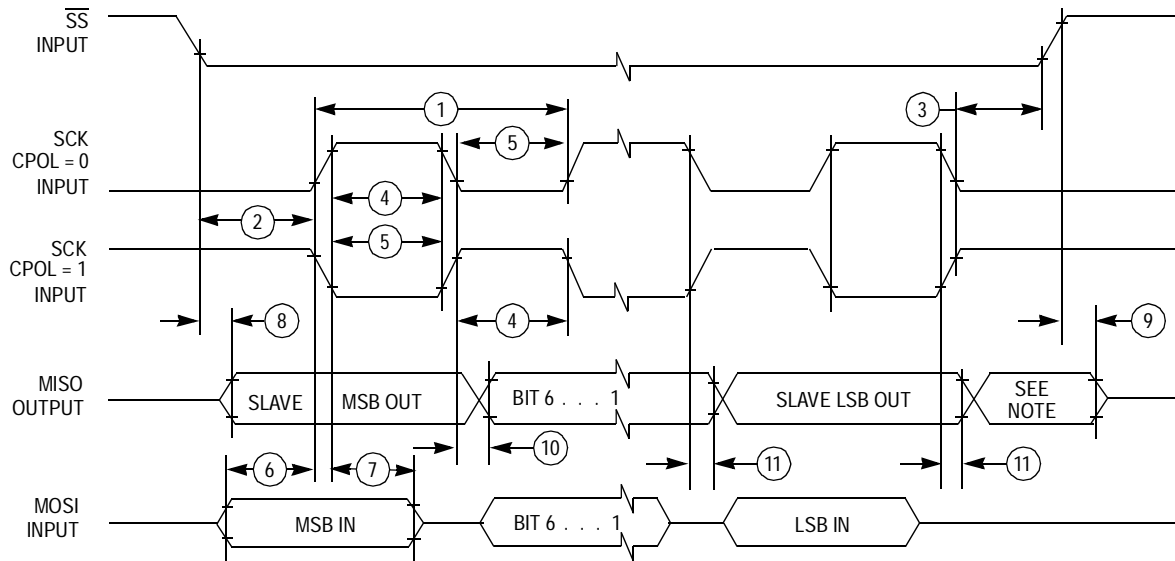
Section 10. Analog-to-Digital (A/D) Converter

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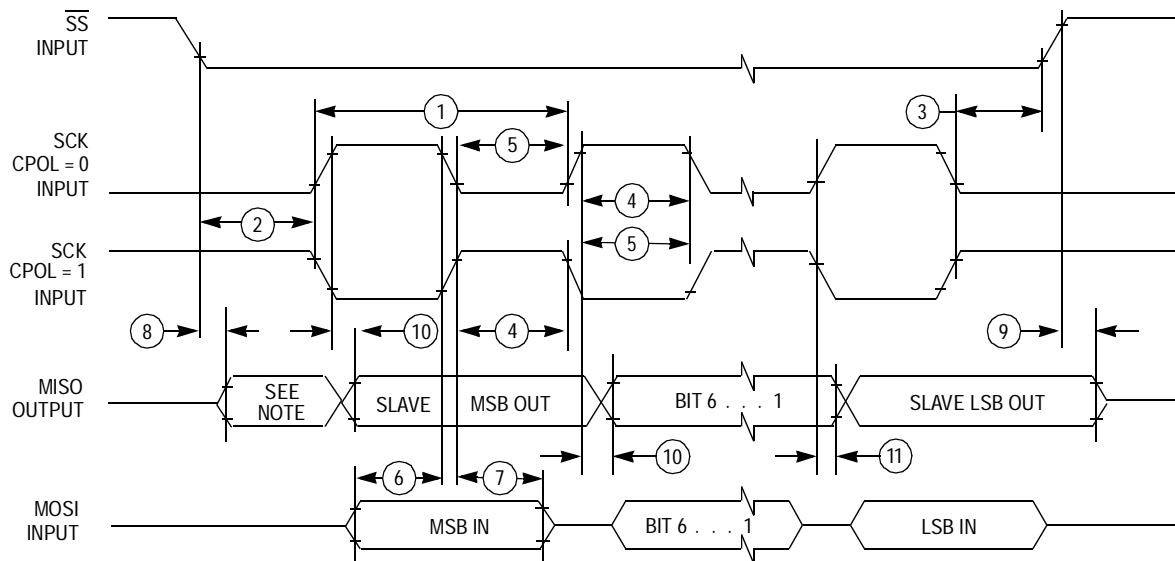
10.2 Introduction

The analog-to-digital (A/D) system, a successive approximation converter, uses an all-capacitive charge redistribution technique to convert analog signals to digital values.



Note: Not defined but normally MSB of character just received

A) SPI Slave Timing (CPHA = 0)



Note: Not defined but normally LSB of character previously transmitted

B) SPI Slave Timing (CPHA = 1)

Figure 11-15. SPI Timing Diagram (Sheet 2 of 2)

11.20 EEPROM Characteristics

Characteristic ⁽¹⁾	Temperature Range			Unit
	–40 to 85°C	–40 to 105°C	–40 to 125°C	
Programming time ⁽²⁾ < 1.0 MHz, RCO enabled 1.0 to 2.0 MHz, RCO disabled ≥ 2.0 MHz (or anytime RCO enabled)	10 20 10	15 Must use RCO 15	20 Must use RCO 20	ms
Erase time ⁽²⁾ Byte, row, and bulk	10	10	10	ms
Write/erase endurance	10,000	10,000	10,000	Cycles
Data retention	10	10	10	Years

1. $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H

2. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure when the E-clock frequency is below 1.0 MHz.

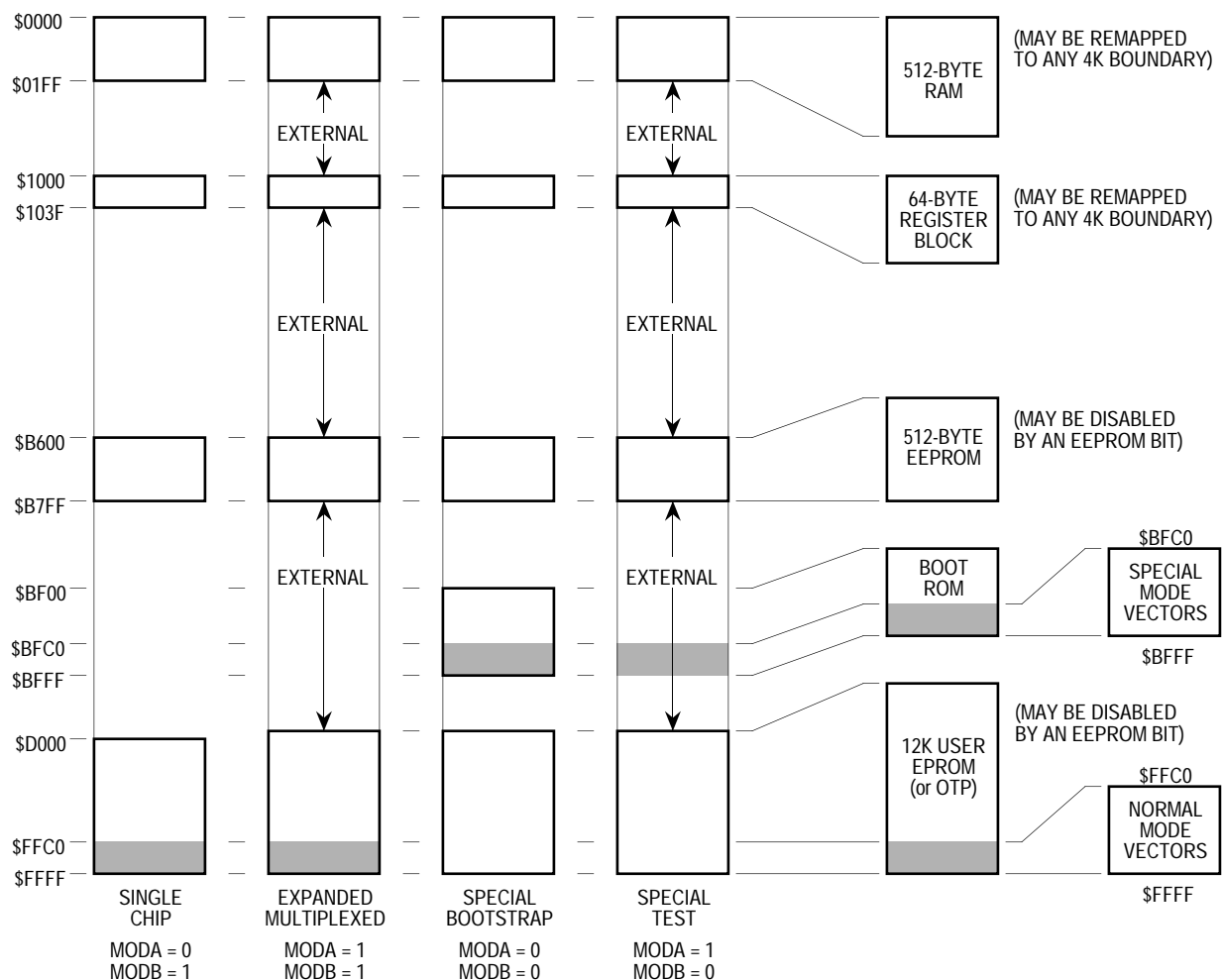
11.21 MC68L11E9 EEPROM Characteristics

Characteristic ⁽¹⁾	Temperature Range –20 to 70°C	Unit
Programming time ⁽²⁾ 3 V, $E \leq 2.0 \text{ MHz}$, RCO enabled 5 V, $E \leq 2.0 \text{ MHz}$, RCO enabled	25 10	ms
Erase time ⁽²⁾ (byte, row, and bulk) 3 V, $E \leq 2.0 \text{ MHz}$, RCO enabled 5 V, $E \leq 2.0 \text{ MHz}$, RCO enabled	25 10	ms
Write/erase endurance	10,000	Cycles
Data retention	10	Years

1. $V_{DD} = 3.0 \text{ Vdc}$ to 5.5 Vdc , $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H

2. The RC oscillator (RCO) must be enabled (by setting the CSEL bit in the OPTION register) for EEPROM programming and erasure.

Application Note



OTE: Software can change some aspects of the memory map after reset.

Figure 1. MC68HC711E9 Composite Memory Map

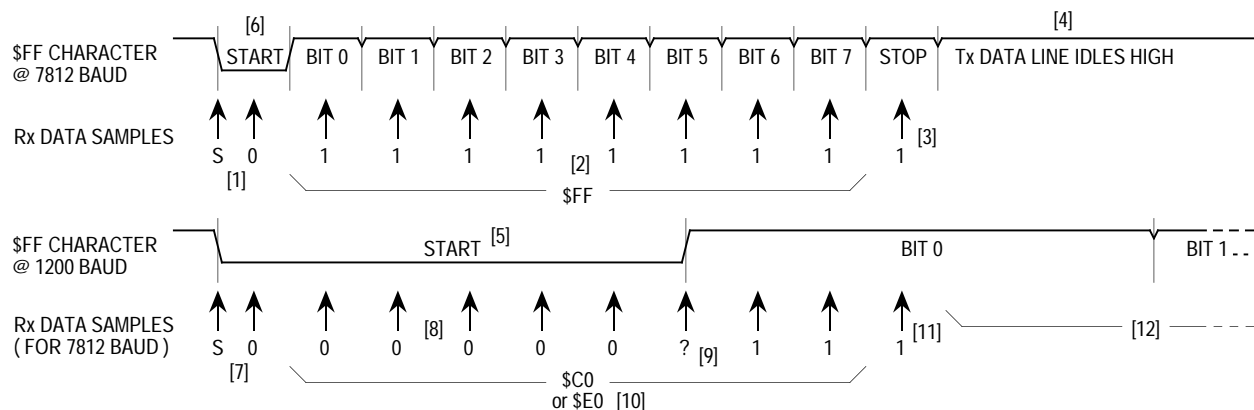


Figure 2. Automatic Detection of Baud Rate

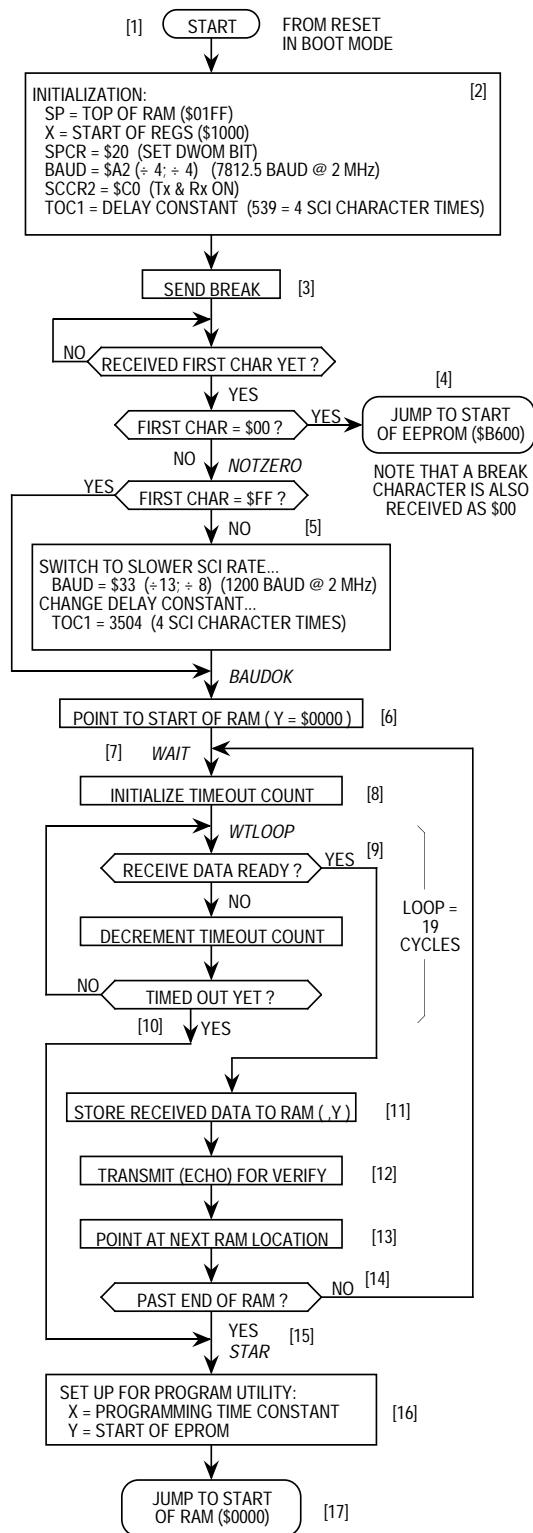


Figure 3. MC68HC711E9 Bootloader Flowchart

The program will inform the user that it is working on converting the file from S records to binary. This process will take from 30 seconds to a few minutes, depending on the computer.

A prompt reading, "Comm port open?" will appear at the end of the file conversion. This is the last chance to ensure that everything is properly configured on the EVBU. Pressing [RETURN] will send the bootcode to the target MC68HC711E9. The program then informs the user that the bootload code is being sent to the target, and the results of the echoing of this code are displayed on the screen.

Another prompt reading "Programming is ready to begin. Are you?" will appear. Turn on the 12-volt programming power supply and press [RETURN] to start the actual programming of the target EPROM.

A count of the byte being verified will be updated continually on the screen as the programming progresses. Any failures will be flagged as they occur.

When programming is complete, a message will be displayed as well as a prompt requesting the user to press [RETURN] to quit.

Turn off the 12-volt programming power supply before turning off 5 volts to the EVBU.