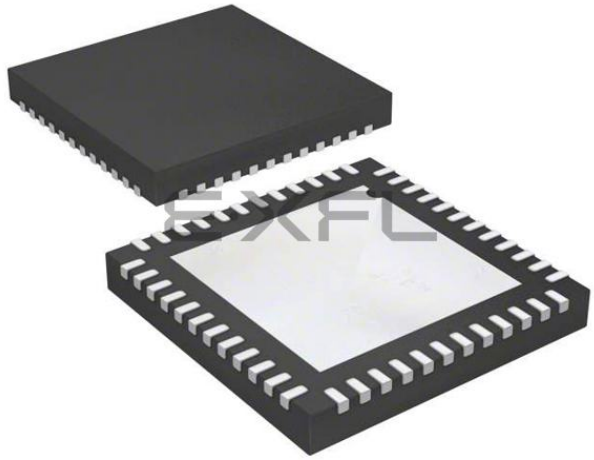

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM7®
Core Size	16/32-Bit
Speed	20.48MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	9
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 32
Voltage - Supply (Vcc/Vdd)	3.5V ~ 18V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 115°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad, CSP
Supplier Device Package	48-LFCSP-VQ (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aduc7036ccpz-rl

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.5 V to 18 V, VREF = 1.2 V internal reference, f_{CORE} = 20.48 MHz (unless otherwise noted) driven from external 32.768 kHz watch crystal or on-chip precision oscillator. All specifications T_A = −40°C to +115°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS					
Conversion Rate[1]	Chop off, ADC normal operating mode	4		8000	Hz
	Chop on, ADC normal operating mode	4		2600	Hz
	Chop on, ADC low power mode	1		650	Hz
Current Channel					
No Missing Codes[1]	Valid for all ADC update rates and ADC modes	16			Bits
Integral Nonlinearity[1, 2]			±10	±60	ppm of FSR
Offset Error[2, 3, 4, 5]	Chop off, 1 LSB = (36.6/gain) μV	−10	±3	+10	LSB
Offset Error[1, 3, 6]	Chop on	−2	±0.5	+2	μV
Offset Error[1, 3]	Chop on, low power or low power plus mode, MCU powered down	100	−50	−300	nV
Offset Error[1, 3]	Chop on, normal mode	+0.5	−1.25	−3	μV
Offset Error Drift[6]	Chop off, valid for ADC gains of 4 to 64, normal mode		0.03		LSB/°C
Offset Error Drift[6]	Chop off, valid for ADC gains of 128 to 512, normal mode		30		nV/°C
Offset Error Drift[6]	Chop on		10		nV/°C
Total Gain Error[1, 3, 7, 8, 9, 10]	Normal mode	−0.5	±0.1	+0.5	%
Total Gain Error[1, 3, 7, 9]	Low power mode, using ADCREF MMR	−4	±0.2	+4	%
Total Gain Error[1, 3, 7, 9, 11]	Low power plus mode, using precision VREF	−1	±0.2	+1	%
Gain Drift			3		ppm/°C
PGA Gain Mismatch Error			±0.1		%
Output Noise[1, 12]	4 Hz update rate, gain = 512, ADCFLT = 0xBF1D		60	90	nV rms
	4 Hz update rate, gain = 512, ADCFLT = 0x3F1D		75	115	nV rms
	10 Hz update rate, gain = 512, ADCFLT = 0x961F		100	150	nV rms
	10 Hz update rate, gain = 512, ADCFLT = 0x161F		120	180	nV rms
	1 kHz update rate, gain ≥ 64, ADCFLT = 0x8101		0.8	1.2	μV rms
	1 kHz update rate, gain ≥ 64, ADCFLT = 0x0101		1	1.5	μV rms
	1 kHz update rate, gain = 512, ADCFLT = 0x0007		0.6	0.9	μV rms
	1 kHz update rate, gain = 32, ADCFLT = 0x0007		0.8	1.2	μV rms
	1 kHz update rate, gain = 8, ADCFLT = 0x8101		2.1	4.1	μV rms
	1 kHz update rate, gain = 8, ADCFLT = 0x0007		1.6	2.4	μV rms
	1 kHz update rate, gain = 8, ADCFLT = 0x0101		2.6	3.9	μV rms
	1 kHz update rate, gain = 4, ADCFLT = 0x0007		2.0	2.8	μV rms
	8 kHz update rate, gain = 32, ADCFLT = 0x0000		2.5	3.5	μV rms
	8 kHz update rate, gain = 4, ADCFLT = 0x0000		14	21	μV rms
	ADC low power mode, f_{ADC} = 10 Hz, gain = 128		1.25	1.9	μV rms
	ADC low power mode, f_{ADC} = 1 Hz, gain = 128		0.35	0.5	μV rms
	ADC low power plus mode, f_{ADC} = 1 Hz, gain = 512		0.1	0.15	μV rms
	ADC low power plus mode, f_{ADC} = 250 Hz, gain = 512		0.6	0.9	μV rms

Table 5. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge		0.5 t_{SL}		ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge[1, 2]			(3 × t_{UCLK}) + (2 × t_{HCLK})	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge[1, 2]	4 × t_{UCLK}			ns
t_{DF}	Data output fall time		3.5		ns
t_{DR}	Data output rise time		3.5		ns
t_{SR}	SCLK rise time		3.5		ns
t_{SF}	SCLK fall time		3.5		ns
t_{DOCS}	Data output valid after $\overline{SS}$ edge[2]			(3 × t_{UCLK}) + (2 × t_{HCLK})	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge		0.5 t_{SL}		ns

[1] t_{HCLK} depends on the clock divider (CD) bits in the POWCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 48.8 ns. It corresponds to the 20.48 MHz internal clock from the PLL before the clock divider.

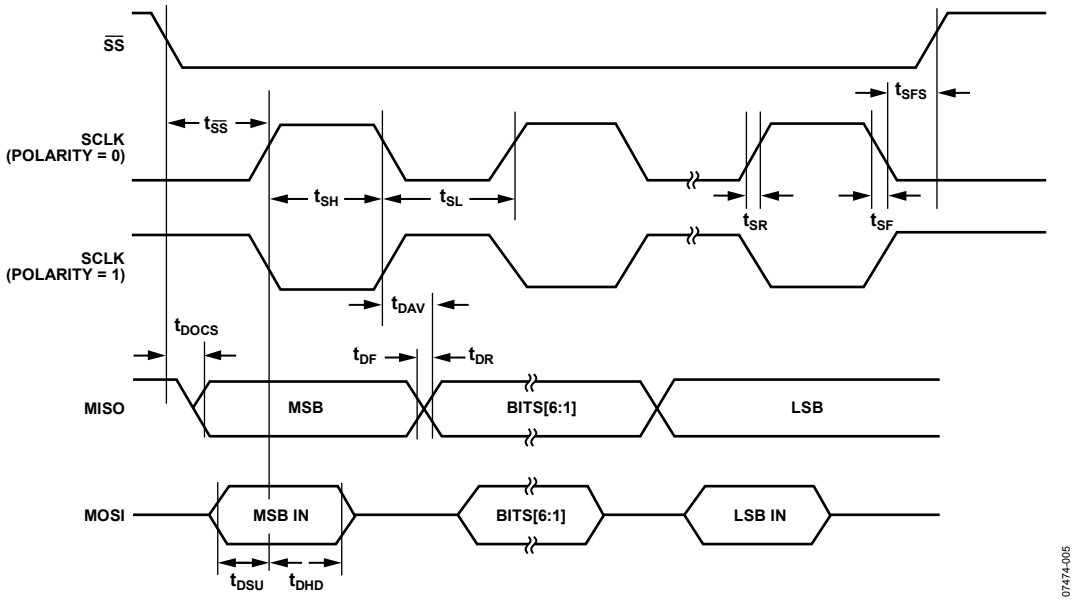

Figure 5. SPI Slave Mode Timing—Phase Mode = 0

ABSOLUTE MAXIMUM RATINGS

T_A = −40°C to +115°C, unless otherwise noted.

Table 6.

Parameter	Rating
AGND to DGND to VSS to IO_VSS	−0.3 V to +0.3 V
VBAT to AGND	−22 V to +40 V
VDD to VSS	−0.3 V to +33 V
VDD to VSS for 1 sec	−0.3 V to +40 V
LIN to IO_VSS	−16 V to +40 V
STI and WU to IO_VSS	−3 V to +33 V
Wake-Up Continuous Current	50 mA
High Voltage I/O Pins Short-Circuit Current	100 mA
Digital I/O Voltage to DGND	−0.3 V to REG_DVDD + 0.3 V
VREF to AGND	−0.3 V to REG_AVDD + 0.3 V
ADC Inputs to AGND	−0.3 V to REG_AVDD + 0.3 V
ESD Human Body Model (HBM) Rating	
HBM-ADI0082 (Based on ANSI/ESD STM5.1-2007). All Pins except LIN and VBAT.	1 kV
LIN and VBAT	±6 kV
IEC 61000-4-2 for LIN and VBAT	±7 kV
Storage Temperature	125°C
Junction Temperature	
Transient	150°C
Continuous	130°C
Lead Temperature	
Soldering Reflow (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

FEE0DAT and FEE1DAT Registers

Name: FEE0DAT and FEE1DAT

Address: 0xFFFF0E0C and 0xFFFF0E8C

Default Value: 0x0000

Access: Read/write access

Function: This 16-bit register contains the data either read from or to be written to the Flash/EE memory.

FEE0MOD and FEE1MOD Registers

Name: FEE0MOD and FEE1MOD

Address: 0xFFFF0E04 and 0xFFFF0E84

Default Value: 0x00

Access: Read/write access

Function: These registers are written by user code to configure the mode of operation of the Flash/EE memory controllers.

Table 15. FEE0MOD and FEE1MOD MMR Bit Designations

Bit	Description[1]
15 to 7	Not used. These bits are reserved for future functionality and should be written as 0 by user code.
6, 5	Flash/EE security lock bits. These bits must be written as [6:5] = 10 to complete the Flash/EE security protect sequence.
4	Flash/EE controller command complete interrupt enable. Set to 1 by user code to enable the Flash/EE controller to generate an interrupt upon completion of a Flash/EE command. Cleared to disable the generation of a Flash/EE interrupt upon completion of a Flash/EE command.
3	Flash/EE erase/write enable. Set by user code to enable the Flash/EE erase and write access via FEExCON. Cleared by user code to disable the Flash/EE erase and write access via FEExCON.
2	Reserved. Should be written as 0.
1	Flash/EE controller abort enable. Set to 1 by user code to enable the Flash/EE controller abort functionality.
0	Reserved. Should be written as 0.

[1] The x represents 0 or 1, designating Flash/EE Block 0 or Flash/EE Block 1.

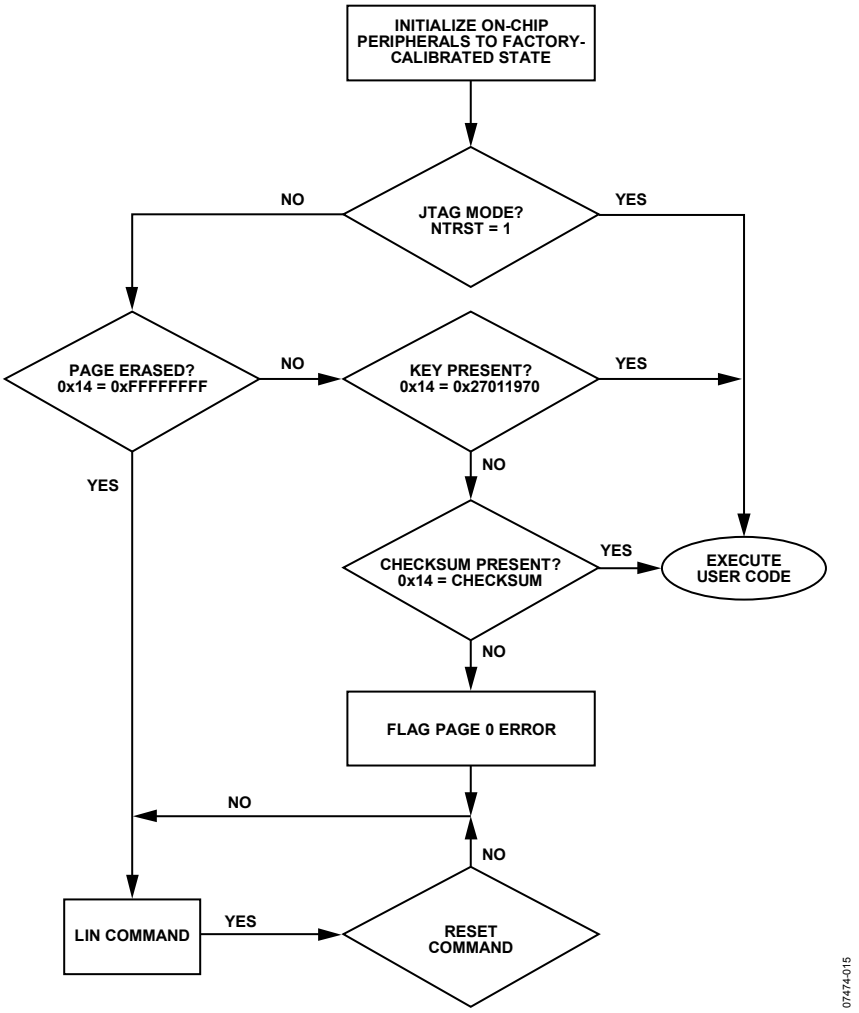

Figure 15. ADuC7036BCPZ and ADuC7036CCPZ Kernel Flowchart

Address	Name	Byte	Access Type	Default Value	Description
0x0340	T2LD	4	RW	0x00000000	Timer2 load register. See the Timer2—Wake-Up Timer and Timer2 Load Register sections.
0x0344	T2VAL	4	R	0xFFFFFFFF	Timer2 value register. See the Timer2—Wake-Up Timer and Timer2 Value Register sections.
0x0348	T2CON	2	RW	0x0000	Timer2 control MMR. See the Timer2—Wake-Up Timer and Timer2 Control Register sections and Table 55.
0x034C	T2CLRI	1	W	N/A	Timer2 interrupt clear register. See the Timer2—Wake-Up Timer and Timer2 Clear Register sections.
0x0360	T3LD	2	RW	0x0040	Timer3 load register. See the Timer3—Watchdog Timer and Timer3 Load Register sections.
0x0364	T3VAL	2	R	0x0040	Timer3 value register. See the Timer3—Watchdog Timer and Timer3 Value Register sections.
0x0368	T3CON	2	RW	0x0000	Timer3 control MMR. See the Timer3—Watchdog Timer, Timer3 Value Register, and Timer 3 Control Register sections and Table 56.
0x036C	T3CLRI[1]	1	W	N/A	Timer3 interrupt clear register. See the Timer3—Watchdog Timer and Timer3 Clear Register sections.
0x0380	T4LD	2	RW	0x0000	Timer4 load register. See the Timer4—STI Timer and Timer4 Load Register sections.
0x0384	T4VAL	2	R	0xFFFF	Timer4 value register. See the Timer4—STI Timer and Timer4 Value Register sections.
0x0388	T4CON	4	RW	0x00000000	Timer4 control MMR. See the Timer4—STI Timer and Timer4 Control Register sections and Table 57.
0x038C	T4CLRI	1	W	N/A	Timer4 interrupt clear register. See the Timer4—STI Timer and Timer4 Clear Register sections.
0x0390	T4CAP	2	R	0x0000	Timer4 capture register. See the Timer4—STI Timer section.

[1] Updated by kernel.

Table 22. PLL Base Address = 0xFFFF0400

Address	Name	Byte	Access Type	Default Value	Description
0x0400	PLLSTA	1	R	N/A	PLL status MMR. See the PLLSTA Register section and Table 44.
0x0404	POWKEY0	4	W	N/A	POWCON prewrite key. See the POWCON Prewrite Key section.
0x0408	POWCON	1	RW	0x79	Power control and core speed control register. See the POWCON Register section.
0x040C	POWKEY1	4	W	N/A	POWCON postwrite key. See the POWCON Postwrite Key section.
0x0410	PLLKEY0	4	W	N/A	PLLCON prewrite key. See the PLLCON Prewrite Key section.
0x0414	PLLCON	1	RW	0x00	PLL clock source selection MMR. See the PLLCON Register section.
0x0418	PLLKEY1	4	W	N/A	PLLCON postwrite key. See the PLLCON Postwrite Key section.
0x042C	OSC0TRM	1	RW	0xX8	Low power oscillator trim bits MMR. See the OSC0TRM Register section.
0x0440	OSC0CON	1	RW	0x00	Low power oscillator calibration control MMR. See the OSC0CON Register section.
0x0444	OSC0STA	1	R	0x00	Low power oscillator calibration status MMR. See the OSC0STA Register section.
0x0448	0SC0VAL0	2	R	0x0000	Low power oscillator calibration Counter 0 MMR. See the OSC0VAL0 Register section.
0x044C	OSC0VAL1	2	R	0x0000	Low power oscillator calibration Counter 1 MMR. See the OSC0VAL1 Register section.

Voltage/Temperature Channel ADC (V-/T-ADC)

The voltage/temperature channel ADC (V-/T-ADC) converts additional battery parameters, such as voltage and temperature. The input to this channel can be multiplexed from one of three input sources: an external voltage, an external temperature sensor circuit, or an on-chip temperature sensor.

As with the current channel ADC (I-ADC), the V-/T-ADC employs an identical Σ-Δ conversion technique, including a modified Sinc3 low-pass filter to provide a valid 16-bit data conversion result at programmable output rates from 4 Hz to 8 kHz. An external RC filter network is not required because this is internally implemented in the voltage channel.

The external battery voltage (VBAT) is routed to the ADC input via an on-chip, high voltage (divide-by-24), resistive attenuator. The voltage attenuator buffers are automatically enabled when the voltage attenuator input is selected.

The battery temperature can be derived through the on-chip temperature sensor or an external temperature sensor input. The time to a first valid (fully settled) result after an input channel switch on the voltage/temperature channel is three ADC conversion cycles with chop mode disabled.

This ADC is again buffered but, unlike the current channel, has a fixed input range of 0 V to V_{REF} on VTEMP and 0 V to 28.8 V on VBAT (assuming an internal 1.2 V reference). A top-level overview of this ADC signal chain is shown in Figure 19.

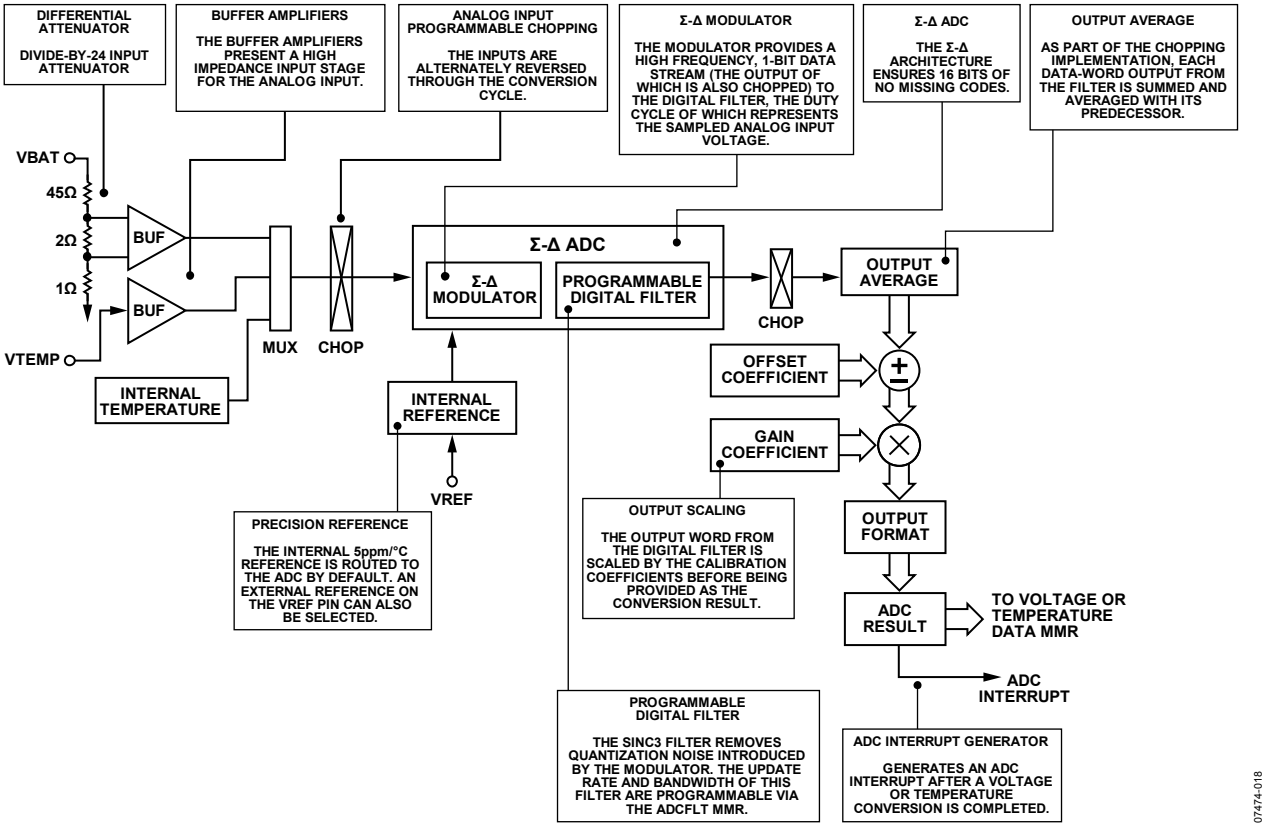

Figure 19. Voltage/Temperature ADC, Top-Level Overview

ADC GROUND SWITCH

The ADuC7036 features an integrated ground switch pin, GND_SW (Pin 15). This switch allows the user to dynamically disconnect ground from external devices and, instead, use either a direct connection to ground or a connection to ground using a 20 kΩ resistor. This additional resistor can be used to reduce the number of external components required for an NTC circuit. The ground switch feature can be used for reducing power consumption on application-specific boards.

An example application is shown in Figure 20.

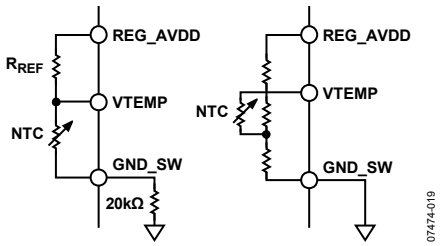

Figure 20. Example External Temperature Sensor Circuits

Figure 20 shows an external NTC used in two modes, with one using the internal 20 kΩ resistor and the second showing a direct connection to ground via GND_SW.

ADCCFG[7] controls the connection of the ground switch to ground, and ADCMDE[6] controls GND_SW resistance, as shown in Figure 21.

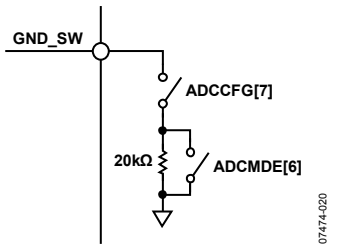

Figure 21. Internal Ground Switch Configuration

The possible combinations of ADCCFG[7] and ADCMDE[6] are shown in Table 31.

Table 31. GND_SW Configuration

ADCCFG[7]	ADCMDE[6]	GND_SW
0	0	Floating
0	1	Floating
1	0	Direct connection to ground
1	1	Connected to ground via 20 kΩ resistor

ADC NOISE PERFORMANCE TABLES

Table 32, Table 33, and Table 34 list the output rms noise in microvolts for some typical output update rates on the I-ADC and V-/T-ADC. The numbers are typical and are generated at a differential input voltage of 0 V. The output rms noise is specified as the standard deviation (or 1 Σ) of the distribution of ADC output codes collected when the ADC input voltage is at a dc voltage. It is expressed in microvolts rms (μV rms).

Table 32. Typical Output RMS Noise of Current Channel ADC in Normal Power Mode

		ADC Input Range									
ADCFLT	Data Update Rate	±2.3 mV (512)	±4.6 mV (256)	±4.68 mV (128)	±18.75 mV (64)	±37.5 mV (32)	±75 mV (16)	±150 mV (8)	±300 mV (4[1])	±600 mV (2[1])	±1.2 V (1[1])
0xBF1D	4 Hz	0.040 μV	0.040 μV	0.043 μV	0.045 μV	0.087 μV	0.175 μV	0.35 μV	0.7 μV	1.4 μV	2.8 μV
0x961F	10 Hz	0.060 μV	0.060 μV	0.060 μV	0.065 μV	0.087 μV	0.175 μV	0.35 μV	0.7 μV	1.4 μV	2.8 μV
0x007F	50 Hz	0.142 μV	0.142 μV	0.144 μV	0.145 μV	0.170 μV	0.305 μV	0.380 μV	0.7 μV	2.3 μV	2.8 μV
0x0007	1 kHz	0.620 μV	0.620 μV	0.625 μV	0.625 μV	0.770 μV	1.310 μV	1.650 μV	2.520 μV	7.600 μV	7.600 μV
0x0000	8 kHz	2.000 μV	2.000 μV	2.000 μV	2.000 μV	2.650 μV	4.960 μV	8.020 μV	15.0 μV	55.0 μV	55.0 μV

[1] The maximum absolute input voltage allowed is −200 mV to +300 mV, relative to ground.

Table 33. Typical Output RMS Noise (Referred to ADC Voltage Attenuator Input) of Voltage Channel ADC

ADCFLT	Data Update Rate	28.8 V ADC Input Range
0xBF1D	4 Hz	65 μV
0x961F	10 Hz	65 μV
0x0007	1 kHz	180 μV
0x0000	8 kHz	1600 μV

Table 34. Typical Output RMS Noise of Temperature Channel ADC

ADCFLT	Data Update Rate	0 V to 1.2 V ADC Input Range
0xBF1D	4 Hz	2.8 μV
0x961F	10 Hz	2.8 μV
0x0007	1 kHz	7.5 μV
0x0000	8 kHz	55 μV

Table 40. ADC Conversion Rates and Settling Times

Chop Enabled	Averaging Factor	Running Average	f_{ADC}	$t_{SETTLING}$[1]
No	No	No	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{3}{f_{ADC}}$
No	No	Yes	$\frac{512{,}000}{[SF+1]\times 64}$	$\frac{4}{f_{ADC}}$
No	Yes	No	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{1}{f_{ADC}}$
No	Yes	Yes	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]}$	$\frac{2}{f_{ADC}}$
Yes	N/A	N/A	$\frac{512{,}000}{[SF+1]\times 64\times[3+AF]+3}$	$\frac{2}{f_{ADC}}$

[1] An additional time of approximately 60 µs per ADC is required before the first ADC is available.

Table 41. Allowable Combinations of SF and AF

	AF Range		
SF	**0**	**1 to 7**	**8 to 63**
0 to 31	Yes	Yes	Yes
32 to 63	Yes	Yes	No
64 to 127	Yes	No	No

ADC COMPARATOR AND ACCUMULATOR

The incorporation of comparator logic on the I-ADC allows the I-ADC result to generate an interrupt after a predefined number of conversions has elapsed or a programmable threshold value has been exceeded.

Every I-ADC result can be compared with a preset threshold level (ADC0TH) that is set via ADCCFG[4:3]. In this case, an MCU interrupt is generated if the absolute (sign independent) value of the ADC result is greater than the preprogrammed comparator threshold level. Alternatively, as an extended function of the comparator, user code can configure a threshold counter (ADC0THV) to monitor the number of I-ADC results that have occurred above or below the preset threshold level. In this case, an ADC interrupt is generated when the threshold counter reaches a preset value that is set via ADC0TCL.

By also incorporating a 32-bit accumulator (ADC0ACC) function that can be configured via ADCCFG[6:5], the I-ADC can add or subtract multiple I-ADC sample results. User code can read the accumulated value directly (ADC0ACC) without any further software processing.

ADC SINC3 DIGITAL FILTER RESPONSE

The overall frequency response on all ADuC7036 ADCs is dominated by the low-pass filter response of the on-chip Sinc3 digital filters. The Sinc3 filters are used to decimate the ADC Σ-Δ modulator output data bit stream to generate a valid 16-bit data result. The digital filter response is identical for all ADCs and is configured via the 16-bit ADC filter register (ADCFLT). This register determines the overall throughput rate of the ADCs. The noise resolution of the ADCs is determined by the programmed ADC throughput rate. In the case of the current channel ADC, the noise resolution is determined by throughput rate and selected gain.

The overall frequency response and the ADC throughput is dominated by the configuration of the Sinc3 filter decimation factor (SF) bits (ADCFLT[6:0]) and the averaging factor (AF) bits (ADCFLT[13:8]). Due to limitations on the digital filter internal data path, there are some limitations on the allowable combinations of SF and AF that can be used to generate a required ADC output rate. This restriction limits the minimum ADC update to 4 Hz in normal power mode and to 1 Hz in low power mode. The calculation of the ADC throughput rate is detailed in the ADCFLT bit designations table (see Table 39), and the restrictions on allowable combinations of AF and SF values are outlined in Table 41.

By default, setting ADCFLT = 0x0007 configures the ADCs for a throughput of 1 kHz with all other filtering options (chop, running average, averaging factor, and Sinc3 modify) disabled. A typical filter response based on this default configuration is shown in Figure 22.

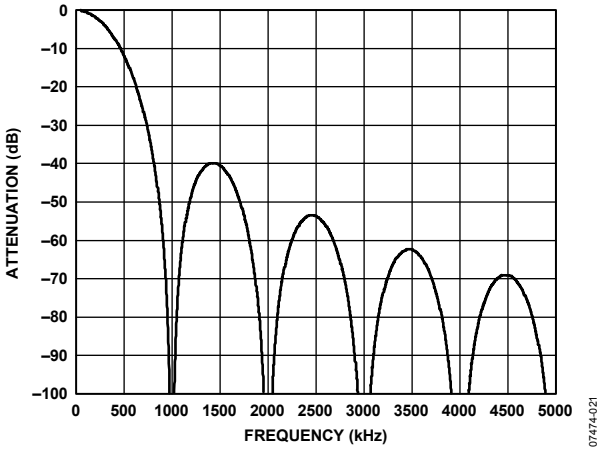

Figure 22. Typical Digital Filter Response at f_{ADC} = 1 kHz (ADCFLT = 0x0007)

In addition, a Sinc3 modify bit (ADCFLT[7]) is available in the ADCFLT register. This bit is set by user code and modifies the standard Sinc3 frequency response to increase the filter stop-band rejection by approximately 5 dB. This is achieved by inserting a second notch at the location determined by

$$f_{NOTCH2} = 1.333 \times f_{NOTCH}$$

where f_{NOTCH} is the location of the first notch in the response.

There is a slight increase in ADC noise if the Sinc3 modify bit is active. Figure 23 shows the modified 1 kHz filter response when the Sinc3 modify bit is active. The new notch is clearly visible at 1.33 kHz, as is the improvement in stop-band rejection when compared with the standard 1 kHz response.

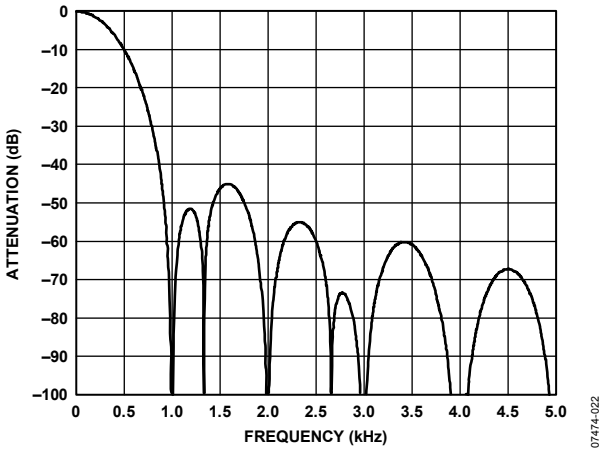

Figure 23. Modified Sinc3 Digital Filter Response at f_{ADC} = 1 kHz (ADCFLT = 0x0087)

The operating mode, clocking mode, and programmable clock divider are controlled using two MMRs, PLLCON and POWCON, and the status of the PLL is indicated by PLLSTA. PLLCON controls the operating mode of the clock system, and POWCON controls both the core clock frequency and the power-down mode. PLLSTA indicates the presence of an oscillator on the XTAL1 pin and provides information about the PLL lock status and the PLL interrupt.

Before powering down the ADuC7036, it is recommended that the clock source for the PLL be switched to the low power 131 kHz oscillator to reduce wake-up time. The low power oscillator is always active.

When the ADuC7036 wakes up from power-down, the MCU core begins executing code as soon as the PLL starts oscillating. This code execution occurs before the PLL has locked to a frequency of 20.48 MHz. To ensure that the Flash/EE memory controller is executing with a valid clock, the controller is driven with a PLL output divide-by-8 clock source while the PLL is locking. When the PLL locks, the PLL output is switched from the PLL output divide-by-8 to the locked PLL output.

If user code requires an accurate PLL output, user code must poll the PLL lock status bit (PLLSTA[1]) after a wake-up before resuming normal code execution.

The PLL is locked within 2 ms if the PLL is clocked from an active clock source, such as a low power 131 kHz oscillator, after waking up.

PLLCON is a protected MMR with two 32-bit keys: PLLKEY0 (prewrite key) and PLLKEY1 (postwrite key). They key values are as follows:

PLLKEY0 = 0x000000AA

PLLKEY1 = 0x00000055

POWCON is a protected MMR with two 32-bit keys: POWKEY0 (prewrite key) and POWKEY1 (postwrite key).

POWKEY0 = 0x00000001

POWKEY1 = 0x000000F4

An example of writing to both MMRs is as follows:

```
POWKEY0       =      0x01   //POWCON key
POWCON        =      0x00   //Full power-down
POWKEY1       =      0xF4   //POWCON KEY
iA1*iA2                     //Dummy cycle to
clear the pipeline, where iA1 and iA2 are
defined as longs and are not 0
PLLKEY0       =      0xAA   //PLLCON key
PLLCON        =      0x0    //Switch to Low
Power Osc.
PLLKEY1       =      0x55   //PLLCON key
iA1*iA2                     //Dummy cycle to
prevent Flash/EE access during clock change
```

SYSTEM CLOCK REGISTERS

PLLSTA Register

Name: PLLSTA

Address: 0xFFFF0400

Default Value: N/A

Access: Read only

Function: This 8-bit register allows user code to monitor the lock state of the PLL and the status of the external crystal.

Table 44. PLLSTA MMR Bit Designations

Bit	Description
7 to 3	Reserved.
2	XTAL clock. This read only bit is a live representation of the current logic level on XTAL1. It indicates if an external clock source is present by alternating between high and low at a frequency of 32.768 kHz.
1	PLL lock status bit. This is a read only bit. Set when the PLL is locked and outputting 20.48 MHz. Cleared when the PLL is not locked and outputting an f_{CORE} divide-by-8 clock source.
0	PLL interrupt. Set if the PLL lock status bit signal goes low. Cleared by writing 1 to this bit.

Timer0 Control Register

Name: T0CON

Address: 0xFFFF030C

Default Value: 0x00000000

Access: Read/write

Function: This 32-bit MMR configures the mode of operation for Timer0.

Table 53. T0CON MMR Bit Designations

Bit	Description
31 to 18	Reserved.
17	Event select bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16 to 12	Event select range (0 to 17). The events are as defined in Table 52.
11	Reserved.
10 to 9	Clock select. 00 = core clock (default). 01 = low power 32.768 kHz oscillator. 10 = external 32.768 kHz watch crystal. 11 = precision 32.768 kHz oscillator.
8	Count up. Available in 16-bit mode only. Set by user for Timer0 to count up. Cleared by user for Timer0 to count down (default).
7	Timer0 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 (default).
6	Timer0 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5	Reserved.
4	Timer0 mode of operation. 0 = 16-bit operation (default). 1 = 48-bit operation.
3 to 0	Prescaler. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. 1111 = source clock/32,768.

TIMER2—WAKE-UP TIMER

Timer2 is a 32-bit wake-up up/down counter timer, with a programmable prescaler. The prescaler is clocked directly from one of four clock sources: namely, the core clock (which is the default selection), the low power 32.768 kHz oscillator, the external 32.768 kHz watch crystal, or the precision 32.768 kHz oscillator. The selected clock source can be scaled by a factor of 1, 16, 256, or 32,768. The wake-up timer continues to run when the core clock is disabled. When the core is operating at 20.48 MHz and at CD = 0 with a prescaler of 1, a minimum resolution of 48.83 ns results.

The counter can be formatted as a plain 32-bit value or as time expressed as hours:minutes:seconds:hundredths.

Timer2 reloads the value from T2LD when Timer2 overflows.

The Timer2 interface consists of four MMRS: T2LD, T2VAL, T2CLRI, and T2CON. T2LD and T2VAL are 32-bit registers and hold 32-bit unsigned integers. T2VAL is a read only register. T2CLRI is an 8-bit register. Writing any value to this register clears the Timer2 interrupt. T2CON is a configuration MMR and is described in Table 55.

Timer2 Load Register

Name: T2LD

Address: 0xFFFF0340

Default Value: 0x00000000

Access: Read/write

Function: This 32-bit register holds the 32-bit value that is loaded into the counter.

Timer2 Clear Register

Name: T2CLRI

Address: 0xFFFF034C

Access: Write only

Function: This 8-bit, write only MMR is written (with any value) by user code to clear the interrupt.

Timer2 Value Register

Name: T2VAL

Address: 0xFFFF0344

Default Value: 0xFFFFFFFF

Access: Read only

Function: This 32-bit register holds the current value of Timer2.

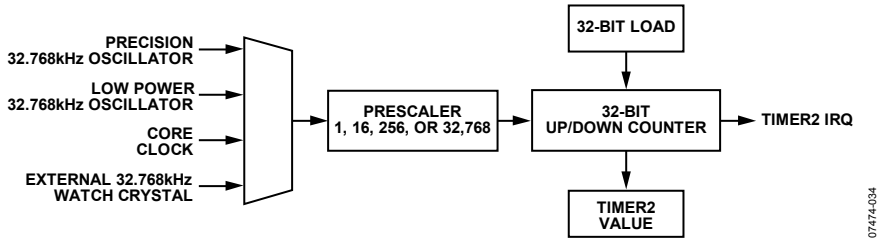

Figure 37. Timer2 Block Diagram

Table 57. T4CON MMR Bit Designations

Bit	Description
31 to 18	Reserved.
17	Event select bit. Set by user to enable time capture of an event. Cleared by user to disable time capture of an event.
16 to 12	Event select range (0 to 17). The events are described in Table 52.
11 to 10	Reserved.
9	Clock select. 0 = core clock (default). 1 = low power 32.768 kHz oscillator.
8	Count up. Set by user for Timer4 to count up. Cleared by user for Timer4 to count down (default).
7	Timer4 enable bit. Set by user to enable Timer0. Cleared by user to disable Timer0 (default).
6	Timer4 mode. Set by user to operate in periodic mode. Cleared by user to operate in free running mode (default).
5 to 4	Reserved.
3 to 0	Prescaler. 0000 = source clock/1 (default). 0100 = source clock/16. 1000 = source clock/256. 1111 = source clock/32,768.

High Voltage Monitor Register

Name: HVMON

Address: Indirectly addressed via the HVCON high voltage interface

Default Value: 0x00

Access: Read only

Function: This 8-bit, read only register reflects the current status of enabled high voltage related circuits and functions on the ADuC7036. This register is not an MMR and does not appear in the MMR memory map. It is accessed via the HVCON register interface, and data is read back from this register via HVDAT.

Table 76. HVMON Bit Designations

Bit	Description
7	WU pin diagnostic readback. When enabled via HVCFG1[4], this read only bit reflects the state of the external WU pin.
6	Overtemperature. 0 = a thermal shutdown event has not occurred. 1 = a thermal shutdown event has occurred.
5	STI pin diagnostic readback. When enabled via HVCFG1[4], this read only bit reflects the state of the external STI pin.
4	Buffer enabled. 0 = the voltage channel ADC input buffer is disabled. 1 = the voltage channel ADC input buffer is enabled.
3	Low voltage flag status bit. Valid only if enabled via HVCFG0[2]. 0 (at power-on) = REG_DVDD has dropped below 2.1 V. In this state, RAM contents can be deemed corrupt. 1 (at power-on) = REG_DVDD has not dropped below 2.1 V. In this state, RAM contents can be deemed valid. It is only cleared by reenabling the low voltage flag in HVCFG0[2].
2	LIN/BSD short-circuit status flag. 0 = the LIN/BSD driver is operating normally. 1 = the LIN/BSD driver has experienced a short-circuit condition and is cleared automatically by writing to HVCFG1[3].
1	STI short-circuit status flag. 0 = the STI driver is operating normally. 1 = the STI driver has experienced a short-circuit condition and is cleared automatically by writing to HVCFG1[3].
0	Wake-up short-circuit status flag. 0 = the wake-up driver is operating normally. 1 = the wake-up driver has experienced a short-circuit condition.

SERIAL TEST INTERFACE

The ADuC7036 incorporates single-pin, serial test interface (STI) ports that can be used for end-customer evaluation or diagnostics on finished production units.

The STI port transmits from one byte to six bytes of data in 12-bit packets. As shown in Figure 44, each transmission packet includes a start bit, the transmitted byte (eight bits), an even parity bit, and two stop bits. The STI data is transmitted on the STI pin, and the baud rate is determined by the overflow rate of Timer4.

The STI port is configured and controlled via six MMRs.

- STIKEY0: Serial Test Interface Key0
- STIKEY1: Serial Test Interface Key1
- STIDAT0: Data0 (16-bit) holds two bytes
- STIDAT1: Data1 (16-bit) holds two bytes
- STIDAT2: Data2 (16-bit) holds two bytes
- STICON: controls the serial test interface

Serial Test Interface Key0 Register

Name: STIKEY0

Address: 0xFFFF0880

Access: Write only

Function: The STIKEY0 MMR is used in conjunction with the STIKEY1 MMR to protect the STICON MMR. STIKEY0 must be written with 0x0007 immediately before any attempt to write to STICON. STIKEY1 must be written with 0x00B9 immediately after STICON is written to ensure the STICON write sequence completes successfully. If STIKEY0 is not written, is written out of sequence, or is written incorrectly, any subsequent write to the STICON MMR is ignored.

Serial Test Interface Key1 Register

Name: STIKEY1

Address: 0xFFFF0888

Access: Write only

Function: The STIKEY1 MMR is used in conjunction with the STIKEY0 MMR to protect the STICON MMR. STIKEY1 must be written with 0x00B9 immediately after any attempt to write to STICON. STIKEY0 must be written with 0x0007 immediately before STICON is written to ensure the STICON write sequence complets successfully. If STIKEY1 is not written, is written out of sequence, or is written incorrectly, any previous write to the STICON MMR is ignored.

Serial Test Interface Data0 Register

Name: STIDAT0

Address: 0xFFFF088C

Default Value: 0x0000

Access: Read/write

Function: The STIDAT0 MMR is a 16-bit register that holds the first and second data bytes that are to be transmitted on the STI pin as soon as the STI port is enabled. The first byte to be transmitted occupies Bits[0:7], and the second byte occupies Bits[8:15].

Serial Test Interface Data1 Register

Name: STIDAT1

Address: 0xFFFF0890

Default Value: 0x0000

Access: Read/write

Function: The STIDAT1 MMR is a 16-bit register that holds the third and fourth data bytes that are to be transmitted on the STI pin when the STI port is enabled. The third byte to be transmitted occupies Bits[0:7], and the fourth byte occupies Bits[8:15].

Serial Test Interface Data2 Register

Name: STIDAT2

Address: 0xFFFF0894

Default Value: 0x0000

Access: Read/write

Function: The STIDAT2 MMR is a 16-bit register that is used to hold the fifth and sixth data bytes that are to be transmitted on the STI pin when the STI port is enabled. The fifth byte to be transmitted occupies Bits[0:7], and the sixth byte occupies Bits[8:15].

Figure 44. Serial ADC Test Interface Example, 3-Byte Transmission

LIN Hardware Synchronization Timer0 Register

Name: LHSVAL0

Address: 0xFFFF0788

Default Value: 0x0000

Access: Read only

Function: This 16-bit, read only register holds the value of the internal LIN synchronization timer. The LIN synchronization timer is clocked from an internal 5 MHz clock and is independent of core clock and baud rate frequency. In LIN mode, the value read by user code from the LHSVAL0 register can be used to calculate the master LIN baud rate. This calculation is then used to configure the internal UART baud rate to ensure correct LIN communication via the UART from the ADuC7036 slave to the LIN master node.

LIN Hardware Synchronization Break Timer1 Register

Name: LHSVAL1

Address: 0xFFFF0790

Default Value: 0x0000

Access: Read/write

Function: When user code reads this location, the 12-bit value returned is the value of the internal LIN break timer, which is clocked directly from the on-chip low power 131 kHz oscillator and times the LIN break pulse. A negative edge on the LIN bus or user code reading the LHSVAL1 results in the timer and the register contents being reset to 0.

When user code writes to this location, the 12-bit value is written not to the LIN break timer but to a LIN break compare register. In LIN mode of operation, the value in the compare register is continuously compared to the break timer value. A LIN break interrupt (IRQEN[7] and LHSSTA[0]) is generated when the timer value reaches the compare value. After the break condition interrupt, the LIN break timer continues to count until the rising edge of the break signal. If a rising edge is not detected and the 12-bit timer overflows (4096 × 1/131 kHz = 31 ms), a break field error interrupt (IRQEN[7] and LHSSTA[4]) is generated. By default, the value in the compare register is 0x0047, corresponding to 11 bit periods (that is, the minimum pulse width for a LIN break pulse at 20 kbps). For different baud rates, this value can be changed by writing to LHSVAL1. Note that if a valid break interrupt is not received, subsequent sync pulse timing through the LHSVAL0 register does not occur.

LIN HARDWARE INTERFACE

LIN Frame Protocol

The LIN frame protocol is broken into four main categories: break symbol, sync byte, protected identifier, and data bytes.

The format of the frame header, break symbol, synchronization byte, and protected identifier is shown in Figure 47. Essentially, the embedded UART, the LIN hardware synchronization logic, and the high voltage transceiver interface all combine on chip to support and manage LIN-based transmissions and receptions.

LIN Frame Break Symbol

As shown in Figure 48, the LIN break symbol, which lasts at least 13 bit periods, is used to signal the start of a new frame. The slave must be able to detect a break symbol even while expecting or receiving data. The ADuC7036 accomplishes this by using the LHSVAL1 break condition and break error detect functionality as described in the LIN Hardware Synchronization Break Timer1 Register section. The break period does not have to be accurately measured, but if a bus fault condition (bus held low) occurs, it must be flagged.

LIN Frame Synchronization Byte

The baud rate of the communication using LIN is calculated from the sync byte, as shown in Figure 49. The time between the first falling edge of the sync field and the fifth falling edge of the sync field is measured and then divided by 8 to determine the baud rate of the data that is to be transmitted. The ADuC7036 implements the timing of this sync byte in hardware. For more information about this feature, see the LIN Hardware Synchronization Status Register section.

LIN Frame Protected Identifier

After receiving the LIN sync field, the required baud rate for the UART is calculated. The UART is then configured, allowing the ADuC7036 to receive the protected identifier, as shown in Figure 50. The protected identifier consists of two subfields: the identifier and the identifier parity. The 6-bit identifier contains the identifier of the target for the frame. The identifier signifies the number of data bytes to be either received or transmitted. The number of bytes is user configurable at the system-level design. The parity is calculated on the identifier and is dependent on the revision of LIN for which the system is designed.

LIN Frame Data Byte

The data byte frame carries between one and eight bytes of data. The number of bytes contained in the frame is dependent on the LIN master. The data byte frame is split into data bytes, as shown in Figure 51.

BIT SERIAL DEVICE (BSD) INTERFACE

BSD is a pulse-width-modulated signal with three possible states: sync, 0, and 1. These are detailed, along with their associated tolerances, in Table 95. The frame length is 19 bits, and communication occurs at 1200 bps ± 3%.

Table 95. BSD Bit Level Description

Parameter	Min	Typ	Max	Unit
TxD Rate	1164	1200	1236	bps
Bit Encoding				
t_{SYNC}	1/16	2/16	3/16	t_{PERIOD}
t_0	5/16	6/16	8/16	t_{PERIOD}
t_1	10/16	12/16	14/16	t_{PERIOD}

BSD COMMUNICATION HARDWARE INTERFACE

The ADuC7036 emulates the BSD communication protocol using a GPIO, an IRQ, and the LIN synchronization hardware, all of which are under software control.

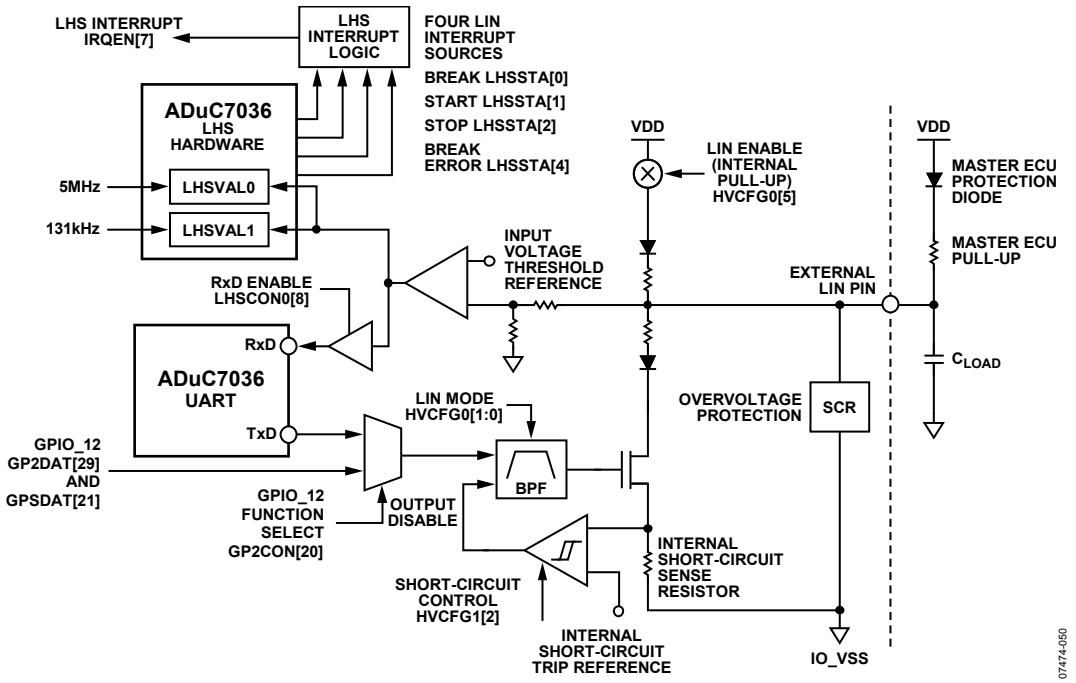

Figure 53. BSD I/O Hardware Interface

PART IDENTIFICATION

Two registers mapped into the MMR space are intended to allow user code to identify and trace manufacturing lot ID information, part ID number, silicon mask revision, and kernel revision. This information is contained in the SYSSER0 and SYSSER1 MMR (see Table 98 and Table 99 for more information).

In addition, the FEE0ADR MMR contains information at power-up that can identify the ADuC7036 family member.

For direct traceability, the assembly lot ID, which can be 64 bits long, is also available. The SYSALI MMR contains the 32-bit lower half of the assembly lot ID, and the upper half is contained in the T1LD MMR at power-up.

The information contained in SYSSER0, SYSSER1, SYSALI, and T1LD allows full traceability of each part.

The lot number is part of the branding on the package as shown in Table 97.

Table 97. Branding Example

Line	LFCSP
Line 1	ADuC7036
Line 2	BCPZ
Line 3	A40 # date code
Line 4	Assembly lot number

System Serial ID Register 0

Name: SYSSER0

Address: 0xFFFF0238

Default Value: 0x00000000 (updated by kernel at power-on)

Access: Read/write

Function: At power-on, this 32-bit register holds the value of the original manufacturing lot number from which this specific ADuC7036 unit was manufactured (bottom die only). Used in conjunction with SYSSER1, this lot number allows the full manufacturing history of this part to be traced (bottom die only).

Table 98. SYSSER0 MMR Bit Designations

Bit	Description
31 to 27	Wafer number. The five bits read from this location give the wafer number (1 to 24) from the wafer fabrication lot ID (from which this device originated). When used in conjunction with SYSSER0[26:0], it provides individual wafer traceability.
26 to 22	Wafer lot fabrication plant. The five bits read from this location reflect the manufacturing plant associated with this wafer lot. When this information is used in conjunction with SYSSER0[21:0], it provides wafer lot traceability.
21 to 16	Wafer lot fabrication ID. The six bits read from this location form part of the wafer lot fabrication ID and, when used in conjunction with SYSSER0[26:22] and SYSSER0[15:0], provide wafer lot traceability.
15 to 0	Wafer lot fabrication ID. These 16 LSBs hold a 16-bit number to be interpreted as the wafer fabrication lot ID number. When used in conjunction with the value in SYSSER1, that is, the manufacturing lot ID, this number is a unique identifier for the part.

SCHEMATIC

This example schematic represents a basic functional circuit implementation. Additional components need to be added to ensure that the system meets any EMC and other overvoltage/overcurrent compliance requirements.

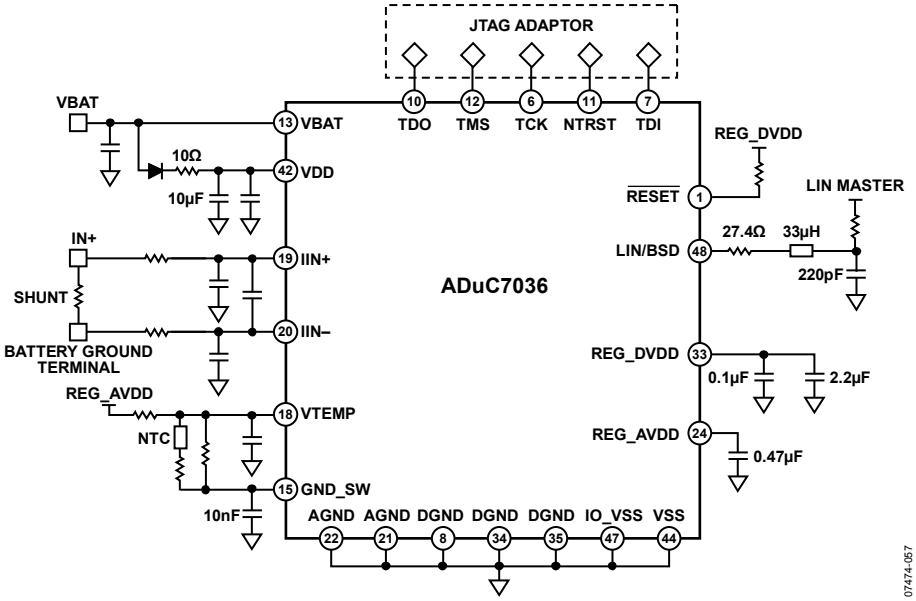

Figure 60. Simplified Schematic