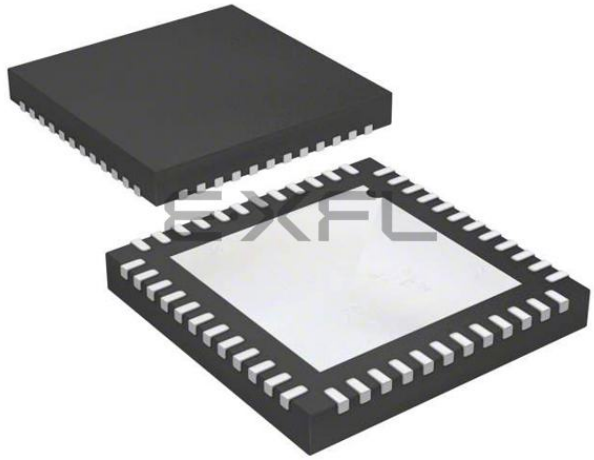

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Core Processor	ARM7®
Core Size	16/32-Bit
Speed	20.48MHz
Connectivity	LINbus, SPI, UART/USART
Peripherals	PSM, Temp Sensor, WDT
Number of I/O	9
Program Memory Size	96KB (48K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 32
Voltage - Supply (Vcc/Vdd)	3.5V ~ 18V
Data Converters	A/D 2x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 115°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	48-LFCSP-VQ (7x7)
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Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

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Table 5. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge		0.5 t_{SL}		ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{HCLK}		ns
t_{DAV}	Data output valid after SCLK edge[1, 2]			(3 × t_{UCLK}) + (2 × t_{HCLK})	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge[1, 2]	4 × t_{UCLK}			ns
t_{DF}	Data output fall time		3.5		ns
t_{DR}	Data output rise time		3.5		ns
t_{SR}	SCLK rise time		3.5		ns
t_{SF}	SCLK fall time		3.5		ns
t_{DOCS}	Data output valid after $\overline{SS}$ edge[2]			(3 × t_{UCLK}) + (2 × t_{HCLK})	ns
t_{SFS}	$\overline{SS}$ high after SCLK edge		0.5 t_{SL}		ns

[1] t_{HCLK} depends on the clock divider (CD) bits in the POWCON MMR. $t_{HCLK} = t_{UCLK}/2^{CD}$.
[2] t_{UCLK} = 48.8 ns. It corresponds to the 20.48 MHz internal clock from the PLL before the clock divider.

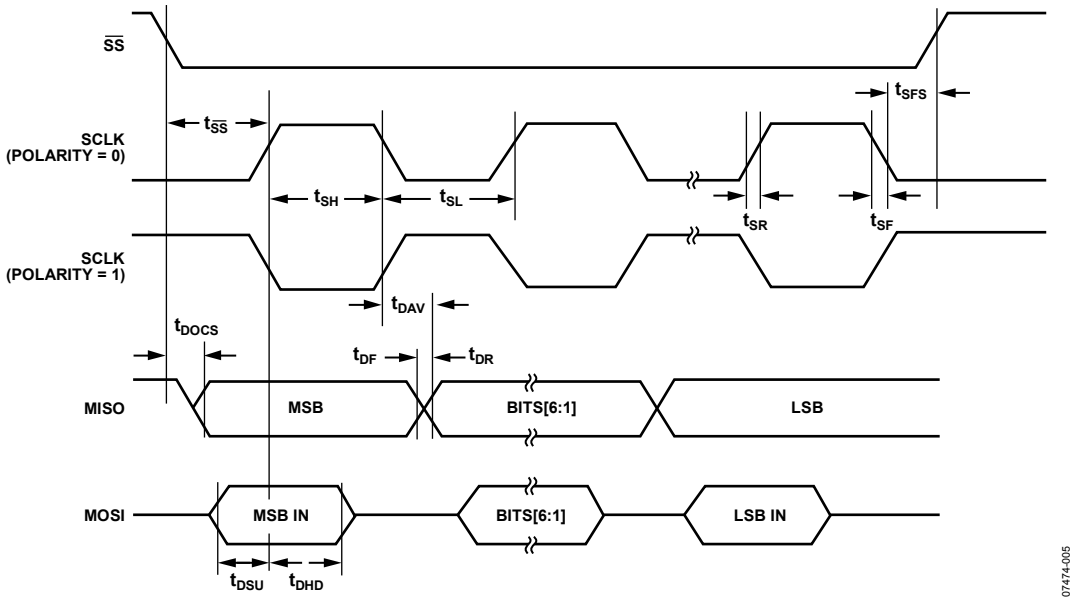

Figure 5. SPI Slave Mode Timing—Phase Mode = 0

LIN Timing Specifications

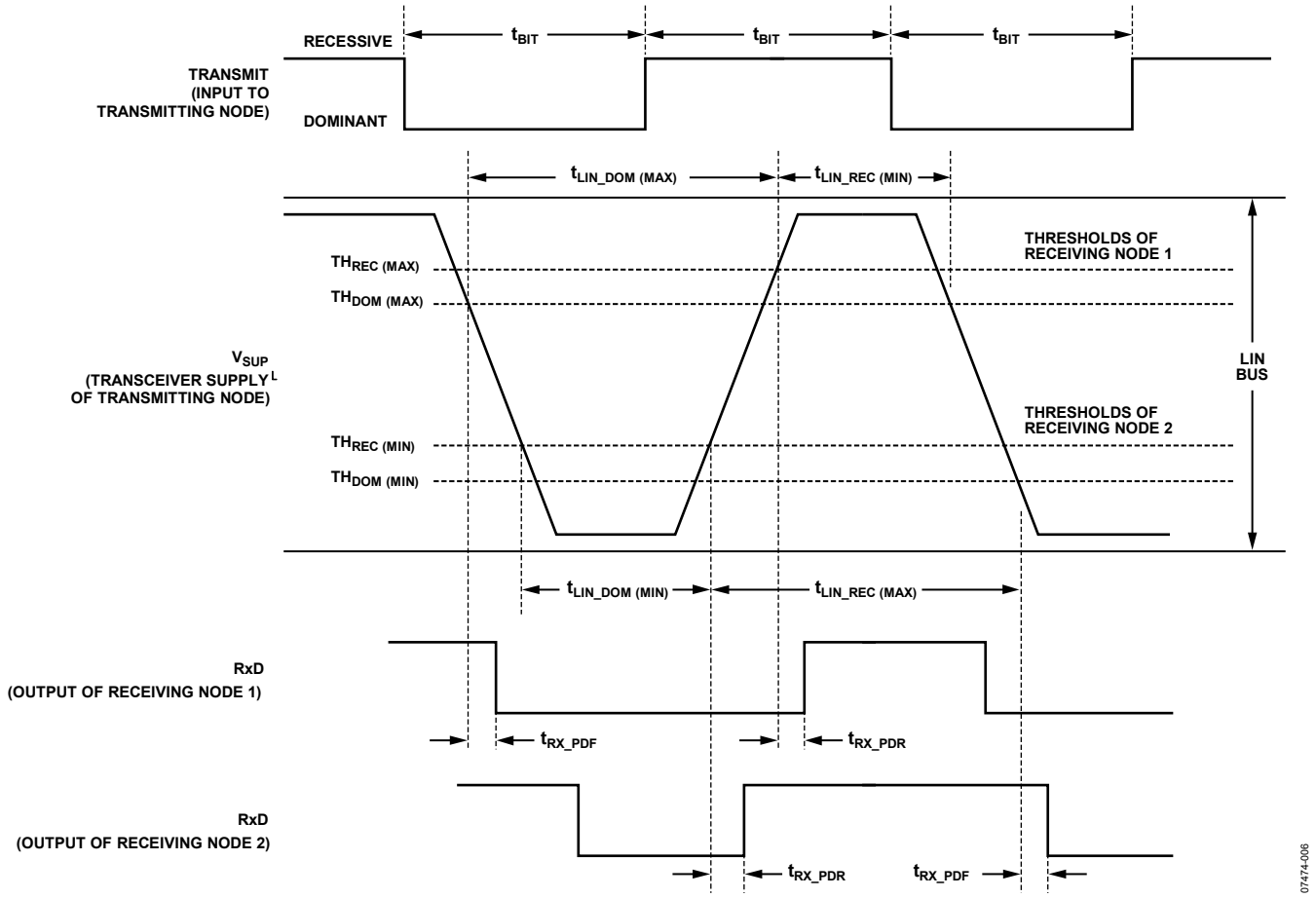

Figure 6. LIN 2.0 Timing Specification

FLASH/EE MEMORY

The ADuC7036 incorporates Flash/EE memory technology on chip to provide the user with nonvolatile, in-circuit reprogrammable memory space.

Like EEPROM, flash memory can be programmed in-system at a byte level, although it must first be erased, with the erasure performed in page blocks. Therefore, flash memory is often and more correctly referred to as Flash/EE memory.

Overall, Flash/EE memory represents a step closer to the ideal memory device that includes nonvolatility, in-circuit programmability, high density, and low cost. Incorporated within the ADuC7036, Flash/EE memory technology allows the user to update program code space in-circuit without the need to replace one-time programmable (OTP) devices at remote operating nodes.

The Flash/EE memory is located at Address 0x80000. Upon a hard reset, the Flash/EE memory maps to Address 0x00000000. The factory-set default contents of all Flash/EE memory locations is 0xFF. Flash/EE can be read in 8-, 16-, and 32-bit segments and written in 16-bit segments. The Flash/EE is rated for 10,000 endurance cycles. This rating is based on the number of times that each byte is cycled, that is, erased and programmed. Implementing a redundancy scheme in the software ensures that none of the flash locations reach 10,000 endurance cycles.

The user can also write data variables to the Flash/EE memory during run-time code execution, for example, for storing diagnostic battery parameter data.

The entire Flash/EE is available to the user as code and nonvolatile data memory. There is no distinction between data and program space during ARM code processing. The real width of the Flash/EE memory is 16 bits, meaning that in ARM mode (32-bit instruction), two accesses to the Flash/EE are necessary for each instruction fetch. When operating at speeds of less than 20.48 MHz, the Flash/EE memory controller can transparently fetch the second 16-bit halfword (part of the 32-bit ARM operation code) within a single core clock period. Therefore, for speeds less than 20.48 MHz (that is, CD > 0), it is recommended to use ARM mode. For 20.48 MHz operation (that is, CD = 0), it is recommended to operate in Thumb mode.

The page size of this Flash/EE memory is 512 bytes. Typically, it takes the Flash/EE controller 20 ms to erase a page, regardless of CD. Writing a 16-bit word at CD = 0, 1, 2, or 3 requires 50 µs; at CD = 4 or 5, 70 µs; at CD = 6, 80 µs; and at CD = 7, 105 µs.

It is possible to write to a single 16-bit location only twice between erasures; that is, it is possible to walk bytes, not bits. If a location is written to more than twice, the contents of the Flash/EE page may become corrupt.

PROGRAMMING FLASH/EE MEMORY IN-CIRCUIT

The Flash/EE memory can be programmed in-circuit, using a serial download mode via the LIN interface or the integrated JTAG port.

Serial Downloading (In-Circuit Programming)

The ADuC7036 facilitates code download via the LIN/BSD pin.

JTAG Access

The ADuC7036 features an on-chip JTAG debug port to facilitate code downloading and debugging.

ADuC7036 Flash/EE Memory

The total 96 kB of Flash/EE is organized as 47,000 × 16 bits. Of this total, 94 kB is designated as user space, and 2 kB is reserved for boot loader/kernel space.

FLASH/EE CONTROL INTERFACE

The access to and control of the Flash/EE memory on the ADuC7036 are managed by an on-chip memory controller. The controller manages the Flash/EE memory as two separate blocks (Block 0 and Block 1).

Block 0 consists of the 32 kB of Flash/EE memory that is mapped from Address 0x00090000 to Address 0x00097FFF, including the 2 kB kernel space that is reserved at the top of this block.

Block 1 consists of the 64 kB of Flash/EE memory that is mapped from Address 0x00080000 to Address 0x0008FFFF.

It should be noted that the MCU core can continue to execute code from one memory block while an active erase or program cycle is being carried out on the other block. If a command operates on the same block as the code currently executing, the core is halted until the command is complete. This also applies to code execution.

User code, LIN, and JTAG programming use the Flash/EE control interface, consisting of the following MMRs:

- FEExSTA (x = 0 or 1): Read only register. Reflects the status of the Flash/EE control interface.
- FEExMOD (x = 0 or 1): Sets the operating mode of the Flash/EE control interface.
- FEExCON (x = 0 or 1): 8-bit command register. The commands are interpreted as described in Table 13.
- FEExDAT (x = 0 or 1): 16-bit data register.
- FEExADR (x = 0 or 1): 16-bit address register.
- FEExSIG (x = 0 or 1): Holds the 24-bit code signature as a result of the signature command being initiated.
- FEExHID (x = 0 or 1): Protection MMR. Controls read and write protection of the Flash/EE memory code space. If previously configured via the FEExPRO register, FEExHID may require a software key to enable access.
- FEExPRO (x= 0 or 1): A buffer of the FEExHID register. Stores the FEExHID value and is automatically downloaded to the FEExHID registers on subsequent reset and power-on events.

Note that user software must ensure that the Flash/EE controller completes any erase or write cycle before the PLL is powered down. If the PLL is powered down before an erase or write cycle is completed, the Flash/EE page or byte may be corrupted.

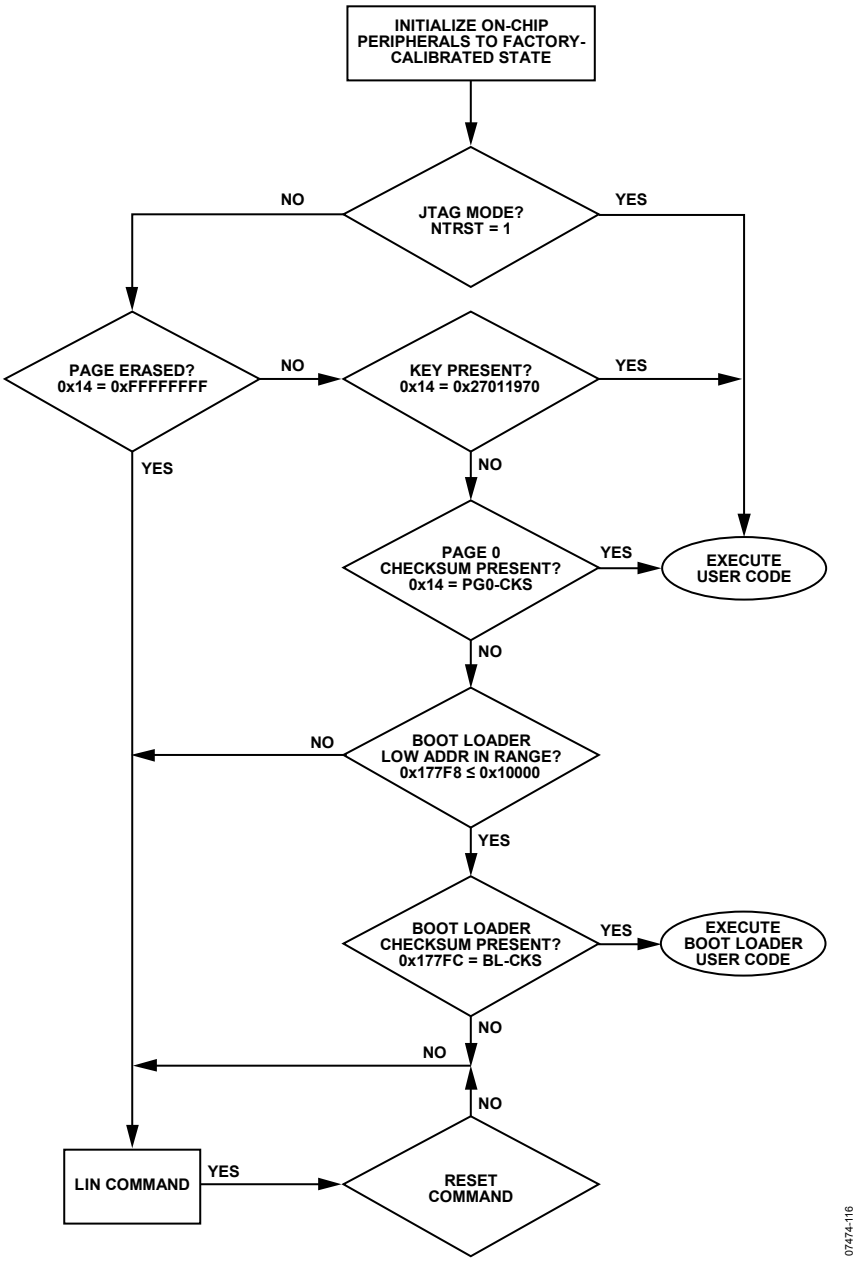

Figure 16. ADuC7036DCPZ Kernel Flowchart

COMPLETE MMR LISTING

In Table 19 to Table 30, addresses are listed in hexadecimal code. Access types include R for read, W for write, and RW for read and write.

Table 19. IRQ Address Base = 0xFFFF0000

Address	Name	Byte	Access Type	Default Value	Description
0x0000	IRQSTA	4	R	0x00000000	Active IRQ source. See the Interrupt System section and Table 50.
0x0004	IRQSIG[1]	4	R	N/A	Current state of all IRQ sources (enabled and disabled). See the Interrupt System section and Table 50.
0x0008	IRQEN	4	RW	0x00000000	Enabled IRQ sources. See the Interrupt System section and Table 50.
0x000C	IRQCLR	4	W	N/A	MMR to disable IRQ sources. See the Interrupt System section and Table 50.
0x0010	SWICFG	4	W	N/A	Software interrupt configuration MMR. See the Programmed Interrupts section and Table 51.
0x0100	FIQSTA	4	R	0x00000000	Active IRQ source. See the Interrupt System section and Table 50.
0x0104	FIQSIG[1]	4	R	N/A	Current state of all IRQ sources (enabled and disabled). See the Interrupt System section and Table 50.
0x0108	FIQEN	4	RW	0x00000000	Enabled IRQ sources. See the Interrupt System section and Table 50.
0x010C	FIQCLR	4	W	N/A	MMR to disable IRQ sources. See the Interrupt System section and Table 50.

[1] Depends on the level on the external interrupt pins (GPIO_0, GPIO_5, GPIO_7, and GPIO_8).

Table 20. System Control Address Base = 0xFFFF0200

Address	Name	Byte	Access Type	Default Value	Description
0x0220	SYSMAP0	1	RW	N/A	Remap control register. See the Remap Operation section and Table 10.
0x0230	RSTSTA	1	RW	Varies; depends on type of reset	Reset status MMR. See the Reset section and Table 11 and Table 12.
0x0234	RSTCLR	1	W	N/A	RSTSTA clear MMR. See the Reset section and Table 11 and Table 12.
0x0238	SYSSER0[1]	4	RW	N/A	System Serial Number 0. See the Part Identification section and Table 98 for details.
0x023C	SYSSER1[1]	4	RW	N/A	System Serial Number 1. See the Part Identification section and Table 99 for details.
0x0560	SYSALI[1]	4	R	N/A	System assembly lot ID. See the Part Identification section for details.
0x0240	SYSCHK[1]	4	RW	N/A	Kernel checksum. See the System Kernel Checksum section.

[1] Updated by kernel.

Table 21. Timer Address Base = 0xFFFF0300

Address	Name	Byte	Access Type	Default Value	Description
0x0300	T0LD	2	RW	0x0000	Timer0 load register. See the Timer0—Lifetime Timer and Timer0 Load Register sections.
0x0304	T0VAL0	2	R	0x0000	Timer0 Value Register 0. See the Timer0—Lifetime Timer and Timer0 Value Registers sections.
0x0308	T0VAL1	4	R	0x00000000	Timer0 Value Register 1. See the Timer0—Lifetime Timer and Timer0 Value Registers sections.
0x030C	T0CON	4	RW	0x00000000	Timer0 control MMR. See the Timer0—Lifetime Timer and Timer0 Control Register sections.
0x0310	T0CLRI	1	W	N/A	Timer0 interrupt clear register. See the Timer0—Lifetime Timer and Timer0 Load Register sections.
0x0314	T0CAP	2	R	0x0000	Timer0 capture register. See the Timer0—Lifetime Timer and Timer0 Capture Register sections.
0x0320	T1LD	4	RW	0x00000000	Timer1 load register. See the Timer1 and Timer1 Load Register sections.
0x0324	T1VAL	4	R	0xFFFFFFFF	Timer1 value register. See the Timer1 and Timer1 Value Register sections.
0x0328	T1CON	4	RW	0x01000000	Timer1 control MMR. See the Timer1 and Timer1 Control Register sections.
0x032C	T1CLRI	1	W	N/A	Timer1 interrupt clear register. See the Timer1 and Timer1 Clear Register sections.
0x0330	T1CAP	4	R	0x00000000	Timer1 capture register. See the Timer1 and Timer1 Capture Register sections.

Table 27. STI Base Address = 0xFFFF0880

Address	Name	Byte	Access Type	Default Value	Description
0x0880	STIKEY0	4	W	N/A	STICON prewrite key. See the Serial Test Interface Key0 Register section.
0x0884	STICON	2	RW	0x0000	Serial test interface control MMR. See the Serial Test Interface Control Register section and Table 91.
0x0888	STIKEY1	4	W	N/A	STICON postwrite key. See the Serial Test Interface Key1 Register section.
0x088C	STIDAT0	2	RW	0x0000	STI Data MMR 0. See the Serial Test Interface Data0 Register section.
0x0890	STIDAT1	2	RW	0x0000	STI Data MMR 1. See the Serial Test Interface Data1 Register section.
0x0894	STIDAT2	2	RW	0x0000	STI Data MMR 2. See the Serial Test Interface Data2 Register section.

Table 28. SPI Base Address = 0xFFFF0A00

Address	Name	Byte	Access Type	Default Value	Description
0x0A00	SPISTA	1	R	0x00	SPI status MMR. See the SPI Status Register section and Table 90.
0x0A04	SPIRX	1	R	0x00	SPI receive MMR. See the SPI Receive Register section.
0x0A08	SPITX	1	W	N/A	SPI transmit MMR. See the SPI Transmit Register section.
0x0A0C	SPIDIV	1	RW	0x1B	SPI baud rate select MMR. See the SPI Divider Register section.
0x0A10	SPICON	2	RW	0x0000	SPI control MMR. See the SPI Control Register section and Table 89.

Table 29. GPIO Base Address = 0xFFFF0D00

Address	Name	Byte	Access Type	Default Value	Description
0x0D00	GP0CON	4	RW	0x11100000	GPIO Port0 control MMR. See the GPIO Port0 Control Register section and Table 59.
0x0D04	GP1CON	4	RW	0x10000000	GPIO Port1 control MMR. See the GPIO Port1 Control Register section and Table 60.
0x0D08	GP2CON	4	RW	0x01000000	GPIO Port2 control MMR. See the GPIO Port2 Control Register section and Table 61.
0x0D20	GP0DAT[1]	4	RW	0x000000XX	GPIO Port0 data control MMR. See the GPIO Port0 Data Register section and Table 62.
0x0D24	GP0SET	4	W	N/A	GPIO Port0 data set MMR. See the GPIO Port0 Set Register section and Table 65.
0x0D28	GP0CLR	4	W	N/A	GPIO Port0 data clear MMR. See the GPIO Port0 Clear Register section and Table 68.
0x0D30	GP1DAT[1]	4	RW	0x000000XX	GPIO Port1 data control MMR. See the GPIO Port1 Data Register section and Table 63.
0x0D34	GP1SET	4	W	N/A	GPIO Port1 data set MMR. See the GPIO Port1 Set Register section and Table 66.
0x0D38	GP1CLR	4	W	N/A	GPIO Port1 data clear MMR. See the GPIO Port1 Clear Register section and Table 69.
0x0D40	GP2DAT[1]	4	RW	0x000000XX	GPIO Port2 data control MMR. See the GPIO Port2 Data Register section and Table 64.
0x0D44	GP2SET	4	W	N/A	GPIO Port2 data set MMR. See the GPIO Port2 Set Register section and Table 67.
0x0D48	GP2CLR	4	W	N/A	GPIO Port2 data clear MMR. See the GPIO Port2 Clear Register section and Table 70.

[1] Depends on the level on the external GPIO pins.

ADC GROUND SWITCH

The ADuC7036 features an integrated ground switch pin, GND_SW (Pin 15). This switch allows the user to dynamically disconnect ground from external devices and, instead, use either a direct connection to ground or a connection to ground using a 20 kΩ resistor. This additional resistor can be used to reduce the number of external components required for an NTC circuit. The ground switch feature can be used for reducing power consumption on application-specific boards.

An example application is shown in Figure 20.

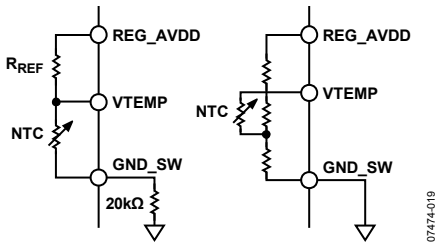

Figure 20. Example External Temperature Sensor Circuits

Figure 20 shows an external NTC used in two modes, with one using the internal 20 kΩ resistor and the second showing a direct connection to ground via GND_SW.

ADCCFG[7] controls the connection of the ground switch to ground, and ADCMDE[6] controls GND_SW resistance, as shown in Figure 21.

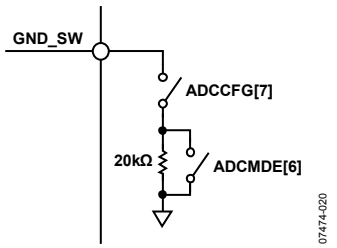

Figure 21. Internal Ground Switch Configuration

The possible combinations of ADCCFG[7] and ADCMDE[6] are shown in Table 31.

Table 31. GND_SW Configuration

ADCCFG[7]	ADCMDE[6]	GND_SW
0	0	Floating
0	1	Floating
1	0	Direct connection to ground
1	1	Connected to ground via 20 kΩ resistor

ADC NOISE PERFORMANCE TABLES

Table 32, Table 33, and Table 34 list the output rms noise in microvolts for some typical output update rates on the I-ADC and V-/T-ADC. The numbers are typical and are generated at a differential input voltage of 0 V. The output rms noise is specified as the standard deviation (or 1 Σ) of the distribution of ADC output codes collected when the ADC input voltage is at a dc voltage. It is expressed in microvolts rms (μV rms).

Table 32. Typical Output RMS Noise of Current Channel ADC in Normal Power Mode

		ADC Input Range									
ADCFLT	Data Update Rate	±2.3 mV (512)	±4.6 mV (256)	±4.68 mV (128)	±18.75 mV (64)	±37.5 mV (32)	±75 mV (16)	±150 mV (8)	±300 mV (4[1])	±600 mV (2[1])	±1.2 V (1[1])
0xBF1D	4 Hz	0.040 μV	0.040 μV	0.043 μV	0.045 μV	0.087 μV	0.175 μV	0.35 μV	0.7 μV	1.4 μV	2.8 μV
0x961F	10 Hz	0.060 μV	0.060 μV	0.060 μV	0.065 μV	0.087 μV	0.175 μV	0.35 μV	0.7 μV	1.4 μV	2.8 μV
0x007F	50 Hz	0.142 μV	0.142 μV	0.144 μV	0.145 μV	0.170 μV	0.305 μV	0.380 μV	0.7 μV	2.3 μV	2.8 μV
0x0007	1 kHz	0.620 μV	0.620 μV	0.625 μV	0.625 μV	0.770 μV	1.310 μV	1.650 μV	2.520 μV	7.600 μV	7.600 μV
0x0000	8 kHz	2.000 μV	2.000 μV	2.000 μV	2.000 μV	2.650 μV	4.960 μV	8.020 μV	15.0 μV	55.0 μV	55.0 μV

[1] The maximum absolute input voltage allowed is −200 mV to +300 mV, relative to ground.

Table 33. Typical Output RMS Noise (Referred to ADC Voltage Attenuator Input) of Voltage Channel ADC

ADCFLT	Data Update Rate	28.8 V ADC Input Range
0xBF1D	4 Hz	65 μV
0x961F	10 Hz	65 μV
0x0007	1 kHz	180 μV
0x0000	8 kHz	1600 μV

Table 34. Typical Output RMS Noise of Temperature Channel ADC

ADCFLT	Data Update Rate	0 V to 1.2 V ADC Input Range
0xBF1D	4 Hz	2.8 μV
0x961F	10 Hz	2.8 μV
0x0007	1 kHz	7.5 μV
0x0000	8 kHz	55 μV

ADC MMR INTERFACE

The ADC is controlled and configured using several MMRs that are described in detail in the ADC Status Register section to the Low Power Voltage Reference Scaling Factor section.

All bits defined in the top eight MSBs (Bits[8:15]) of the ADCSTA MMR are used as flags only and do not generate interrupts. All bits defined in the lower eight LSBs (Bits[0:7]) of this MMR are logic OR'ed to produce a single ADC interrupt to the MCU core. In response to an ADC interrupt, user code should interrogate the ADCSTA MMR to determine the source of the interrupt. Each ADC interrupt source can be individually masked via the ADCMSKI MMR described in the ADC Interrupt Mask Register section.

All ADC result ready bits are cleared by a read of the ADC0DAT MMR. If the current channel ADC is not enabled, all ADC result ready bits are cleared by a read of the ADC1DAT or ADC2DAT MMRs. To ensure that I-ADC and V-/T-ADC conversion data are synchronous, user code should first read the ADC1DAT MMR and then the ADC0DAT MMR. New ADC conversion results are not written to the ADCxDAT MMRs unless the respective ADC result ready bits are first cleared. The only exception to this rule is the data conversion result updates when the ARM core is powered down. In this mode, ADCxDAT registers always contain the most recent ADC conversion result, even though the ready bits have not been cleared.

ADC Status Register

Name: ADCSTA

Address: 0xFFFF0500

Default Value: 0x0000

Access: Read only

Function: This read only register holds general status information related to the mode of operation or current status of the ADCs.

Table 35. ADCSTA MMR Bit Designations

Bit	Description
15	ADC calibration status. Set automatically in hardware to indicate that an ADC calibration cycle has been completed. Cleared after ADCMDE is written to.
14	ADC temperature conversion error. Set automatically in hardware to indicate that a temperature conversion overrange or underrange has occurred. The conversion result is clamped to negative full scale (underrange error) or positive full scale (overrange error) in this case. Cleared when a valid (in-range) temperature conversion result is written to the ADC2DAT register.
13	ADC voltage conversion error. Set automatically in hardware to indicate that a voltage conversion overrange or underrange has occurred. The conversion result is clamped to negative full scale (underrange error) or positive full scale (overrange error) in this case. Cleared when a valid (in-range) voltage conversion result is written to the ADC1DAT register.
12	ADC current conversion error. Set automatically in hardware to indicate that a current conversion overrange or underrange has occurred. The conversion result is clamped to negative full scale (underrange error) or positive full scale (overrange error) in this case. Cleared when a valid (in-range) current conversion result is written to the ADC0DAT register.
11 to 5	Not used. These bits are reserved for future functionality and should not be monitored by user code.
4	Current channel ADC comparator threshold. Valid only if the current channel ADC comparator is enabled via the ADCCFG MMR. Set by hardware if the absolute value of the I-ADC conversion result exceeds the value written in the ADC0TH MMR. However, if the ADC threshold counter is used (ADC0TCL), this bit is set only when the specified number of I-ADC conversions equals the value in the ADC0THV MMR. Cleared automatically by hardware when reconfiguring the ADC or if the comparator is disabled.
3	Current channel ADC overrange bit. Set by hardware if the overrange detect function is enabled via the ADCCFG MMR and the I-ADC input is grossly (>30% approximate) over range. This bit is updated every 125 µs. Cleared by software only when ADCCFG[2] is cleared to disable the function, or the ADC gain is changed via the ADC0CON MMR.
2	Temperature conversion result ready bit. Set by hardware, if the temperature channel ADC is enabled, as soon as a valid temperature conversion result is written in the temperature data register (ADC2DAT MMR). It is also set at the end of a calibration. Cleared by reading either ADC2DAT or ADC0DAT.
1	Voltage conversion result ready bit. Set by hardware, if the voltage channel ADC is enabled, as soon as a valid voltage conversion result is written in the voltage data register (ADC1DAT MMR). It is also set at the end of a calibration. Cleared by reading either ADC1DAT or ADC0DAT.
0	Current conversion result ready bit. Set by hardware, if the current channel ADC is enabled, as soon as a valid current conversion result is written in the current data register (ADC0DAT MMR). It is also set at the end of a calibration. Cleared by reading ADC0DAT.

ADC Filter Register

Name: ADCFLT

Address: 0xFFFF0518

Default Value: 0x0007

Access: Read/write

Function: This 16-bit register controls the speed and resolution of the on-chip ADCs.

Note that if ADCFLT is modified, the current and voltage/temperature ADCs are reset.

Table 39. ADCFLT MMR Bit Designations

Bit	Description
15	Chop enable. Set by the user to enable system chopping of all active ADCs. When this bit is set, the ADC has very low offset errors and drift, but the ADC output rate is reduced by a factor of three if AF = 0 (see Sinc3 decimation factor, Bits[6:0], in this table). If AF > 0, then the ADC output update rate is the same with chop on or off. When chop is enabled, the settling time is two output periods.
14	Running average. Set by the user to enable a running-average-by-two function reducing ADC noise. This function is automatically enabled when chopping is active. It is an optional feature when chopping is inactive, and if enabled (when chopping is inactive), does not reduce the ADC output rate but does increase the settling time by one conversion period. Cleared by the user to disable the running average function.
13 to 8	Averaging factor (AF). The values written to these bits are used to implement a programmable first-order Sinc3 postfilter. The averaging factor can further reduce ADC noise at the expense of output rate, as described in Bits[6:0], Sinc3 decimation factor, in this table.
7	Sinc3 modify. Set by the user to modify the standard Sinc3 frequency response to increase the filter stop-band rejection by approximately 5 dB. This is achieved by inserting a second notch (NOTCH2) a $f_{NOTCH2} = 1.333 \times f_{NOTCH}$, where f_{NOTCH} is the location of the first notch in the response.
6 to 0	Sinc3 decimation factor (SF).[1] The value (SF) written in these bits controls the oversampling (decimation factor) of the Sinc3 filter. The output rate from the Sinc3 filter is given by $f_{ADC} = (512{,}000/([SF + 1] \times 64))$ Hz[2], when the chop bit (Bit 15, chop enable) = 0 and the averaging factor (AF) = 0. This is valid for all SF values ≤ 125. For SF = 126, f_{ADC} is forced to 60 Hz. For SF = 127, f_{ADC} is forced to 50 Hz. For information on calculating the f_{ADC} for SF (other than 126 and 127) and AF values, refer to Table 40.

[1] Due to limitations on the digital filter internal data path, there are some limitations on the combinations of the Sinc3 decimation factor (SF) and averaging factor (AF) that can be used to generate a required ADC output rate. This restriction limits the minimum ADC update in normal power mode to 4 Hz or 1 Hz in lower power mode.
[2] In low power mode and low power plus mode, the ADC is driven directly by the low power oscillator (131 kHz) and not 512 kHz. All f_{ADC} calculations should be divided by 4 (approximately).

Normal Interrupt (IRQ) Request

The IRQ request is the exception signal allowed to enter the processor in IRQ mode. It is used to service general-purpose interrupt handling of internal and external events.

All 32 bits of the IRQSTA MMR are OR'ed to create a single IRQ signal to the ARM7TDMI core. The four 32-bit registers dedicated to IRQ are described in the IRQSTA Register to the IRQCLR Register sections.

IRQSTA Register

Name: IRQSTA

Adress: 0xFFFF0000

Default Value: 0x00000000

Access: Read only

Function: This register provides the status of the IRQ source that is currently enabled by IRQ source status (see Figure 32). When a bit in this register is set to 1, the corresponding source generates an active IRQ request to the ARM7TDMI core. There is no priority encoder or interrupt vector generation. This function is implemented in software in a common interrupt handler routine.

IRQSIG Register

Name: IRQSIG

Address: 0xFFFF0004

Default Value: 0x00000000

Access: Read only

Function: This 32-bit register reflects the status of the different IRQ sources. If a peripheral generates an IRQ signal, the corresponding bit in the IRQSIG is set; otherwise, the corresponding bit is cleared. The IRQSIG bits are cleared when the interrupt in the particular peripheral is cleared. All IRQ sources can be masked in the IRQEN MMR. IRQSIG is read only.

IRQEN Register

Name: IRQEN

Address: 0xFFFF0008

Default Value: 0x00000000

Access: Read/write

Function: This register provides the value of the current enable mask. When a bit in this register is set to 1, the corresponding source request is enabled to create an IRQ exception signal. When a bit is set to 0, the corresponding source request is disabled or masked and does not create an IRQ exception signal. The IRQEN register cannot be used to disable an interrupt.

IRQCLR Register

Name: IRQCLR

Address: 0xFFFF000C

Access: Write only

Function: This register allows the IRQEN register to clear to mask an interrupt source. Each bit set to 1 clears the corresponding bit in the IRQEN register without affecting the remaining bits. When used as a pair of registers, IRQEN and IRQCLR allow independent manipulation of the enable mask without requiring an automatic read-modify-write instruction.

Fast Interrupt Request (FIQ)

The FIQ is the exception signal allowed to enter the processor in FIQ mode. It is provided to service data transfer or communication channel tasks with low latency. The FIQ interface is identical to the IRQ interface and provides the second-level interrupt (highest priority). Four 32-bit registers are dedicated to FIQ: FIQSIG, FIQEN, FIQCLR, and FIQSTA.

All 32 bits of the FIQSTA MMR are OR'ed to create the FIQ signal to the core and to Bit 0 of both the FIQ and IRQ registers (FIQ source).

The logic for FIQEN and FIQCLR does not allow an interrupt source to be enabled in both IRQ and FIQ masks. As a side effect, a bit set to 1 in FIQEN clears the same bit in IRQEN. Likewise, a bit set to 1 in IRQEN clears the same bit in FIQEN. An interrupt source can be disabled in both IRQEN and FIQEN masks.

Programmed Interrupts

Because the programmed interrupts are not maskable, they are controlled by another register, SWICFG, that writes into both IRQSTA and IRQSIG registers and/or the FIQSTA and FIQSIG registers at the same time.

The 32-bit register dedicated to software interrupt is SWICFG; it is described in Table 51. This MMR allows the control of a programmed source interrupt.

Table 51. SWICFG MMR Bit Designations

Bit	Description
31 to 3	Reserved.
2	Programmed interrupt FIQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of FIQSTA and FIQSIG.
1	Programmed interrupt IRQ. Setting/clearing this bit corresponds to setting/clearing Bit 1 of IRQSTA and IRQSIG.
0	Reserved.

Note that any interrupt signal must be active for at least the minimum interrupt latency time to be detected by the interrupt controller and by the user in the IRQSTA or FIQSTA register.

GPIO Port0 Control Register

Name: GP0CON

Address: 0xFFFF0D00

Default Value: 0x11100000

Access: Read/write

Function: This 32-bit MMR selects the pin function for each Port0 pin.

Table 59. GP0CON MMR Bit Designations

Bit	Description
31 to 29	Reserved. These bits are reserved and should be written as 0 by user code.
28	Reserved. This bit is reserved and should be written as 1 by user code.
27 to 25	Reserved. These bits are reserved and should be written as 0 by user code.
24	Internal P0.6 enable bit. This bit must be set to 1 by user software to enable the high voltage serial interface before using the HVCON and HVDAT registered high voltage interface.
23 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	Internal P0.5 enable bit. This bit must be set to 1 by user software to enable the high voltage serial interface before using the HVCON and HVDAT registered high voltage interface.
19 to 17	Reserved. These bits are reserved and should be written as 0 by user code.
16	GPIO_4 function select bit. Set to 1 by user code to configure the GPIO_4 pin as ECLK, enabling a 2.56 MHz clock output on this pin. Cleared by user code to 0 to configure the GPIO_4 pin as a general-purpose I/O (GPIO) pin.
15 to 13	Reserved. These bits are reserved and should be written as 0 by user code.
12	GPIO_3 function select bit. Set to 1 by user code to configure the GPIO_3 pin as MOSI, master output, and slave input data for the SPI port. Cleared by user code to 0 to configure the GPIO_3 pin as a general-purpose I/O (GPIO) pin.
11 to 9	Reserved. These bits are reserved and should be written as 0 by user code.
8	GPIO_2 function select bit. Set to 1 by user code to configure the GPIO_2 pin as MISO, master input and slave output data for the SPI port. Cleared by user code to 0 to configure the GPIO_2 pin as a general-purpose I/O (GPIO) pin.
7 to 5	Reserved. These bits are reserved and should be written as 0 by user code.
4	GPIO_1 function select bit. Set to 1 by user code to configure the GPIO_1 pin as SCLK, serial clock I/O for the SPI port. Cleared by user code to 0 to configure the GPIO_1 pin as a general-purpose I/O (GPIO) pin.
3 to 1	Reserved. These bits are reserved and should be written as 0 by user code.
0	GPIO_0 function select bit. Set to 1 by user code to configure the GPIO_0 pin as $\overline{SS}$, serial clock I/O for the SPI port. Cleared by user code to 0 to configure the GPIO_0 pin as a general-purpose I/O (GPIO) pin.

GPIO Port2 Set Register

Name: GP2SET

Address: 0xFFFF0D44

Access: Write only

Function: This 32-bit MMR allows user code to individually bit-address external GPIO pins to set them high only. User code can accomplish this using the GP2SET MMR without having to modify or maintain the status of the GPIO pins (as user code requires when using GP2DAT).

Table 67. GP2SET MMR Bit Designations

Bit	Description
31 to 23	Reserved. These bits are reserved and should be written as 0 by user code.
22	Port 2.6 set bit. Set to 1 by user code to set the external GPIO_13 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_13 pin.
21	Port 2.5 set bit. Set to 1 by user code to set the external GPIO_12 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_12 pin.
20 to 18	Reserved. These bits are reserved and should be written as 0 by user code.
17	Port 2.1 set bit. Set to 1 by user code to set the external GPIO_8 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_8 pin.
16	Port 2.0 set bit. Set to 1 by user code to set the external GPIO_7 pin high. Clearing this bit to 0 via user software has no effect on the external GPIO_7 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

GPIO Port0 Clear Register

Name: GP0CLR

Address: 0xFFFF0D28

Access: Write only

Function: This 32-bit MMR allows user code to individually bit-address external GPIO pins to clear them low only. User code can accomplish this using the GP0CLR MMR without having to modify or maintain the status of the GPIO pins (as user code requires when using GP0DAT).

Table 68. GP0CLR MMR Bit Designations

Bit	Description
31 to 21	Reserved. These bits are reserved and should be written as 0 by user code.
20	Port 0.4 clear bit. Set to 1 by user code to clear the external GPIO_4 pin low. Clearing this bit to 0 via user software has no effect on the external GPIO_4 pin.
19	Port 0.3 clear bit. Set to 1 by user code to clear the external GPIO_3 pin low. Clearing this bit to 0 via user software has no effect on the external GPIO_3 pin.
18	Port 0.2 clear bit. Set to 1 by user code to clear the external GPIO_2 pin low. Clearing this bit to 0 via user software has no effect on the external GPIO_2 pin.
17	Port 0.1 clear bit. Set to 1 by user code to clear the external GPIO_1 pin low. Clearing this bit to 0 via user software has no effect on the external GPIO_1 pin.
16	Port 0.0 clear bit. Set to 1 by user code to clear the external GPIO_0 pin low. Clearing this bit to 0 via user software has no effect on the external GPIO_0 pin.
15 to 0	Reserved. These bits are reserved and should be written as 0 by user code.

High Voltage Data Register

Name: HVDAT

Address: 0xFFFF080C

Default Value: Updated by kernel

Access: Read/write

Function: This 12-bit register holds data to be written indirectly to, and read indirectly from, the following high voltage interface registers.

Table 73. HVDAT MMR Bit Designations

Bit	Description
11 to 8	Command with which High Voltage Data HVDAT[7:0] is associated. These bits are read only and should be written as 0s. 0x00 = read back High Voltage Register HVCFG0 into HVDAT. 0x01 = read back High Voltage Register HVCFG1 into HVDAT. 0x02 = read back High Voltage Status Register HVSTA into HVDAT. 0x03 = read back High Voltage Status Register HVMON into HVDAT. 0x08 = write the value in HVDAT to the High Voltage Register HVCFG0. 0x09 = write the value in HVDAT to the High Voltage Register HVCFG1.
7 to 0	High voltage data to read/write.

High Voltage Configuration1 Register

Name: HVCFG1

Address: Indirectly addressed via the HVCON high voltage interface

Default Value: 0x00

Access: Read/write

Function: This 8-bit register controls the function of high voltage circuits on the ADuC7036. This register is not an MMR and does not appear in the MMR memory map. It is accessed via the HVCON register interface. Data to be written to this register is loaded through HVDAT, and data is read back from this register using HVDAT.

Table 75. HVCFG1 Bit Designations

Bit	Description
7	Voltage attenuator diagnostic enable bit. Set to 1 to turn on a 1.29 µA current source that adds 170 mV differential voltage to the voltage channel measurement. Cleared to 0 to disable the voltage attenuator diagnostic.
6	High voltage temperature monitor. The high voltage temperature monitor is an uncalibrated temperature monitor located on chip, close to the high voltage circuits. This monitor is completely separate to the on-chip, precision temperature sensor (controlled via ADC1CON[7:6]) and allows user code to monitor die temperature change close to the hottest part of the ADuC7036 die. The monitor generates a typical output voltage of 600 mV at 25°C and has a negative temperature coefficient of typically −2.1 mV/°C. Set to 1 to enable the on-chip, high voltage temperature monitor. When enabled, this voltage output temperature monitor is routed directly to the voltage channel ADC. Cleared to 0 to disable the on-chip, high voltage temperature monitor.
5	Voltage channel short enable bit. Set to 1 to enable an internal short (at the attenuator, before the ADC input buffers) on the voltage channel ADC and to allow noise to be measured as a self-diagnostic test. Cleared to 0 to disable an internal short on the voltage channel.
4	WU and STI readback enable bit. Set to 1 to enable input capability on the external WU and STI pins. In this mode, a rising or falling edge transition on the WU and STI pins generates a high voltage interrupt. When this bit is set, the state of the WU and STI pins can be monitored via the HVMON register (HVMON[7] and HVMON[5]). Cleared to 0 to disable input capability on the external WU and STI pins.
3	High voltage I/O driver enable bit. Set to 1 to reenable high voltage I/O pins (LIN/BSD, STI, and WU) that have been disabled as a result of a short-circuit current event (the event must last longer than 20 µs for the LIN/BSD and STI pins and longer than 400 µs for the WU pin). This bit must also be set to 1 to reenable the WU and STI pins if they were disabled by a thermal event. It should be noted that this bit must be set to clear any pending interrupt generated by the short-circuit event (even if the event has passed) as well as reenabling the high voltage I/O pins. Cleared to 0 automatically.
2	Enable/disable short-circuit protection (LIN/BSD and STI). Set to 1 to enable passive short-circuit protection on the LIN pin. In this mode, a short-circuit event on the LIN/BSD pin generates a high voltage interrupt, IRQ3 (if enabled in IRQEN[16]), and asserts the appropriate status bit in HVSTA but does not disable the short-circuiting pin. Cleared to 0 to enable active short-circuit protection on the LIN/BSD pin. In this mode, during a short-circuit event, the LIN/BSD pin generates a high voltage interrupt (IRQ3), asserts HVSTA[16], and automatically disables the short-circuiting pin. When disabled, the I/O pin can only be reenabled by writing to HVCFG1[3].
1	WU pin timeout (monoflop) counter enable/disable. Set to disable the WU I/O timeout counter. Cleared to enable a timeout counter that automatically deasserts the WU pin 1.3 sec after user code has asserted the WU pin via HVCFG0[4].
0	WU open-circuit diagnostic enable. Set to enable an internal WU I/O diagnostic pull-up resistor to the VDD pin, thus allowing detection of an open-circuit condition on the WU pin. Cleared to disable an internal WU I/O diagnostic pull-up resistor.

UART Fractional Divider Register

Name: COMDIV2

Address: 0xFFFF072C

Default Value: 0x0000

Access: Read/write

Function: This 16-bit register controls the operation of the fractional divider for the ADuC7036.

Table 86. COMDIV2 MMR Bit Designations

Bit	Name	Description
15	FBEN	Fractional baud rate generator enable bit. Set by the user to enable the fractional baud rate generator. Cleared by the user to generate the baud rate using the standard 450 UART baud rate generator.
14 to 13		Reserved.
12 to 11	FBM[1:0]	Fractional Divider M. If FBM = 0, M = 4. See Equation 2 for the calculation of the baud rate using the M fractional divider and Table 80 for common baud rate values.
10 to 0	FBN[10:0]	Fractional Divider N. See Equation 2 for the calculation of the baud rate using a fractional divider and Table 80 for common baud rate values.

LIN (LOCAL INTERCONNECT NETWORK) INTERFACE

The ADuC7036 features high voltage physical interfaces between the ARM7 MCU core and an external LIN bus. The LIN interface operates as a slave only interface, operating from 1 kBaud to 20 kBaud, and it is compatible with the LIN 2.0 standard. The pull-up resistor required for a slave node is on chip, reducing the need for external circuitry. The LIN protocol is emulated using the on-chip UART, an IRQ, a dedicated LIN timer, and the high voltage transceiver (also incorporated on chip) as shown in Figure 46. The LIN is clocked from the low power oscillator for the break timer, and a 5 MHz output from the PLL is used for the synchronous byte timing.

LIN MMR DESCRIPTION

The LIN hardware synchronization (LHS) functionality is controlled through five MMRs. The function of each MMR is as follows:

- LHSSTA: LHS status register. This MMR contains information flags that describe the current status on the interface.
- LHSCON0: LHS Control Register 0. This MMR controls the configuration of the LHS timer.
- LHSCON1: LHS start and stop edge control register. This MMR dictates on which edge of the LIN synchronization byte the LHS starts/stops counting.
- LHSVAL0: LHS synchronization 16-bit timer. This MMR is controlled by LHSCON0.
- LHSVAL1: LHS break timer register.

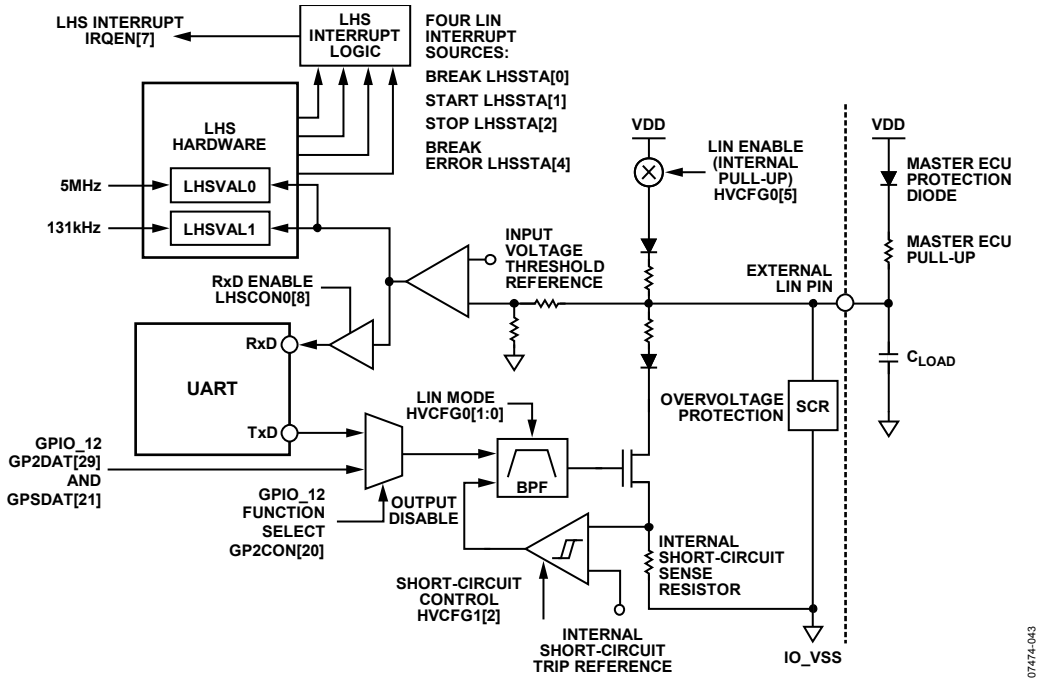

Figure 46. LIN I/O Block Diagram

Bit	Description
5	Enable compare interrupt bit. Set to 1 by user code to generate an LHS interrupt (IRQEN[7]) when the value in LHSVAL0 (the LIN synchronization bit timer) equals the value in the LHSCMP register. The LHS compare interrupt bit, LHSSTA[3], is set when this interrupt occurs. This configuration is used in BSD write mode to allow user code to correctly time the output pulse widths of BSD bits to be transmitted. Cleared to 0 by user code to disable compare interrupts.
4	Enable stop interrupt. Set to 1 by user code to generate an interrupt when a stop condition occurs. Cleared to 0 by user code to disable interrupts when a stop condition occurs.
3	Enable start interrupt. Set to 1 by user code to generate an interrupt when a start condition occurs. Cleared to 0 by user code to disable interrupts when a start condition occurs.
2	LIN sync enable bit. Set to 1 by user code to enable LHS functionality. Cleared to 0 by user code to disable LHS functionality.
1	Edge counter clear bit. Set to 1 by user code to clear the internal edge counters in the LHS peripheral. Cleared automatically to 0 after a 15 µs delay.
0	LHS reset bit. Set to 1 by user code to reset all LHS logic to default conditions. Cleared automatically to 0 after a 15 µs delay.

[1] In BSD mode, LHSCON0[6] is set to 1. Because of the finite propagation delay in the BSD transmit (from the MCU to the external pin) and receive (from the external pin to the MCU) paths, user code must not switch between BSD write and read modes until the MCU confirms that the external BSD pin is deasserted. Failure to adhere to this recommendation may result in the generation of an inadvertent break condition interrupt after user code switches from BSD write mode to BSD read mode. A stop condition interrupt can be used to ensure that this scenario is avoided.

LIN Hardware Synchronization Control Register 1

Name: LHSCON1

Address: 0xFFFF078C

Default Value: 0x00000032

Access: Read/write

Function: This 32-bit LHS control register, in conjunction with the LHSCON0 register, is used to configure the LIN mode of operation.

Table 94. LHSCON1 MMR Bit Designations

Bit	Description
31 to 8	Reserved. These bits are reserved for future use and should be written as 0 by user software.
7 to 4	LIN stop edge count. Set by user code to the number of falling or rising edges on which to stop the internal LIN synchronization counter. The stop value of this counter can be read by user code using LHSVAL0. The type of edge, either rising or falling, is configured by LHSCON0[7]. The default value of these bits is 0x3, which configures the hardware to stop counting on the third falling edge. Note that the first falling edge is considered to be the falling edge at the start of the LIN break pulse.
3 to 0	LIN start edge count. These four bits are set by user code to the number of falling edges that must occur before the internal LIN synchronization timer starts counting. The stop value of this counter can be read by user code using LHSVAL0. The default value of these bits is 0x2, which configures the hardware to start counting on the second falling edge. Note that the first falling edge is considered to be the falling edge at the start of the LIN break pulse.

LIN Diagnostics

The ADuC7036 features the capability to nonintrusively monitor the current state of the LIN/BSD pin. This readback functionality is implemented using GPIO_11. The current state of the LIN/BSD pin is contained in GP2DAT[4].

It is also possible to drive the LIN/BSD pin high and low through user software, allowing the user to detect open-circuit conditions. This functionality is implemented via GPIO_12. To enable this functionality, GPIO_12 must be configured as a GPIO through GP2CON[20]. After it is configured, the LIN/BSD pin can be pulled high or low using GP2DAT.

The ADuC7036 also features short-circuit protection on the LIN/BSD pin. If a short-circuit condition is detected on the LIN/BSD pin, HVSTA[2] is set. This bit is cleared by reenabling the LIN driver using HVCFG1[3]. It is possible to disable this feature through HVCFG1[2].

LIN Operation During Thermal Shutdown

When a thermal event occurs, that is, when HVSTA[3] is set, LIN communications continue uninterrupted.

OUTLINE DIMENSIONS

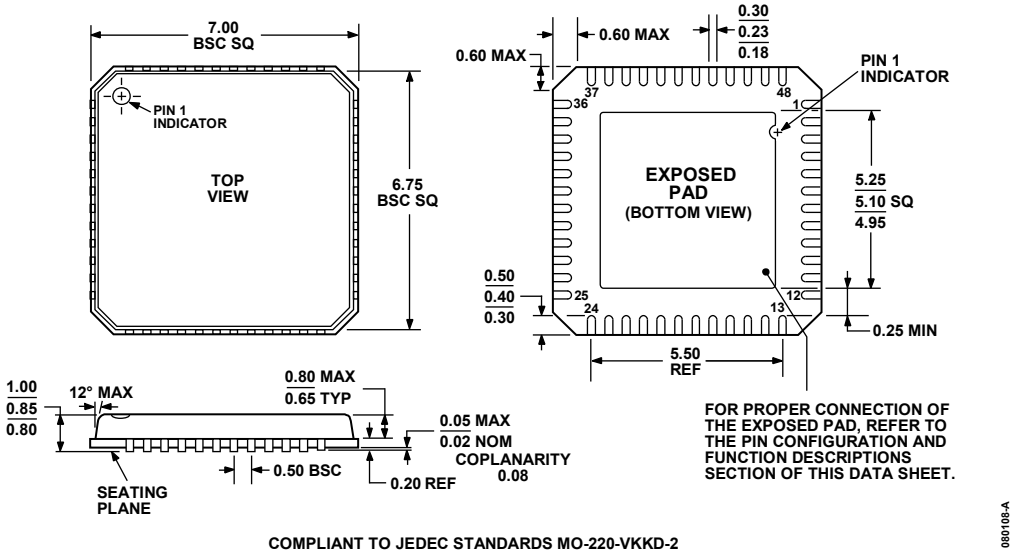

Figure 61. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Model Information	Package Option
ADuC7036BCPZ	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	10 MHz	CP-48-1
ADuC7036BCPZ-RL	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	10 MHz	CP-48-1
ADuC7036CCPZ	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	20 MHz	CP-48-1
ADuC7036CCPZ-RL	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	20 MHz	CP-48-1
ADuC7036DCPZ	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	20 MHz	CP-48-1
ADuC7036DCPZ-RL	−40°C to +115°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	20 MHz	CP-48-1
EVAL-ADuC7036QSPZ		Evaluation Board	10 MHz	

[1] Z = RoHS Compliant Part.

D07474-0-4/10(B)