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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	393216
Number of I/O	660
Number of Gates	1569178
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1156-BBGA
Supplier Device Package	1156-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000e-6fg1156i

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal

implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.

indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

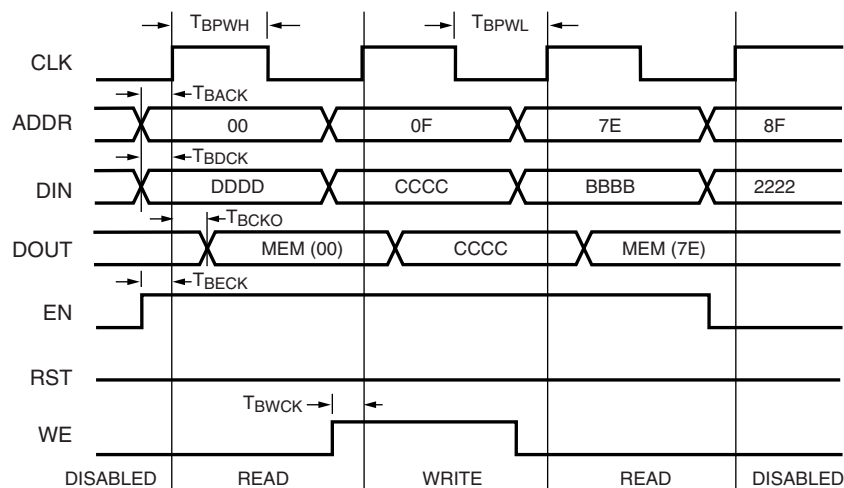
Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS} , (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition,

the contents of the memory are correct, but the read port has invalid data.

At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.



ds022_0343_121399

Figure 33: Timing Diagram for Single Port Block SelectRAM+ Memory

LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in [Figure 54](#). A sample circuit illustrating a valid termination for receiving LVDS signals appears in [Figure 55](#). [Table 38](#) lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on [Table 40](#).

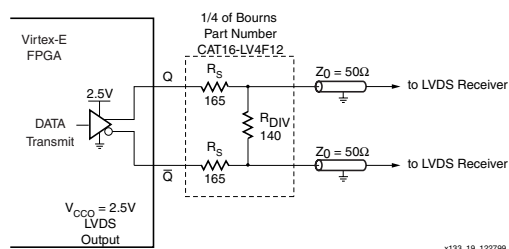


Figure 54: Transmitting LVDS Signal Circuit

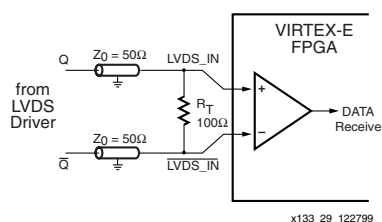


Figure 55: Receiving LVDS Signal Circuit

Table 38: LVDS Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
$V_{ICM}^{(2)}$	0.2	1.25	2.2
$V_{OCM}^{(1)}$	1.125	1.25	1.375
$V_{IDIFF}^{(1)}$	0.1	0.35	-
$V_{ODIFF}^{(1)}$	0.25	0.35	0.45
$V_{OH}^{(1)}$	1.25	-	-
$V_{OL}^{(1)}$	-	-	1.25

Notes:

1. Measured with a 100 Ω resistor across Q and $\bar{Q}$.
2. Measured with a differential input voltage = ± 350 mV.

LVPECL

Depending on whether the device is transmitting or receiving an LVPECL signal, two different circuits are used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in [Figure 56](#). A sample circuit illustrating a valid termination for receiving LVPECL signals appears in [Figure 57](#). [Table 39](#) lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on [Table 40](#).

Table 39: LVPECL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.49	-	2.72
V_{IL}	0.86	-	2.125
V_{OH}	1.8	-	-
V_{OL}	-	-	1.57

Notes:

1. For more detailed information, see [DS022-3: Virtex-E 1.8V FPGA DC and Switching Characteristics](#), Module 3, LVPECL DC Specifications section.

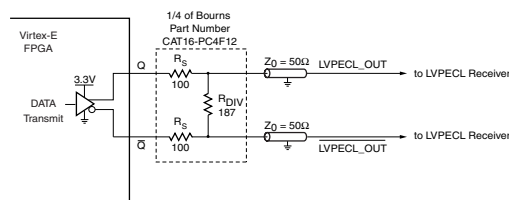


Figure 56: Transmitting LVPECL Signal Circuit

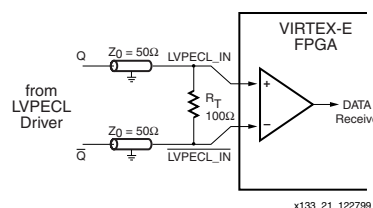


Figure 57: Receiving LVPECL Signal Circuit

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E		200	mA
			XCV100E		200	mA
			XCV200E		300	mA
			XCV300E		300	mA
			XCV400E		300	mA
			XCV600E		400	mA
			XCV1000E		500	mA
			XCV1600E		500	mA
			XCV2000E		500	mA
			XCV2600E		500	mA
			XCV3200E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E		2	mA
			XCV100E		2	mA
			XCV200E		2	mA
			XCV300E		2	mA
			XCV400E		2	mA
			XCV600E		2	mA
			XCV1000E		2	mA
			XCV1600E		2	mA
			XCV2000E		2	mA
			XCV2600E		2	mA
			XCV3200E		2	mA
I_L	Input or output leakage current		All	-10	+10	μ A
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{in} = 0$ V, $V_{CCO} = 3.3$ V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)			Note 2	0.25	mA

Notes:

- With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
- Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Table 2: IOB Input Switching Characteristics (Continued)

			Speed Grade ⁽¹⁾				Units
Description ⁽²⁾	Symbol	Device	Min	-8	-7	-6	
Sequential Delays							
Clock CLK							
Minimum Pulse Width, High	T _{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T _{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T _{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T _{IOPICK} / T _{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	T _{IOPICKD} / T _{IOICKPD}	XCV50E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV100E	1.25 / 0	2.8 / 0	2.9 / 0	2.9 / 0	ns, min
		XCV200E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV300E	1.33 / 0	3.0 / 0	3.1 / 0	3.1 / 0	ns, min
		XCV400E	1.37 / 0	3.1 / 0	3.2 / 0	3.2 / 0	ns, min
		XCV600E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1000E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV1600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2000E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
		XCV2600E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min
XCV3200E	1.53 / 0	3.5 / 0	3.6 / 0	3.6 / 0	ns, min		
ICE input	T _{IOICECK} / T _{IOCKICE}	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	T _{IOSRCKI}	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T _{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T _{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing t_i for LVTTTL is measured at 1.4 V. For other I/O standards, see Table 4.

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO_DLL_L40P
1	5	P89	P87	NA	IO_DLL_L40N
2	1	P210	P209	NA	IO_DLL_L6P
3	0	P213	P215	NA	IO_DLL_L6N
IO LVDS					
Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	✓	-
2	0	P228	P229	✓	VREF
3	0	P223	P224	✓	-
4	0	P220	P221	✓	-
5	0	P217	P218	✓	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	✓	VREF
8	1	P202	P203	✓	-
9	1	P199	P200	✓	-
10	1	P194	P195	✓	VREF
11	1	P191	P192	✓	VREF
12	1	P188	P189	✓	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	✓	CS
15	2	P178	P177	✓	DIN, D0

**Table 9: HQ240 Differential Pin Pair Summary
XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	✓	-
17	2	P171	P170	✓	VREF
18	2	P168	P167	✓	D1
19	2	P163	P162	✓	D2
20	2	P160	P159	✓	-
21	2	P157	P156	✓	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	✓	-
24	3	P145	P144	✓	D4, VREF
25	3	P142	P141	✓	-
26	3	P139	P138	✓	D5
27	3	P134	P133	✓	VREF
28	3	P131	P130	✓	VREF
29	3	P128	P127	✓	-
30	3	P126	P125	1	VREF
31	3	P124	P123	✓	INIT
32	4	P118	P117	✓	-
33	4	P114	P113	✓	-
34	4	P111	P110	✓	VREF
35	4	P108	P107	✓	VREF
36	4	P103	P102	✓	-
37	4	P100	P99	✓	-
38	4	P97	P96	✓	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	✓	-
43	5	P74	P73	✓	VREF
44	5	P71	P70	✓	VREF
45	5	P68	P67	✓	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	✓	-

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	VCCINT	V24
NA	VCCINT	R23
NA	VCCINT	P25
NA	VCCINT	L25
NA	VCCINT	J24
0	VCCO	D19
0	VCCO	B25
0	VCCO	A17
1	VCCO	D13
1	VCCO	D7
1	VCCO	A10
2	VCCO	K1
2	VCCO	H4
2	VCCO	B2
3	VCCO	Y4
3	VCCO	U1
3	VCCO	P4
4	VCCO	AF10
4	VCCO	AE2
4	VCCO	AC8
5	VCCO	AF17
5	VCCO	AC20
5	VCCO	AC14
6	VCCO	AE25
6	VCCO	W23
6	VCCO	U26
7	VCCO	N23
7	VCCO	K26
7	VCCO	G23
NA	GND	A26
NA	GND	A25
NA	GND	A22

Table 10: BG352 — XCV100E, XCV200E, XCV300E

Bank	Pin Description	Pin #
NA	GND	A19
NA	GND	A14
NA	GND	A8
NA	GND	A5
NA	GND	A2
NA	GND	A1
NA	GND	B26
NA	GND	B1
NA	GND	E26
NA	GND	E1
NA	GND	H26
NA	GND	H1
NA	GND	N1
NA	GND	P26
NA	GND	W26
NA	GND	W1
NA	GND	AB26
NA	GND	AB1
NA	GND	AE26
NA	GND	AE1
NA	GND	AF26
NA	GND	AF25
NA	GND	AF22
NA	GND	AF19
NA	GND	AF13
NA	GND	AF8
NA	GND	AF5
NA	GND	AF2
NA	GND	AF1

Notes:

1. No Connect in the XCV100E.
2. V_{REF} or I/O option only in the XCV200E and XCV300E; otherwise, I/O option only.

BG432 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A ✓ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AL16	AH15	NA	IO_DLL_L86P
1	5	AK16	AL17	NA	IO_DLL_L86N
2	1	A16	B16	NA	IO_DLL_L16P
3	0	D17	C17	NA	IO_DLL_L16N
IO LVDS					
Total Outputs: 137, Asynchronous Output Pairs: 63					
0	0	D27	B29	1	-
1	0	C27	B28	✓	-
2	0	A28	D26	✓	VREF
3	0	C26	B27	2	-
4	0	A27	D25	✓	-
5	0	C25	D24	✓	VREF
6	0	D23	B25	1	-
7	0	B24	C24	1	VREF
8	0	A24	D22	✓	VREF
9	0	B22	C22	✓	-
10	0	D20	C21	✓	-
11	0	C20	B21	✓	-
12	0	D19	A20	✓	-
13	0	A19	B19	✓	VREF
14	0	D18	B18	1	-
15	0	B17	C18	1	VREF

Table 13: BG432 Differential Pin Pair Summary
XCV300E, XCV400E, XC600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	1	B16	C17	NA	IO_LVDS_DLL
17	1	B15	A15	1	VREF
18	1	D15	C15	1	-
19	1	A13	B14	✓	VREF
20	1	D14	B13	✓	-
21	1	B12	C13	✓	-
22	1	C12	D13	✓	-
23	1	C11	D12	✓	-
24	1	C10	B10	✓	VREF
25	1	D10	C9	1	VREF
26	1	B8	A8	1	-
27	1	B7	C8	✓	VREF
28	1	A6	D8	✓	-
29	1	D7	B6	2	-
30	1	C6	A5	✓	VREF
31	1	D6	B5	✓	-
32	1	C5	A4	1	-
33	1	D5	B4	✓	CS, WRITE
34	2	D3	C2	✓	DIN, D0, BUSY
35	2	D2	E4	3	-
36	2	D1	E3	4	-
37	2	E2	F4	1	VREF
38	2	E1	F3	5	-
39	2	F2	G4	1	-
40	2	G3	G2	✓	VREF
41	2	H3	H2	4	-
42	2	H1	J4	1	VREF
43	2	J2	K4	✓	D1
44	2	K2	K1	✓	D2
45	2	L2	M4	4	-
46	2	M3	M2	1	-
47	2	N4	N3	1	-

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13 ¹
1	IO	A16 ¹
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24 ¹
1	IO	B15 ¹
1	IO	B17 ¹
1	IO	B23
1	IO_LVDS_DLL_L21P	F14

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19 ²
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D25 ¹
2	IO	D26
2	IO	E26
2	IO	F26
2	IO	H26 ¹
2	IO	K26 ¹
2	IO	M25 ¹
2	IO	N26 ¹
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25

Table 20: FG676 — XCV400E, XCV600E

Bank	Pin Description	Pin #
2	IO_VREF_L54P_Y	G26 ²
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21
2	IO_L58P_YY	H25
2	IO_L58N_YY	K23
2	IO_L59P_Y	L20
2	IO_L59N_Y	J26
2	IO_L60P_Y	K25
2	IO_L60N_Y	L22
2	IO_L61P_Y	L21
2	IO_L61N_Y	L23
2	IO_L62P_Y	M20
2	IO_L62N_Y	L24
2	IO_VREF_L63P_YY	M23
2	IO_D3_L63N_YY	M22
2	IO_L64P_YY	L26
2	IO_L64N_YY	M21
2	IO_L65P_Y	N19
2	IO_L65N_Y	M24
2	IO_VREF_L66P_Y	M26
2	IO_L66N_Y	N20
2	IO_L67P_YY	N24
2	IO_L67N_YY	N21
2	IO_L68P_YY	N23
2	IO_L68N_YY	N22
3	IO	P24
3	IO	P26 ¹
3	IO	R26 ¹
3	IO	T26 ¹
3	IO	U26 ¹
3	IO	W25

FG676 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A $\checkmark$ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	E13	B13	NA	IO_DLL_L21N
2	1	C13	F14	NA	IO_DLL_L21P
1	5	AB13	AF13	NA	IO_DLL_L115N
0	4	AA14	AC14	NA	IO_DLL_L115P
IOLVDS					
Total Pairs: 183, Asynchronous Output Pairs: 97					
0	0	F7	C4	1	-
1	0	C5	G8	$\checkmark$	-
2	0	E7	D6	$\checkmark$	VREF
3	0	F8	A4	NA	-
4	0	D7	B5	NA	-
5	0	G9	E8	$\checkmark$	VREF
6	0	F9	A5	$\checkmark$	-
7	0	C7	D8	1	-
8	0	E9	B7	1	VREF
9	0	D9	A7	NA	-
10	0	G10	B8	NA	VREF
11	0	F10	C9	$\checkmark$	-
12	0	E10	A8	1	-
13	0	D10	G11	$\checkmark$	-
14	0	F11	B10	$\checkmark$	-
15	0	E11	C10	NA	-
16	0	D11	G12	$\checkmark$	-
17	0	F12	C11	$\checkmark$	VREF

Table 21: FG676 Differential Pin Pair Summary
XCV400E, XCV600E

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	0	E12	A11	$\checkmark$	-
19	0	C12	D12	1	-
20	0	H13	A12	1	VREF
21	1	F14	B13	NA	IO_LVDS_DLL
22	1	F13	E14	NA	-
23	1	A14	D14	1	VREF
24	1	H14	C14	1	-
25	1	C15	G14	$\checkmark$	-
26	1	D15	E15	$\checkmark$	VREF
27	1	F15	C16	$\checkmark$	-
28	1	D16	G15	-	-
29	1	A17	E16	$\checkmark$	-
30	1	E17	C17	$\checkmark$	-
31	1	D17	F16	1	-
32	1	C18	F17	$\checkmark$	-
33	1	G16	A18	$\checkmark$	VREF
34	1	G17	C19	$\checkmark$	-
35	1	B19	D18	1	VREF
36	1	E18	D19	1	-
37	1	B20	F18	$\checkmark$	-
38	1	C20	G19	$\checkmark$	VREF
39	1	E19	G18	$\checkmark$	-
40	1	D20	A21	$\checkmark$	-
41	1	C21	F19	$\checkmark$	VREF
42	1	E20	B22	$\checkmark$	-
43	1	D21	A23	2	-
44	1	E21	C22	$\checkmark$	CS
45	2	E23	F22	$\checkmark$	DIN, D0
46	2	E24	F20	$\checkmark$	-
47	2	G21	G22	2	-
48	2	F24	H20	1	VREF
49	2	E25	H21	1	-
50	2	F23	G23	$\checkmark$	-
51	2	H23	J20	$\checkmark$	VREF

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1 ³
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4 ²
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1 ²
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L166P_YY	AV26
5	IO_L166N_YY	AW27
5	IO_L167P_Y	AU26
5	IO_L167N_Y	AV27
5	IO_L168P_Y	AT26
5	IO_L168N_Y	AW28
5	IO_L169P_YY	AU27
5	IO_L169N_YY	AV28
5	IO_L170P_YY	AW29
5	IO_VREF_L170N_YY	AT27
5	IO_L171P_Y	AW30
5	IO_L171N_Y	AU28
5	IO_L172P_Y	AV30
5	IO_L172N_Y	AV29
5	IO_L173P_YY	AW31
5	IO_VREF_L173N_YY	AU29
5	IO_L174P_YY	AV31
5	IO_L174N_YY	AT29
5	IO_L175P_Y	AW32
5	IO_VREF_L175N_Y	AU30 ³
5	IO_L176P_Y	AW33
5	IO_L176N_Y	AT30
5	IO_L177P_YY	AV33
5	IO_VREF_L177N_YY	AU31
5	IO_L178P_YY	AT31
5	IO_L178N_YY	AW34
5	IO_L179P_Y	AV32
5	IO_L179N_Y	AV34
5	IO_L180P_Y	AU32
5	IO_L180N_Y	AW35
5	IO_L181P_YY	AT32
5	IO_VREF_L181N_YY	AV35
5	IO_L182P_YY	AU33
5	IO_L182N_YY	AW36
5	IO_L183P_Y	AT33
5	IO_VREF_L183N_Y	AV36 ¹

Table 22: FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
5	IO_L184P_Y	AU34
5	IO_L184N_Y	AU36
6	IO	W39
6	IO	AR37
6	IO	AR39
6	IO_L185N_YY	AR36
6	IO_L185P_YY	AT38
6	IO_L186N_Y	AR38
6	IO_L186P_Y	AP36
6	IO_VREF_L187N	AT39 ¹
6	IO_L187P	AP37
6	IO_L188N	AP38
6	IO_L188P	AP39
6	IO_VREF_L189N_Y	AN36
6	IO_L189P_Y	AN38
6	IO_L190N_YY	AN37
6	IO_L190P_YY	AN39
6	IO_L191N	AM36
6	IO_L191P	AM38
6	IO_L192N_Y	AM37
6	IO_L192P_Y	AL36
6	IO_VREF_L193N_YY	AM39
6	IO_L193P_YY	AL37
6	IO_L194N_YY	AL38
6	IO_L194P_YY	AK36
6	IO_VREF_L195N	AL39 ³
6	IO_L195P	AK37
6	IO_L196N	AK38
6	IO_L196P	AJ36
6	IO_VREF_L197N_YY	AK39
6	IO_L197P_YY	AJ37
6	IO_L198N_YY	AJ38
6	IO_L198P_YY	AH37
6	IO_L199N	AJ39
6	IO_L199P	AH38

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	6	AP39	AP38	4	-
189	6	AN38	AN36	6	VREF
190	6	AN39	AN37	√	-
191	6	AM38	AM36	4	-
192	6	AL36	AM37	6	-
193	6	AL37	AM39	√	VREF
194	6	AK36	AL38	√	-
195	6	AK37	AL39	7	VREF
196	6	AJ36	AK38	4	-
197	6	AJ37	AK39	√	VREF
198	6	AH37	AJ38	√	-
199	6	AH38	AJ39	4	-
200	6	AG38	AH39	√	VREF
201	6	AG39	AG36	√	-
202	6	AF39	AG37	6	-
203	6	AE38	AF36	4	-
204	6	AF38	AF37	4	-
205	6	AE36	AE39	6	VREF
206	6	AE37	AD38	√	-
207	6	AD36	AD39	4	-
208	6	AC39	AC38	6	-
209	6	AB38	AD37	√	VREF
210	6	AB39	AC35	√	-
211	6	AA38	AC36	7	-
212	6	AA39	AC37	4	-
213	6	Y38	AB35	√	VREF
214	6	Y39	AB36	√	-
215	6	AA36	AB37	4	VREF
216	7	W38	AA37	√	-
217	7	V39	W37	4	VREF
218	7	U39	W36	√	-
219	7	U38	V38	√	VREF
220	7	T39	V37	4	-
221	7	T38	V36	7	-

Table 23: FG680 Differential Pin Pair Summary
XCV600E, XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
222	7	R39	V35	√	-
223	7	U36	U37	√	VREF
224	7	U35	R38	6	-
225	7	T37	P39	4	-
226	7	T36	P38	√	-
227	7	N38	N39	6	VREF
228	7	M39	R37	4	-
229	7	M38	R36	4	-
230	7	L39	P37	6	-
231	7	N37	P36	√	-
232	7	N36	L38	√	VREF
233	7	M37	K39	4	-
234	7	L37	K38	√	-
235	7	L36	J39	√	VREF
236	7	K37	J38	4	-
237	7	K36	H39	√	VREF
238	7	J37	H38	√	-
239	7	G38	G39	√	VREF
240	7	F39	J36	6	-
241	7	F38	H37	4	-
242	7	E39	H36	√	-
243	7	E38	G37	6	VREF
244	7	D39	G36	4	-
245	7	F36	D38	4	VREF
246	7	E37	D37	6	-

Notes:

1. AO in the XCV1000E, 1600E, 2000E.
2. AO in the XCV600E, 1000E, 1600E.
3. AO in the XCV600E, 1000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV600E, 1000E, 2000E.
7. AO in the XCV1000E.
8. AO in the XCV2000E.

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L147N_YY	AW7
4	IO_L148P_Y	AY7
4	IO_L148N_Y	BB8
4	IO_L149P_Y	BA9
4	IO_L149N_Y	AV8
4	IO_L150P_YY	AW8
4	IO_L150N_YY	BA10
4	IO_VREF_L151P_YY	BB10
4	IO_L151N_YY	AY8
4	IO_L152P_Y	AV9
4	IO_L152N_Y	BA11
4	IO_VREF_L153P_Y	BB11 ²
4	IO_L153N_Y	AW9
4	IO_L154P_YY	AY9
4	IO_L154N_YY	BA12
4	IO_VREF_L155P_YY	BB12
4	IO_L155N_YY	AV10
4	IO_L156P_Y	BA13
4	IO_L156N_Y	AW10
4	IO_L157P_Y	BB13
4	IO_L157N_Y	AY10
4	IO_VREF_L158P_YY	AV11
4	IO_L158N_YY	BA14
4	IO_L159P_YY	AW11
4	IO_L159N_YY	BB14
4	IO_L160P_Y	AV12
4	IO_L160N_Y	BA15
4	IO_L161P_Y	AW12
4	IO_L161N_Y	AY15
4	IO_L162P_Y	AW13
4	IO_L162N_Y	BB15
4	IO_L163P_Y	AV14
4	IO_L163N_Y	BA16
4	IO_L164P_YY	AW14
4	IO_L164N_YY	AY16
4	IO_VREF_L165P_YY	BB16
4	IO_L165N_YY	AV15

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
4	IO_L166P_Y	AY17
4	IO_L166N_Y	AW15
4	IO_L167P_Y	BB17
4	IO_L167N_Y	AU16
4	IO_L168P_YY	AV16
4	IO_L168N_YY	AY18
4	IO_VREF_L169P_YY	AW16
4	IO_L169N_YY	BA18
4	IO_L170P_Y	BB19
4	IO_L170N_Y	AW17
4	IO_L171P_Y	AY19
4	IO_L171N_Y	AV18
4	IO_L172P_YY	AW18
4	IO_L172N_YY	BB20
4	IO_VREF_L173P_YY	AY20
4	IO_L173N_YY	AV19
4	IO_L174P_Y	BB21
4	IO_L174N_Y	AW19
4	IO_VREF_L175P_Y	AY21 ¹
4	IO_L175N_Y	AV20
4	IO_LVDS_DLL_L176P	AW20
5	GCK1	AY22
5	IO	AV24
5	IO	AV34
5	IO	AW27
5	IO	AW36
5	IO	AY23
5	IO	AY31
5	IO	AY33
5	IO	BA26
5	IO	BA29
5	IO	BA33
5	IO	BB25
5	IO_LVDS_DLL_L176N	AW21
5	IO_L177P_Y	BB22
5	IO_VREF_L177N_Y	AW22 ¹

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	C42
NA	GND	C41
NA	GND	C40
NA	GND	C3
NA	GND	C2
NA	GND	C1
NA	GND	BB41
NA	GND	BB40
NA	GND	BB4
NA	GND	BB39
NA	GND	BB3
NA	GND	BB2
NA	GND	BA42
NA	GND	BA41
NA	GND	BA40
NA	GND	BA3
NA	GND	BA2
NA	GND	BA1
NA	GND	B42
NA	GND	B41
NA	GND	B40
NA	GND	B3
NA	GND	B2
NA	GND	B1
NA	GND	AY42
NA	GND	AY41
NA	GND	AY40
NA	GND	AY3
NA	GND	AY2
NA	GND	AY1
NA	GND	AW42
NA	GND	AW4
NA	GND	AW39
NA	GND	AW1
NA	GND	AV5
NA	GND	AV38
NA	GND	AV30

Table 24: FG860 — XCV1000E, XCV1600E, XCV2000E

Bank	Pin Description	Pin #
NA	GND	AV22
NA	GND	AV21
NA	GND	AV13
NA	GND	AU6
NA	GND	AU37
NA	GND	AU30
NA	GND	AU22
NA	GND	AU21
NA	GND	AU13
NA	GND	AK6
NA	GND	AK5
NA	GND	AK38
NA	GND	AK37
NA	GND	AB6
NA	GND	AB5
NA	GND	AB38
NA	GND	AB37
NA	GND	AA6
NA	GND	AA5
NA	GND	AA38
NA	GND	AA37
NA	GND	A41
NA	GND	A40
NA	GND	A4
NA	GND	A39
NA	GND	A3
NA	GND	A2

Notes:

1. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_L188N_YY	AJ12 ¹
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L190P	AK12 ⁴
5	IO_L190N	Y13 ⁴
5	IO_L191P	AG11
5	IO_L191N	AF11
5	IO_L192P	AH11
5	IO_L192N	AJ11
5	IO_L193P_YY	AE12 ⁴
5	IO_L193N_YY	AG10 ⁴
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_L195N_YY	AC12
5	IO_L196P_YY	AK10
5	IO_L196N_YY	AD11
5	IO_L197P_YY	AJ9
5	IO_L197N_YY	AE9
5	IO_L198P_YY	AH10
5	IO_VREF_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L208P	AD8 ⁴
5	IO_L208N	AK5 ⁴
5	IO_L209P	AC9
5	IO_VREF_L209N	AJ4 ¹
5	IO_L210P	AG5
5	IO_L210N	AK4
5	IO_L211P_YY	AH5 ³
5	IO_L211N_YY	AG3 ⁴
6	IO	T2 ⁴
6	IO	T10 ⁴
6	IO	U1
6	IO	U4 ⁵
6	IO	U6 ⁴
6	IO	U7 ⁴
6	IO	V1 ⁴
6	IO	V5 ⁵
6	IO	V8
6	IO	Y10 ⁴
6	IO	AA4 ⁴
6	IO	AB5 ⁵
6	IO	AB7 ⁴
6	IO	AC3 ⁵

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
7	IO_L275N_YY	G3
7	IO_L275P_YY	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N	E4
7	IO_VREF_L277P	K9
7	IO_L278N_YY	J8
7	IO_L278P_YY	F4
7	IO_L279N_Y	D1 ³
7	IO_L279P_Y	H7 ⁴
7	IO_L280N_YY	G6
7	IO_VREF_L280P_YY	C2 ¹
7	IO_L281N	D2
7	IO_L281P	F5
7	IO_L282N_YY	D3 ⁴
7	IO_L282P_YY	K10 ³
2	CCLK	F26
3	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19

Table 26: FG900 — XCV600E, XCV1000E, XCV1600E

Bank	Pin Description	Pin #
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U13
NA	VCCINT	U18
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF

Table 29: FG1156 Differential Pin Pair Summary:
XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF