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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	393216
Number of I/O	660
Number of Gates	1569178
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	860-BGA Exposed Pad
Supplier Device Package	860-FBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000e-6fg860i

Virtex-E Ordering Information

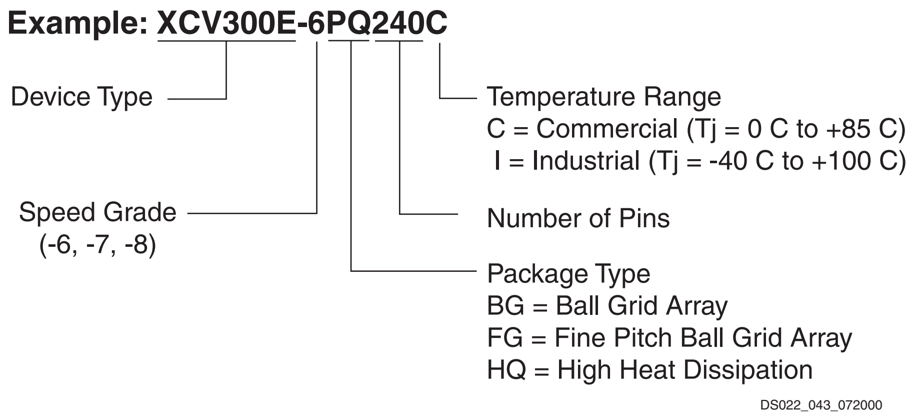

Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple devices.

To guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. For more information about DLL functionality, see the Design Consideration section of the data sheet.

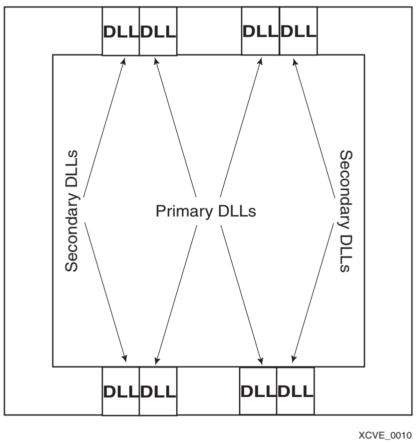

Figure 10: **DLL Locations**

Boundary Scan

Virtex-E devices support all the mandatory Boundary Scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary Scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the Boundary Scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the Boundary Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the Boundary Scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series Boundary Scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.

Table 21: **Guidelines for Max Number of Simultaneously Switching Outputs per Power/Ground Pair *(Continued)***

Standard	Package		
	BGA, CS, FGA	HQ	PQ, TQ
HSTL Class I	18	13	9
HSTL Class III	9	7	5
HSTL Class IV	5	4	3
SSTL2 Class I	15	11	8
SSTL2 Class II	10	7	5
SSTL3 Class I	11	8	6
SSTL3 Class II	7	5	4
CTT	14	10	7
AGP	9	7	5

Note: This analysis assumes a 35 pF load for each output.

Table 22: **Virtex-E Equivalent Power/Ground Pairs**

Pkg/Part	XCV100E	XCV200E	XCV300E	XCV400E	XCV600E	XCV1000E	XCV1600E	XCV2000E
CS144	12	12						
PQ240	20	20	20	20				
HQ240					20	20		
BG352	20	32	32					
BG432			32	40	40			
BG560				40	40	56	58	60
FG256(1)	20	24	24					
FG456		40	40					
FG676				54	56			
FG680(2)					46	56	56	56
FG860						58	60	64
FG900					56	58		60
FG1156						96	104	120

Notes:
1. Virtex-E devices in FG256 packages have more V_{CCO} than Virtex series devices.
2. FG680 numbers are preliminary.

Table 44: **Bidirectional I/O Library Macros**

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

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8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade(1) Min	-8	-7	-6	Units
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T_{ICK} / T_{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK} / T_{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK} / T_{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK} / T_{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK} / T_{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK} / T_{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK} / T_{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	-	416	400	357	MHz

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade(1) Min	-8	-7	-6	Units
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode						
Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

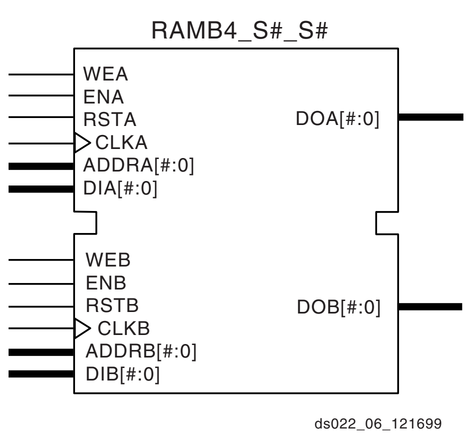

Figure 3: **Dual-Port Block SelectRAM**

Block RAM Switching Characteristics

		Speed Grade(1)				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

TBUF Switching Characteristics

		Speed Grade				
Description	**Symbol**	**Min**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P66	IO_VREF_L46P	5
P65	IO_L46N	5
P64	IO_L47P_YY	5
P63	IO_L47N_YY	5
P62	M2	NA
P61	VCCO	5
P60	M0	NA
P59	GND	NA
P58	M1	NA
P57	IO_L48N_YY	6
P56	IO_L48P_YY	6
P55	VCCO	6
P54	IO_VREF	6
P53	IO_L49N_Y	6
P52	IO_L49P_Y	6
P51	GND	NA
P50	IO_VREF_L50N_Y	6
P49	IO_L50P_Y	6
P48	IO_VREF	6
P47	IO_VREF_L51N_Y	6
P46	IO_L51P_Y	6
P45	GND	NA
P44	VCCO	6
P43	VCCINT	NA
P42	IO_L52N_YY	6
P41	IO_L52P_YY	6
P40[1]	IO_VREF	6
P39	IO_L53N_Y	6
P38	IO_L53P_Y	6
P37	GND	NA
P36	IO_VREF_L54N_Y	6
P35	IO_L54P_Y	6
P34	IO_L55N_Y	6
P33	IO_VREF_L55P_Y	6
P32	VCCINT	NA
P31	IO	6

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P30	VCCO	6
P29	GND	NA
P28	IO_L56N_YY	7
P27	IO_L56P_YY	7
P26	IO_VREF	7
P25	VCCO	7
P24	IO_L57N_Y	7
P23	IO_VREF_L57P_Y	7
P22	GND	NA
P21	IO_L58N_Y	7
P20	IO_L58P_Y	7
P19[1]	IO_VREF	7
P18	IO_L59N_YY	7
P17	IO_L59P_YY	7
P16	VCCINT	NA
P15	VCCO	7
P14	GND	NA
P13	IO_L60N_Y	7
P12	IO_VREF_L60P_Y	7
P11	IO_VREF	7
P10	IO_L61N_Y	7
P9	IO_VREF_L61P_Y	7
P8	GND	NA
P7	IO_L62N_Y	7
P6	IO_L62P_Y	7
P5	IO_VREF_L63N_Y	7
P4	IO_L63P_Y	7
P3	IO	7
P2	TMS	NA
P1	GND	NA

Notes:
1. V_{REF} or I/O option only in the XCV1000E; otherwise, I/O option only.

Table 11: **BG352 Differential Pin Pair Summary XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
55	5	AC13	AD14	√	GCLK LVDS 1/0
56	5	AD15	AC15	√	VREF_5
57	5	AE16	AE17	√	-
58	5	AC16	AF18	2	-
59	5	AD17	AC17	√	-
60	5	AD18	AC18	√	VREF_5
61	5	AF20	AE20	1	-
62	5	AE21	AD20	√	VREF_5
63	5	AF23	AE22	√	-
64	5	AC21	AE23	√	VREF_5
65	6	AD25	AC24	√	-
66	6	AC26	AD26	√	VREF_6
67	6	AB25	AA24	√	-
68	6	Y24	AA25	√	VREF_6
69	6	W24	V23	2	-
70	6	U23	Y26	√	VREF_6
71	6	U24	V25	√	-
72	6	U25	T23	1	-
73	6	T26	T25	√	-
74	6	R25	R24	√	VREF_6
75	6	P24	R26	2	-
76	7	N24	N25	√	-
77	7	M24	M25	2	-
78	7	L26	M23	√	VREF_7
79	7	L24	K25	√	-
80	7	J25	J26	1	-
81	7	H25	K23	√	-
82	7	G26	J23	√	VREF_7
83	7	H24	G25	1	-
84	7	D26	G24	√	VREF_7
85	7	F24	E25	√	-
86	7	E24	D25	√	VREF_7

Notes:
1. AO in the XCV100E.
2. AO in the XCV200E.

BG432 Ball Grid Array Packages

XCV300E, XCV400E, and XCV600E devices in BG432 Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 12, see Table 13 for Differential Pair information.

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	GCK3	D17
0	IO	A22
0	IO	A26
0	IO	B20
0	IO	C23
0	IO	C28
0	IO_L0N_Y	B29
0	IO_L0P_Y	D27
0	IO_L1N_YY	B28
0	IO_L1P_YY	C27
0	IO_VREF_L2N_YY	D26
0	IO_L2P_YY	A28
0	IO_L3N_Y	B27
0	IO_L3P_Y	C26
0	IO_L4N_YY	D25
0	IO_L4P_YY	A27
0	IO_VREF_L5N_YY	D24
0	IO_L5P_YY	C25
0	IO_L6N_Y	B25
0	IO_L6P_Y	D23
0	IO_VREF_L7N_Y	C24[1]
0	IO_L7P_Y	B24
0	IO_VREF_L8N_YY	D22
0	IO_L8P_YY	A24
0	IO_L9N_YY	C22
0	IO_L9P_YY	B22
0	IO_L10N_YY	C21
0	IO_L10P_YY	D20
0	IO_L11N_YY	B21
0	IO_L11P_YY	C20

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
6	VCCO	AL31
7	VCCO	A31
7	VCCO	L28
7	VCCO	L31
NA	GND	A2
NA	GND	A3
NA	GND	A7
NA	GND	A9
NA	GND	A14
NA	GND	A18
NA	GND	A23
NA	GND	A25
NA	GND	A29
NA	GND	A30
NA	GND	B1
NA	GND	B2
NA	GND	B30
NA	GND	B31
NA	GND	C1
NA	GND	C31
NA	GND	D16
NA	GND	G1
NA	GND	G31
NA	GND	J1
NA	GND	J31
NA	GND	P1
NA	GND	P31
NA	GND	T4
NA	GND	T28
NA	GND	V1
NA	GND	V31
NA	GND	AC1
NA	GND	AC31
NA	GND	AE1
NA	GND	AE31
NA	GND	AH16
NA	GND	AJ1
NA	GND	AJ31
NA	GND	AK1
NA	GND	AK2
NA	GND	AK30
NA	GND	AK31
NA	GND	AL2
NA	GND	AL3
NA	GND	AL7
NA	GND	AL9
NA	GND	AL14
NA	GND	AL18
NA	GND	AL23
NA	GND	AL25
NA	GND	AL29
NA	GND	AL30

Notes:

1. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV400E, XCV600E; otherwise, I/O option only.

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	1	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	1	VREF
129	5	AF7	AB9	1	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	2	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	2	-
140	6	Y5	AB3	1	VREF
141	6	V7	AB2	1	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	2	-
146	6	U7	Y1	1	VREF
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	2	-
152	6	T6	U2	1	-
153	6	T4	U1	1	-
154	6	T3	R7	1	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	2	-
158	6	P6	R1	1	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	1	VREF
163	7	M7	N7	2	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	1	-
167	7	K2	L6	1	-
168	7	K1	L4	1	-
169	7	L5	K3	2	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	1	VREF
175	7	J6	G2	2	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	1	-
179	7	H6	E2	2	-
180	7	F4	G5	1	VREF
181	7	G6	H7	2	-
182	7	E4	E3	√	-

Notes:
1. AO in the XCV600E.
2. AO in the XCV400E.

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L63N	G4
2	IO_L64P	G3
2	IO_L64N	E2
2	IO_VREF_L65P_Y	H4
2	IO_L65N_Y	E1
2	IO_L66P_YY	H3
2	IO_L66N_YY	F2
2	IO_L67P	J4
2	IO_L67N	F1
2	IO_L68P_Y	J3
2	IO_L68N_Y	G2
2	IO_VREF_L69P_YY	G1
2	IO_L69N_YY	K4
2	IO_L70P_YY	H2
2	IO_L70N_YY	K3
2	IO_VREF_L71P	H1[3]
2	IO_L71N	L4
2	IO_L72P	J2
2	IO_L72N	L3
2	IO_VREF_L73P_YY	J1
2	IO_L73N_YY	M3
2	IO_L74P_YY	K2
2	IO_L74N_YY	N4
2	IO_L75P	K1
2	IO_L75N	N3
2	IO_VREF_L76P_YY	L2
2	IO_D1_L76N_YY	P4
2	IO_D2_L77P_YY	P3
2	IO_L77N_YY	L1
2	IO_L78P_Y	R4
2	IO_L78N_Y	M2
2	IO_L79P	R3
2	IO_L79N	M1
2	IO_L80P	T4
2	IO_L80N	N2
2	IO_VREF_L81P_Y	N1[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
2	IO_L81N_Y	T3
2	IO_L82P_YY	P2
2	IO_L82N_YY	U5
2	IO_L83P	P1
2	IO_L83N	U4
2	IO_L84P_Y	R2
2	IO_L84N_Y	U3
2	IO_VREF_L85P_YY	V5
2	IO_D3_L85N_YY	R1
2	IO_L86P_YY	V4
2	IO_L86N_YY	T2
2	IO_L87P	V3
2	IO_L87N	T1
2	IO_L88P	W4
2	IO_L88N	U2
2	IO_VREF_L89P_YY	W3
2	IO_L89N_YY	U1
2	IO_L90P_YY	AA3
2	IO_L90N_YY	V2
2	IO_VREF_L91P	AA4[2]
2	IO_L91N	V1
2	IO_L92P_YY	AB2
2	IO_L92N_YY	W2
3	IO	AP3
3	IO	AT3
3	IO	AB3
3	IO_L93P	AB4
3	IO_VREF_L93N	W1[2]
3	IO_L94P_YY	AB5
3	IO_L94N_YY	Y2
3	IO_L95P_YY	AC2
3	IO_VREF_L95N_YY	Y1
3	IO_L96P	AC3
3	IO_L96N	AA1
3	IO_L97P	AC4

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L147N_YY	AW7
4	IO_L148P_Y	AY7
4	IO_L148N_Y	BB8
4	IO_L149P_Y	BA9
4	IO_L149N_Y	AV8
4	IO_L150P_YY	AW8
4	IO_L150N_YY	BA10
4	IO_VREF_L151P_YY	BB10
4	IO_L151N_YY	AY8
4	IO_L152P_Y	AV9
4	IO_L152N_Y	BA11
4	IO_VREF_L153P_Y	BB11[2]
4	IO_L153N_Y	AW9
4	IO_L154P_YY	AY9
4	IO_L154N_YY	BA12
4	IO_VREF_L155P_YY	BB12
4	IO_L155N_YY	AV10
4	IO_L156P_Y	BA13
4	IO_L156N_Y	AW10
4	IO_L157P_Y	BB13
4	IO_L157N_Y	AY10
4	IO_VREF_L158P_YY	AV11
4	IO_L158N_YY	BA14
4	IO_L159P_YY	AW11
4	IO_L159N_YY	BB14
4	IO_L160P_Y	AV12
4	IO_L160N_Y	BA15
4	IO_L161P_Y	AW12
4	IO_L161N_Y	AY15
4	IO_L162P_Y	AW13
4	IO_L162N_Y	BB15
4	IO_L163P_Y	AV14
4	IO_L163N_Y	BA16
4	IO_L164P_YY	AW14
4	IO_L164N_YY	AY16
4	IO_VREF_L165P_YY	BB16
4	IO_L165N_YY	AV15

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L166P_Y	AY17
4	IO_L166N_Y	AW15
4	IO_L167P_Y	BB17
4	IO_L167N_Y	AU16
4	IO_L168P_YY	AV16
4	IO_L168N_YY	AY18
4	IO_VREF_L169P_YY	AW16
4	IO_L169N_YY	BA18
4	IO_L170P_Y	BB19
4	IO_L170N_Y	AW17
4	IO_L171P_Y	AY19
4	IO_L171N_Y	AV18
4	IO_L172P_YY	AW18
4	IO_L172N_YY	BB20
4	IO_VREF_L173P_YY	AY20
4	IO_L173N_YY	AV19
4	IO_L174P_Y	BB21
4	IO_L174N_Y	AW19
4	IO_VREF_L175P_Y	AY21[1]
4	IO_L175N_Y	AV20
4	IO_LVDS_DLL_L176P	AW20
5	GCK1	AY22
5	IO	AV24
5	IO	AV34
5	IO	AW27
5	IO	AW36
5	IO	AY23
5	IO	AY31
5	IO	AY33
5	IO	BA26
5	IO	BA29
5	IO	BA33
5	IO	BB25
5	IO_LVDS_DLL_L176N	AW21
5	IO_L177P_Y	BB22
5	IO_VREF_L177N_Y	AW22[1]

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40[2]
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO	J20[5]
1	IO	L18[4]
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N_YY	B16
1	IO_VREF_L35P_YY	F16[2]
1	IO_L36N_YY	A16
1	IO_L36P_YY	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N_Y	A17
1	IO_L39P_Y	E17
1	IO_L40N_Y	F17
1	IO_L40P_Y	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N_Y	B19
1	IO_L43P_Y	G18
1	IO_L44N_Y	D19
1	IO_L44P_Y	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19[1]
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L47N_Y	D20[4]
1	IO_L47P_Y	A20[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L50N_YY	B21[4]
1	IO_L50P_YY	D21[4]
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N_YY	H19
1	IO_L53P_YY	B22
1	IO_L54N_YY	E21
1	IO_L54P_YY	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N_Y	G21
1	IO_L57P_Y	A23
1	IO_L58N_Y	A24
1	IO_L58P_Y	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N_Y	E23
1	IO_L61P_Y	C25
1	IO_L62N_Y	D24
1	IO_L62P_Y	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L65N_Y	C26[4]
1	IO_L65P_Y	F23[4]
1	IO_L66N_Y	B27
1	IO_VREF_L66P_Y	G23[1]
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_L68N_YY	B28[3]
1	IO_L68P_YY	A28[4]
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AA30	W24	4	-
121	3	AA29	V20	1	-
122	3	Y27	W23	NA	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	4	-
126	3	W22	Y23	4	-
127	3	Y24	AB28	4	VREF
128	3	AC30	AA25	√	-
129	3	W21	AA24	2	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	2	-
133	3	AC26	AE30	4	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	1	VREF
136	3	AB23	AE28	4	-
137	3	AG30	AC25	3	-
138	3	AE26	AG29	4	VREF
139	3	AH30	AC24	1	-
140	3	AF28	AD25	NA	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
143	4	AG26	AH27	4	-
144	4	AD23	AJ27	2	-
145	4	AB21	AF25	2	VREF
146	4	AC22	AH26	2	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	1	-
150	4	AC21	AF24	1	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	2	-

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AC20	AG23	2	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
157	4	AK24	AD20	NA	-
158	4	AA19	AF21	4	-
159	4	AH22	AA18	NA	VREF
160	4	AG21	AK23	NA	-
161	4	AH21	AD19	4	-
162	4	AE20	AJ21	2	-
163	4	AG20	AF20	2	-
164	4	AC18	AF19	2	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	1	-
168	4	AJ19	AD17	1	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	2	-
172	4	AK19	AD16	2	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
175	4	AD15	AH17	NA	-
176	4	AG16	AK17	4	VREF
177	5	AF16	AH16	NA	IO_ LVDS_DLL
178	5	AC15	AG15	4	VREF
179	5	AB15	AF15	√	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	2	-
183	5	AH14	AJ14	2	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	1	-
187	5	AC13	AA13	1	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
71	1	A27	G24	3200 2000 1000	-
72	1	G25	B27	3200 1600	-
73	1	C27	E26	3200 2600 2000 1600 1000	VREF
74	1	B28	J24	3200 2600 2000 1600 1000	-
75	1	H25	K24	3200 2600	-
76	1	F26	D27	3200 1000	-
77	1	C28	G26	3200 1000	-
78	1	J25	E27	2000 1600	-
79	1	H26	A30	3200 2600 2000 1600 1000	VREF
80	1	B29	G27	3200 2600 2000 1600 1000	-
81	1	C29	F27	3200 2600 1000	-
82	1	F28	E28	3200 2000 1000	VREF
83	1	B30	L25	3200 2000 1000	-
84	1	E29	B31	3200 1600 1000	-
85	1	D30	A31	3200 2600 2000 1600 1000	CS
86	2	D32	J27	3200 2600 2000 1600 1000	DIN, D0
87	2	E31	F30	3200 2600 2000	-
88	2	G29	F32	2600 2000 1000	-
89	2	E32	G30	3200 2600 1600 1000	VREF
90	2	M25	G31	2600 1600	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
91	2	L26	D33	3200 2600 1600 1000	-
92	2	D34	H29	2600 2000 1000	VREF
93	2	J28	E33	3200 2600 2000 1600	-
94	2	H28	H30	3200 2600 2000 1600 1000	-
95	2	H32	K28	3200 2600 1600 1000	-
96	2	L27	F33	3200 2600 2000	-
97	2	M26	E34	2600 2000 1000	-
98	2	H31	G32	3200 2600 2000 1600 1000	VREF
99	2	N25	J31	2000 1600	-
100	2	J30	G33	3200 2600 2000 1600 1000	-
101	2	H34	J29	2600 1000	VREF
102	2	M27	H33	3200 2600 1600	-
103	2	K29	J34	3200 2600 1600 1000	-
104	2	L29	J33	3200 2600 2000 1600 1000	VREF
105	2	M28	K34	3200 2600 2000 1600 1000	-
106	2	N27	L34	3200 1600 1000	-
107	2	K33	P26	2000 1600 1000	D1
108	2	R25	M34	3200 2600 2000	-
109	2	L31	L33	2000 1000	-
110	2	P27	M33	3200 2600 1600 1000	-