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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	393216
Number of I/O	512
Number of Gates	1569178
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	680-LBGA Exposed Pad
Supplier Device Package	680-FTEBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000e-7fg680i

Virtex-E Ordering Information

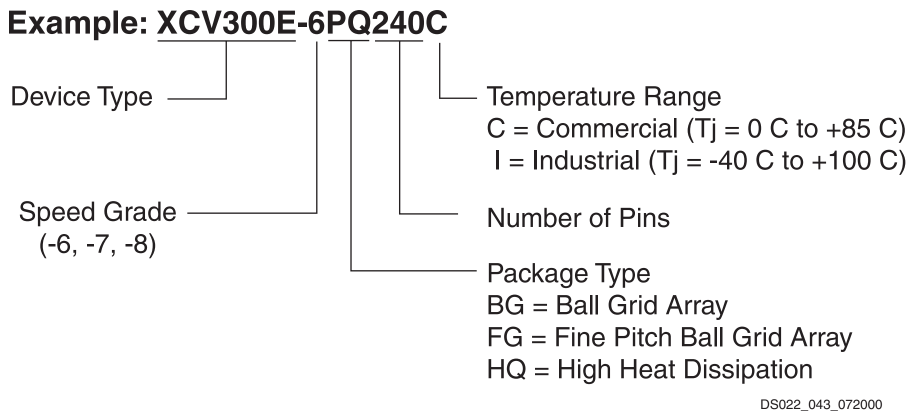

Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to "No Connect in the XCV100E" and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to "No connect in XCV600E" in Table 74 (Module 4). • Changed pin J30 to "VREF option only in the XCV600E" in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be "AO in the XCV1000E, XCV1600E".

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but I/Os can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible Boundary Scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

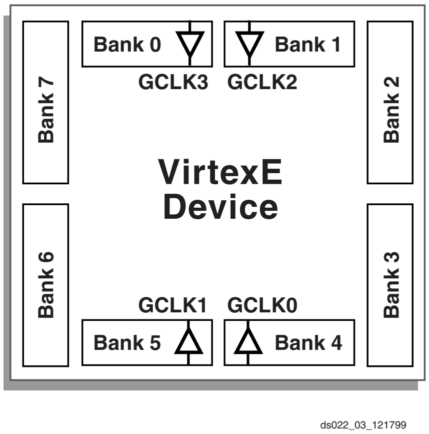

Figure 3: **Virtex-E I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or can be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

Configurable Logic Blocks

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

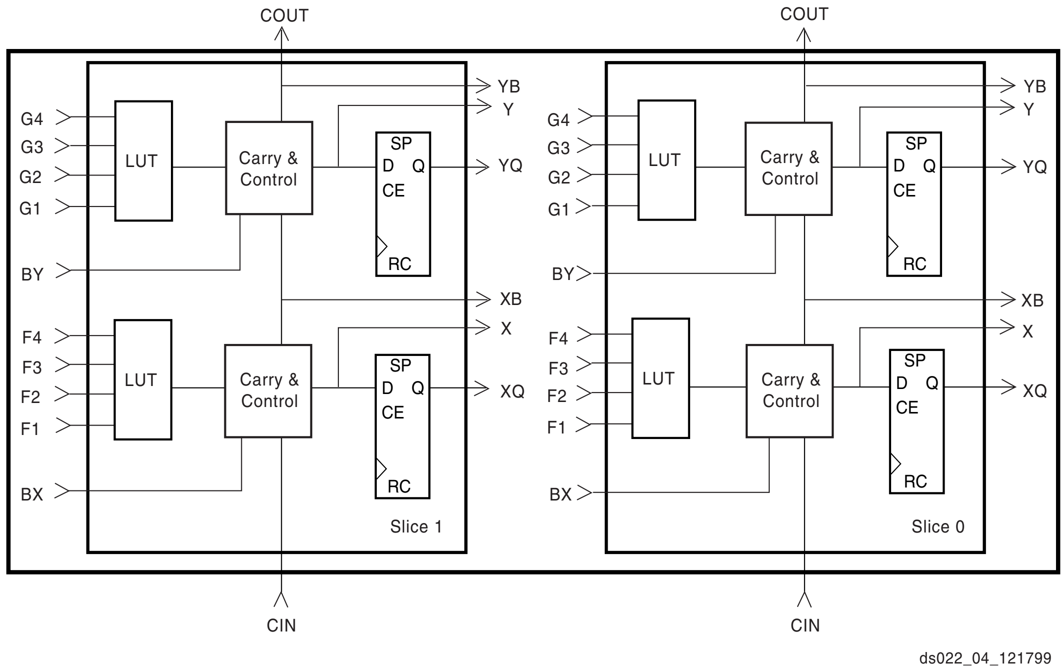

Figure 4: **2-Slice Virtex-E CLB**

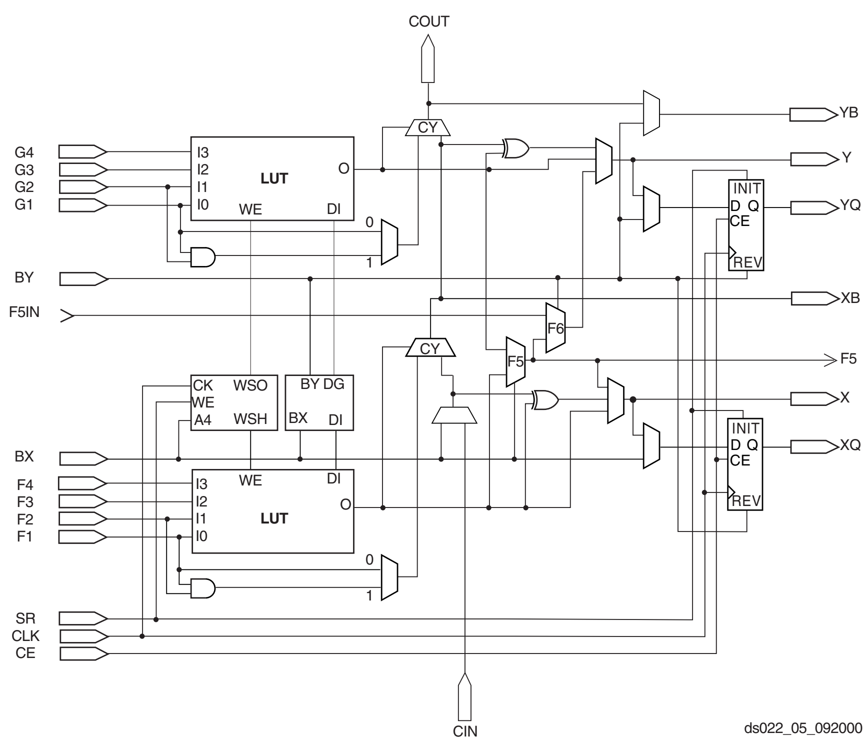

Figure 5: **Detailed View of Virtex-E Slice**

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

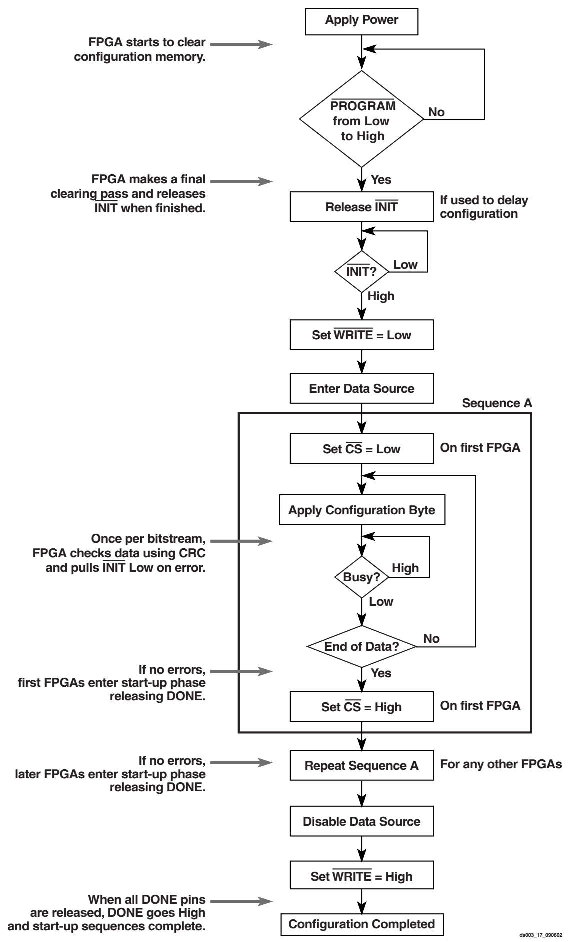

Figure 18: **SelectMAP Flowchart for Write Operations**

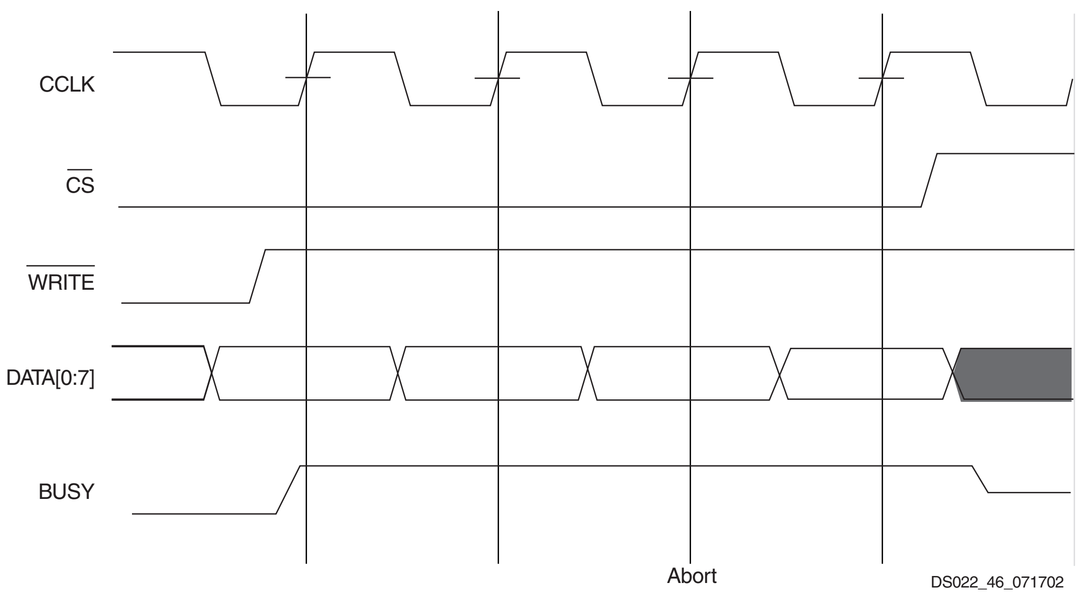

Figure 19: **SelectMAP Write Abort Waveforms**

Boundary Scan Mode

In the Boundary Scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{\text{PROGRAM}}$ pin resets the TAP controller and no JTAG operations can be performed.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

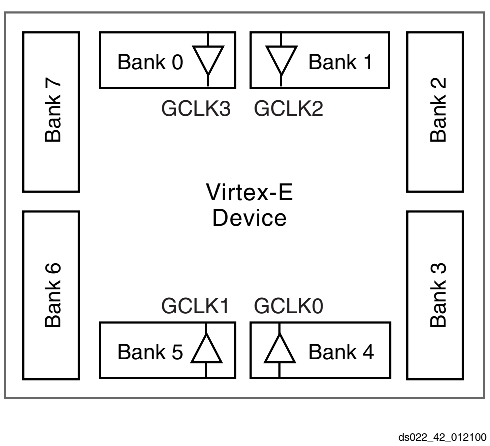

Figure 38: **Virtex-E I/O Banks**

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

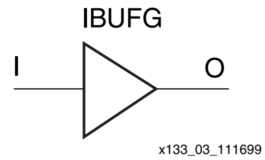

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs:
Introduction and Ordering Information (Module 1)
- DS022-2, Virtex-E 1.8V FPGAs:
Functional Description (Module 2)
- DS022-3, Virtex-E 1.8V FPGAs:
DC and Switching Characteristics (Module 3)
- DS022-4, Virtex-E 1.8V FPGAs:
Pinout Tables (Module 4)

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description(2)	Current Requirement(3)
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:

1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Virtex-E Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description(1)	Symbol	Device	Speed Grade(2, 3)				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	$T_{ICKOFDLL}$	XCV50E	1.0	3.1	3.1	3.1	ns
		XCV100E	1.0	3.1	3.1	3.1	ns
		XCV200E	1.0	3.1	3.1	3.1	ns
		XCV300E	1.0	3.1	3.1	3.1	ns
		XCV400E	1.0	3.1	3.1	3.1	ns
		XCV600E	1.0	3.1	3.1	3.1	ns
		XCV1000E	1.0	3.1	3.1	3.1	ns
		XCV1600E	1.0	3.1	3.1	3.1	ns
		XCV2000E	1.0	3.1	3.1	3.1	ns
		XCV2600E	1.0	3.1	3.1	3.1	ns
		XCV3200E	1.0	3.1	3.1	3.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.
3. DLL output jitter is already included in the timing calculation.

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
6	IO_L74P _Y	R25
6	IO_L75N	R26
6	IO_L75P	P24
6	IO	P23[1]
6	IO	N26
7	IO_L76N_YY	N25
7	IO_L76P_YY	N24
7	IO	M26[1]
7	IO_L77N	M25
7	IO_L77P	M24
7	IO_L78N _Y	M23
7	IO_VREF_7_L78P _Y	L26
7	IO_L79N_YY	K25
7	IO_L79P_YY	L24
7	IO	L23[1]
7	IO_L80N	J26
7	IO_L80P	J25
7	IO	K24[1]
7	IO_L81N_YY	K23
7	IO_L81P_YY	H25
7	IO_L82N _Y	J23
7	IO_VREF_7_L82P _Y	G26
7	IO_L83N _Y	G25
7	IO_L83P _Y	H24
7	IO	H23
7	IO	F26[1]
7	IO	F25[1]
7	IO_L84N_Y	G24
7	IO_VREF_7_L84P_Y	D26
7	IO_L85N_YY	E25
7	IO_L85P_YY	F24
7	IO	F23[1]
7	IO_L86N_YY	D25

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
7	IO_VREF_7_L86P_YY	E24[2]
7	IO	C26
7	IO	E23[1]
7	IO	D24[1]
7	IO	C25
NA	TDI	B3
NA	TDO	D4
NA	CCLK	C3
NA	TCK	C24
NA	TMS	D23
NA	PROGRAM	AC4
NA	DONE	AD3
NA	DXN	AD23
NA	DXP	AE24
NA	M2	AC23
NA	M0	AD24
NA	M1	AB23
NA	VCCINT	A20
NA	VCCINT	B16
NA	VCCINT	C14
NA	VCCINT	D12
NA	VCCINT	D10
NA	VCCINT	K4
NA	VCCINT	L1
NA	VCCINT	P2
NA	VCCINT	T1
NA	VCCINT	W2
NA	VCCINT	AC10
NA	VCCINT	AF11
NA	VCCINT	AE14
NA	VCCINT	AF16
NA	VCCINT	AE19

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L70N_Y	AK4
4	IO_L71P_YY	AJ5
4	IO_L71N_YY	AH6
4	IO_VREF_L72P_YY	AL4
4	IO_L72N_YY	AK5
4	IO_L73P_Y	AJ6
4	IO_L73N_Y	AH7
4	IO_L74P_YY	AL5
4	IO_L74N_YY	AK6
4	IO_VREF_L75P_YY	AJ7
4	IO_L75N_YY	AL6
4	IO_L76P_Y	AH9
4	IO_L76N_Y	AJ8
4	IO_VREF_L77P_Y	AK8[1]
4	IO_L77N_Y	AJ9
4	IO_VREF_L78P_YY	AL8
4	IO_L78N_YY	AK9
4	IO_L79P_YY	AK10
4	IO_L79N_YY	AL10
4	IO_L80P_YY	AH12
4	IO_L80N_YY	AK11
4	IO_L81P_YY	AJ12
4	IO_L81N_YY	AK12
4	IO_L82P_YY	AH13
4	IO_L82N_YY	AJ13
4	IO_VREF_L83P_YY	AL13
4	IO_L83N_YY	AK14
4	IO_L84P_Y	AH14
4	IO_L84N_Y	AJ14
4	IO_VREF_L85P_Y	AK15[2]
4	IO_L85N_Y	AJ15
4	IO_LVDS_DLL_L86P	AH15
5	GCK1	AK16
5	IO	AH20
5	IO	AJ19
5	IO	AJ23
5	IO	AJ24
5	IO_LVDS_DLL_L86N	AL17
5	IO_L87P_Y	AK17
5	IO_VREF_L87N_Y	AJ17[2]
5	IO_L88P_Y	AH17
5	IO_L88N_Y	AK18
5	IO_L89P_YY	AL19
5	IO_VREF_L89N_YY	AJ18
5	IO_L90P_YY	AH18
5	IO_L90N_YY	AL20
5	IO_L91P_YY	AK20
5	IO_L91N_YY	AH19
5	IO_L92P_YY	AJ20
5	IO_L92N_YY	AK21
5	IO_L93P_YY	AJ21
5	IO_L93N_YY	AL22
5	IO_L94P_YY	AJ22
5	IO_VREF_L94N_YY	AK23
5	IO_L95P_Y	AH22
5	IO_VREF_L95N_Y	AL24[1]
5	IO_L96P_Y	AK24
5	IO_L96N_Y	AH23
5	IO_L97P_YY	AK25
5	IO_VREF_L97N_YY	AJ25
5	IO_L98P_YY	AL26
5	IO_L98N_YY	AK26
5	IO_L99P_Y	AH25
5	IO_L99N_Y	AL27
5	IO_L100P_YY	AJ26
5	IO_VREF_L100N_YY	AK27
5	IO_L101P_YY	AH26
5	IO_L101N_YY	AL28
5	IO_L102P_Y	AJ27
5	IO_L102N_Y	AK28

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO_L132P_Y	G28
7	IO_L133N	E31
7	IO_L133P	E30
7	IO_L134N_Y	F29
7	IO_VREF_L134P_Y	F28
7	IO_L135N_Y	D31
7	IO_L135P_Y	D30
7	IO_L136N	E29
7	IO_L136P	E28
2	CCLK	D4
3	DONE	AH4
NA	DXN	AH27
NA	DXP	AK29
NA	M0	AH28
NA	M1	AH29
NA	M2	AJ28
NA	PROGRAM	AH3
NA	TCK	D28
NA	TDI	B3
2	TDO	C4
NA	TMS	D29
NA	VCCINT	A10
NA	VCCINT	A17
NA	VCCINT	B23
NA	VCCINT	B26
NA	VCCINT	C7
NA	VCCINT	C14
NA	VCCINT	C19
NA	VCCINT	F1
NA	VCCINT	F30
NA	VCCINT	K3
NA	VCCINT	K29
NA	VCCINT	N2
NA	VCCINT	N29

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	VCCINT	T1
NA	VCCINT	T29
NA	VCCINT	W2
NA	VCCINT	W31
NA	VCCINT	AB2
NA	VCCINT	AB30
NA	VCCINT	AE29
NA	VCCINT	AF1
NA	VCCINT	AH8
NA	VCCINT	AH24
NA	VCCINT	AJ10
NA	VCCINT	AJ16
NA	VCCINT	AK22
NA	VCCINT	AK13
NA	VCCINT	AK19
0	VCCO	A21
0	VCCO	C29
0	VCCO	D21
1	VCCO	A1
1	VCCO	A11
1	VCCO	D11
2	VCCO	C3
2	VCCO	L4
2	VCCO	L1
3	VCCO	AA1
3	VCCO	AA4
3	VCCO	AJ3
4	VCCO	AH11
4	VCCO	AL1
4	VCCO	AL11
5	VCCO	AH21
5	VCCO	AL21
5	VCCO	AJ29
6	VCCO	AA28
6	VCCO	AA31

FG456 Fine-Pitch Ball Grid Array Packages

XCV200E and XCV300E devices in FG456 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in both devices provided in this package. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 18, see Table 19 for Differential Pair information.

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
0	GCK3	C11
0	IO	A2[1]
0	IO	A3
0	IO	A6[1]
0	IO	A10
0	IO	B5
0	IO	B9
0	IO	C5
0	IO	D8
0	IO	D10
0	IO	E11[1]
0	IO_L0N	D5
0	IO_L0P	B3
0	IO_VREF_L1N_YY	B4
0	IO_L1P_YY	E6
0	IO_L2N	A4
0	IO_L2P	E7
0	IO_VREF_L3N_YY	C6
0	IO_L3P_YY	D6
0	IO_L4N_Y	A5
0	IO_L4P_Y	B6
0	IO_L5N_Y	D7
0	IO_L5P_Y	C7
0	IO_VREF_L6N_YY	E8
0	IO_L6P_YY	B7
0	IO_L7N_YY	A7
0	IO_L7P_YY	E9
0	IO_L8N_Y	C8
0	IO_L8P_Y	B8
0	IO_L9N_Y	D9
0	IO_L9P_Y	A8
0	IO_L10N	C9
0	IO_L10P	E10
0	IO_VREF_L11N_YY	A9
0	IO_L11P_YY	C10
0	IO_L12N_Y	F11
0	IO_L12P_Y	B10
0	IO_LVDS_DLL_L13N	B11
1	GCK2	A11
1	IO	A12[1]
1	IO	A14
1	IO	B16[1]
1	IO	B19
1	IO	E13
1	IO	E15
1	IO	E16
1	IO	E17[1]
1	IO_LVDS_DLL_L13P	D11
1	IO_L14N_Y	C12
1	IO_L14P_Y	D12
1	IO_L15N_Y	B12
1	IO_L15P_Y	A13
1	IO_L16N_YY	E12
1	IO_VREF_L16P_YY	B13
1	IO_L17N_YY	C13
1	IO_L17P_YY	D13
1	IO_L18N_Y	B14
1	IO_L18P_Y	C14
1	IO_L19N_Y	F12
1	IO_L19P_Y	A15
1	IO_L20N_YY	B15
1	IO_L20P_YY	C15
1	IO_L21N_YY	A16
1	IO_VREF_L21P_YY	E14
1	IO_L22N_Y	D14
1	IO_L22P_Y	C16
1	IO_L23N_Y	D15

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
4	IO_L98N_YY	AB19
4	IO_L99P_YY	AC20
4	IO_L99N_YY	AA18
4	IO_L100P_Y	AC19
4	IO_L100N_Y	AD20
4	IO_VREF_L101P_Y	AF20[2]
4	IO_L101N_Y	AB18
4	IO_L102P	AD19
4	IO_L102N	Y17
4	IO_L103P	AE19
4	IO_VREF_L103N	AD18
4	IO_L104P_YY	AF19
4	IO_L104N_YY	AA17
4	IO_L105P_Y	AC17
4	IO_L105N_Y	AB17
4	IO_L106P_YY	Y16
4	IO_L106N_YY	AE17
4	IO_L107P_YY	AF17
4	IO_L107N_YY	AA16
4	IO_L108P	AD17
4	IO_L108N	AB16
4	IO_L109P_YY	AC16
4	IO_L109N_YY	AD16
4	IO_VREF_L110P_YY	AC15
4	IO_L110N_YY	Y15
4	IO_L111P_YY	AD15
4	IO_L111N_YY	AA15
4	IO_L112P_Y	W14
4	IO_L112N_Y	AB15
4	IO_VREF_L113P_Y	AF15
4	IO_L113N_Y	Y14
4	IO_L114P	AD14
4	IO_L114N	AB14
4	IO_LVDS_DLL_L115P	AC14
5	GCK1	AB13
5	IO	Y13[1]

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
5	IO	AD7
5	IO	AD13
5	IO	AE4
5	IO	AE7
5	IO	AE12[1]
5	IO	AF3[1]
5	IO	AF5
5	IO	AF10[1]
5	IO	AF11[1]
5	IO_LVDS_DLL_L115N	AF13
5	IO_L116P_Y	AA13
5	IO_VREF_L116N_Y	AF12
5	IO_L117P_Y	AC13
5	IO_L117N_Y	W13
5	IO_L118P_YY	AA12
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_VREF_L128N_Y	AF8[2]
5	IO_L129P_Y	AF7

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
5	IO_L129N_Y	AB9
5	IO_L130P_YY	AA9
5	IO_L130N_YY	AF6
5	IO_L131P_YY	AC8
5	IO_VREF_L131N_YY	AC7
5	IO_L132P_YY	AD6
5	IO_L132N_YY	Y9
5	IO_L133P_YY	AE5
5	IO_L133N_YY	AA8
5	IO_L134P_YY	AC6
5	IO_VREF_L134N_YY	AB8
5	IO_L135P_YY	AD5
5	IO_L135N_YY	AA7
5	IO_L136P_Y	AF4
5	IO_L136N_Y	AC5
6	IO	P3
6	IO	AA3
6	IO	AC1[1]
6	IO	P1[1]
6	IO	R2[1]
6	IO	T1[1]
6	IO	V1[1]
6	IO	W3
6	IO	Y2
6	IO	Y6
6	IO_L137N_YY	AA5
6	IO_L137P_YY	AC3
6	IO_L138N_YY	AC2
6	IO_L138P_YY	AB4
6	IO_L139N_Y	W6
6	IO_L139P_Y	AA4
6	IO_VREF_L140N_Y	AB3
6	IO_L140P_Y	Y5
6	IO_L141N_Y	AB2
6	IO_L141P_Y	V7
6	IO_L142N_YY	AB1
6	IO_L142P_YY	Y4
6	IO_VREF_L143N_YY	V5
6	IO_L143P_YY	W5
6	IO_L144N_YY	AA1
6	IO_L144P_YY	V6
6	IO_L145N_Y	W4
6	IO_L145P_Y	Y3
6	IO_VREF_L146N_Y	Y1[2]
6	IO_L146P_Y	U7
6	IO_L147N_YY	W1
6	IO_L147P_YY	V4
6	IO_L148N_YY	W2
6	IO_VREF_L148P_YY	U6
6	IO_L149N_YY	V3
6	IO_L149P_YY	T5
6	IO_L150N_YY	U5
6	IO_L150P_YY	U4
6	IO_L151N_Y	T7
6	IO_L151P_Y	U3
6	IO_L152N_Y	U2
6	IO_L152P_Y	T6
6	IO_L153N_Y	U1
6	IO_L153P_Y	T4
6	IO_L154N_Y	R7
6	IO_L154P_Y	T3
6	IO_VREF_L155N_YY	R4
6	IO_L155P_YY	R6
6	IO_L156N_YY	R3
6	IO_L156P_YY	R5
6	IO_L157N_Y	P8
6	IO_L157P_Y	P7
6	IO_VREF_L158N_Y	R1
6	IO_L158P_Y	P6
6	IO_L159N_YY	P5
6	IO_L159P_YY	P4
7	IO	D1[1]

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_VREF_L200N_YY	AH39
6	IO_L200P_YY	AG38
6	IO_L201N_YY	AG36
6	IO_L201P_YY	AG39
6	IO_L202N_Y	AG37
6	IO_L202P_Y	AF39
6	IO_L203N	AF36
6	IO_L203P	AE38
6	IO_L204N	AF37
6	IO_L204P	AF38
6	IO_VREF_L205N_Y	AE39[1]
6	IO_L205P_Y	AE36
6	IO_L206N_YY	AD38
6	IO_L206P_YY	AE37
6	IO_L207N	AD39
6	IO_L207P	AD36
6	IO_L208N_Y	AC38
6	IO_L208P_Y	AC39
6	IO_VREF_L209N_YY	AD37
6	IO_L209P_YY	AB38
6	IO_L210N_YY	AC35
6	IO_L210P_YY	AB39
6	IO_L211N	AC36
6	IO_L211P	AA38
6	IO_L212N	AC37
6	IO_L212P	AA39
6	IO_VREF_L213N_YY	AB35
6	IO_L213P_YY	Y38
6	IO_L214N_YY	AB36
6	IO_L214P_YY	Y39
6	IO_VREF_L215N	AB37[2]
6	IO_L215P	AA36
7	IO	C38
7	IO	B37
7	IO	F37

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L216N_YY	AA37
7	IO_L216P_YY	W38
7	IO_L217N	W37
7	IO_VREF_L217P	V39[2]
7	IO_L218N_YY	W36
7	IO_L218P_YY	U39
7	IO_L219N_YY	V38
7	IO_VREF_L219P_YY	U38
7	IO_L220N	V37
7	IO_L220P	T39
7	IO_L221N	V36
7	IO_L221P	T38
7	IO_L222N_YY	V35
7	IO_L222P_YY	R39
7	IO_L223N_YY	U37
7	IO_VREF_L223P_YY	U36
7	IO_L224N_Y	R38
7	IO_L224P_Y	U35
7	IO_L225N	P39
7	IO_L225P	T37
7	IO_L226N_YY	P38
7	IO_L226P_YY	T36
7	IO_L227N_Y	N39
7	IO_VREF_L227P_Y	N38[1]
7	IO_L228N	R37
7	IO_L228P	M39
7	IO_L229N	R36
7	IO_L229P	M38
7	IO_L230N_Y	P37
7	IO_L230P_Y	L39
7	IO_L231N_YY	P36
7	IO_L231P_YY	N37
7	IO_L232N_YY	L38
7	IO_VREF_L232P_YY	N36
7	IO_L233N	K39
7	IO_L233P	M37

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L127P_YY	Y24
3	IO_VREF_L127N_YY	AB28
3	IO_L128P_YY	AC30
3	IO_L128N_YY	AA25
3	IO_L129P	W21
3	IO_L129N	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P_YY	AC26
3	IO_L133N_YY	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P	AF29
3	IO_VREF_L135N	AB24
3	IO_L136P_YY	AB23
3	IO_L136N_YY	AE28
3	IO_L137P_Y	AG30[3]
3	IO_L137N_Y	AC25[4]
3	IO_L138P_YY	AE26
3	IO_VREF_L138N_YY	AG29[1]
3	IO_L139P	AH30
3	IO_L139N	AC24
3	IO_L140P	AF28[3]
3	IO_L140N	AD25[4]
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19[4]
4	IO	AC16[4]
4	IO	AC19
4	IO	AD18[4]
4	IO	AD21[4]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO	AE15[4]
4	IO	AE18[4]
4	IO	AE21
4	IO	AE24[5]
4	IO	AF17[5]
4	IO	AF18[5]
4	IO	AJ18[4]
4	IO	AK18
4	IO	AK25[5]
4	IO	AK27[4]
4	IO	AH23[4]
4	IO	AH24[5]
4	IO_L142P_YY	AF27
4	IO_L142N_YY	AK28
4	IO_L143P_YY	AG26[4]
4	IO_L143N_YY	AH27[3]
4	IO_L144P	AD23
4	IO_L144N	AJ27
4	IO_VREF_L145P	AB21[1]
4	IO_L145N	AF25
4	IO_L146P	AC22[4]
4	IO_L146N	AH26[4]
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCINT	N22
NA	VCCINT	P13
NA	VCCINT	P22
NA	VCCINT	R13
NA	VCCINT	R22
NA	VCCINT	T13
NA	VCCINT	T22
NA	VCCINT	U10
NA	VCCINT	U25
NA	VCCINT	V10
NA	VCCINT	V25
NA	VCCINT	W13
NA	VCCINT	W22
NA	VCCINT	Y13
NA	VCCINT	Y22
NA	VCCINT	AA13
NA	VCCINT	AA22
NA	VCCINT	AB13
NA	VCCINT	AB14
NA	VCCINT	AB15
NA	VCCINT	AB16
NA	VCCINT	AB19
NA	VCCINT	AB20
NA	VCCINT	AB21
NA	VCCINT	AB22
NA	VCCINT	AC12
NA	VCCINT	AC23
NA	VCCINT	AD24
NA	VCCINT	AD11
NA	VCCINT	AE10
NA	VCCINT	AE17
NA	VCCINT	AE18
NA	VCCINT	AE25

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_0	M17
NA	VCCO_0	L17
NA	VCCO_0	L16
NA	VCCO_0	E10
NA	VCCO_0	C14
NA	VCCO_0	A6
NA	VCCO_0	M13
NA	VCCO_0	M14
NA	VCCO_0	M15
NA	VCCO_0	M16
NA	VCCO_0	L12
NA	VCCO_0	L13
NA	VCCO_0	L14
NA	VCCO_0	L15
NA	VCCO_1	M18
NA	VCCO_1	L18
NA	VCCO_1	L23
NA	VCCO_1	E25
NA	VCCO_1	C21
NA	VCCO_1	A29
NA	VCCO_1	M19
NA	VCCO_1	M20
NA	VCCO_1	M21
NA	VCCO_1	M22
NA	VCCO_1	L19
NA	VCCO_1	L20
NA	VCCO_1	L21
NA	VCCO_1	L22
NA	VCCO_2	U24
NA	VCCO_2	U23
NA	VCCO_2	N24
NA	VCCO_2	M24
NA	VCCO_2	K30
NA	VCCO_2	F34

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
270	6	AG2	AE7	2600 2000 1000	-
271	6	AG1	AF6	3200 2600 2000 1600 1000	VREF
272	6	AG4	AC9	2000 1600	-
273	6	AF3	AE6	3200 2600 2000 1600 1000	-
274	6	AF4	AF1	2600 1000	VREF
275	6	AF2	AB10	3200 2600 1600	-
276	6	AE1	AC8	3200 2600 1600 1000	-
277	6	AE3	AD5	3200 2600 2000 1600 1000	VREF
278	6	AD1	AC7	3200 2600 2000 1600 1000	-
279	6	AD2	AD6	3200 1600 1000	-
280	6	AC1	AB8	2000 1600 1000	VREF
281	6	AC2	AC5	3200 2600 2000 1600 1000	-
282	6	AC3	AA9	3200 2600 2000	-
283	6	AD4	AC4	2000 1000	-
284	6	AB6	AA8	3200 2600 1600 1000	-
285	6	Y10	AB1	2600 1600	-
286	6	AA7	AB2	3200 1600 1000	-
287	6	AA1	AA4	2600 2000 1000	VREF
288	6	AB4	Y9	3200 2600 2000 1600	-
289	6	Y8	AA2	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
290	6	AA5	AA6	3200 2600 1600 1000	-
291	6	Y7	AB3	3200 2600 2000	-
292	6	W10	Y1	2600 2000 1000	-
293	6	Y2	Y5	2000 1600 1000	VREF
294	6	W2	W9	2000 1600	-
295	6	Y4	W7	3200 2600 2000 1600 1000	-
296	6	Y6	W1	1000	-
297	6	W3	W6	3200 1600	-
298	6	W4	V9	3200 2600 1600 1000	-
299	6	V1	W5	2000 1600 1000	VREF
300	6	U2	V7	2000 1600 1000	-
301	6	U1	V6	3200 2600 1600 1000	VREF
302	7	U4	U9	3200 2600 2000 1600 1000	-
303	7	U5	U7	3200 2600 1600 1000	VREF
304	7	U6	U3	2000 1600 1000	-
305	7	T6	T3	2000 1600 1000	VREF
306	7	T4	T9	3200 2600 1600 1000	-
307	7	R1	T5	3200 1600	-
308	7	T10	R6	1000	-
309	7	R5	R2	3200 2600 2000 1600 1000	-
310	7	P5	P1	2000 1600 1000	VREF