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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	393216
Number of I/O	404
Number of Gates	1569178
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000e-8bg560c

Virtex-E Ordering Information

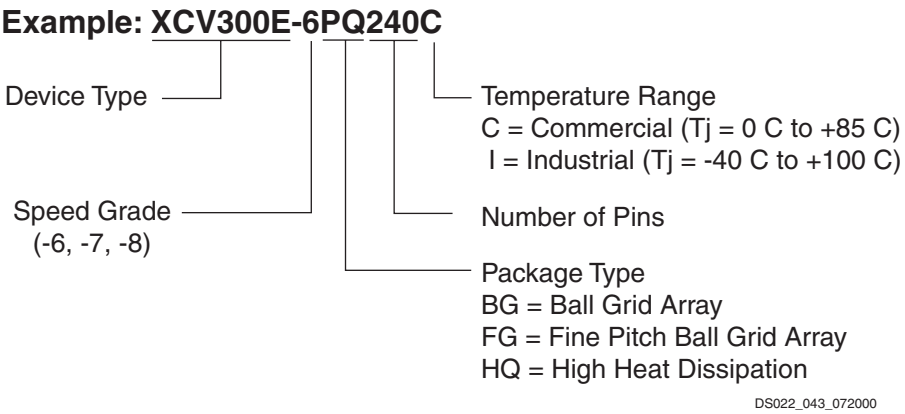


Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/7/99	1.0	Initial Xilinx release.
1/10/00	1.1	Re-released with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and SelectI/O information.
1/28/00	1.2	Added Delay Measurement Methodology table, updated SelectI/O section, Figures 30, 54, & 55, text explaining Table 5, T_{BYP} values, buffered Hex Line info, p. 8, I/O Timing Measurement notes, notes for Tables 15, 16, and corrected F1156 pinout table footnote references.
2/29/00	1.3	Updated pinout tables, V_{CC} page 20, and corrected Figure 20.
5/23/00	1.4	Correction to table on p. 22.
7/10/00	1.5	• Numerous minor edits. • Data sheet upgraded to Preliminary. • Preview -8 numbers added to **Virtex-E Electrical Characteristics** tables.
8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.
9/20/00	1.7	• Min values added to **Virtex-E Electrical Characteristics** tables. • XCV2600E and XCV3200E numbers added to **Virtex-E Electrical Characteristics** tables (Module 3). • Corrected user I/O count for XCV100E device in Table 1 (Module 1). • Changed several pins to “No Connect in the XCV100E“ and removed duplicate V_{CCINT} pins in Table ~ (Module 4). • Changed pin J10 to “No connect in XCV600E” in Table 74 (Module 4). • Changed pin J30 to “VREF option only in the XCV600E” in Table 74 (Module 4). • Corrected pair 18 in Table 75 (Module 4) to be “AO in the XCV1000E, XCV1600E“.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

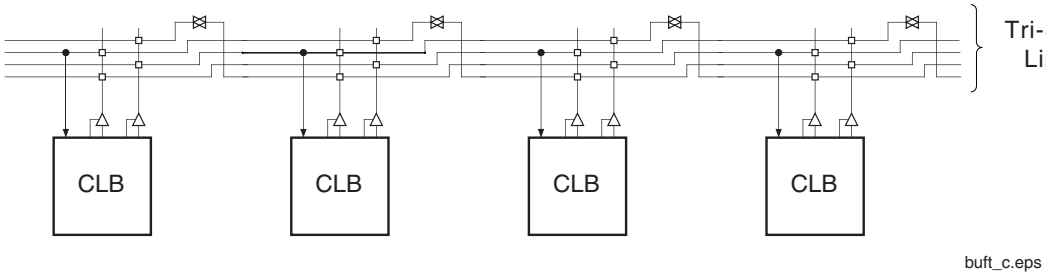


Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

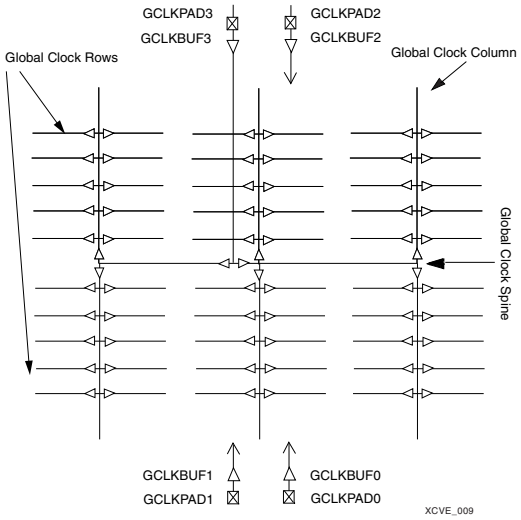


Figure 9: **Global Clock Distribution Network**

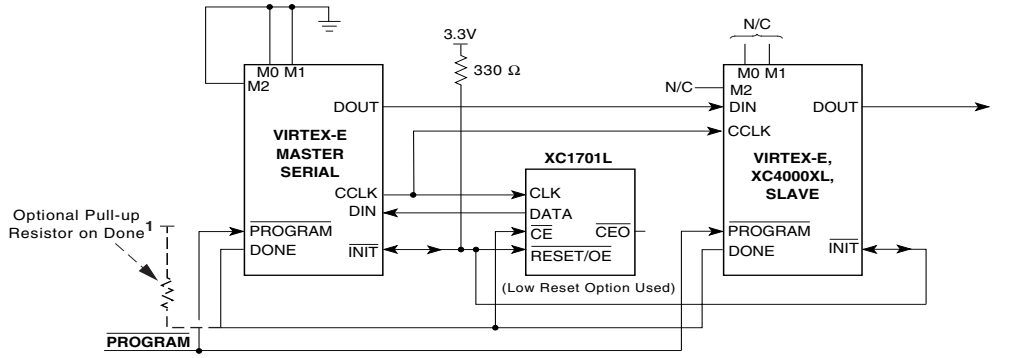
Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.



Note 1: If none of the Virtex FPGAs have been selected to drive DONE, an external pull-up resistor of 330 Ω should be added to the common DONE line. (For Spartan-XL devices, add a 4.7K Ω pull-up resistor.) This pull-up is not needed if the DriveDONE attribute is set. If used, DriveDONE should be selected only for the last device in the configuration chain.

XCVE_ds_013_050103

Figure 13: **Master/Slave Serial Mode Circuit Diagram**

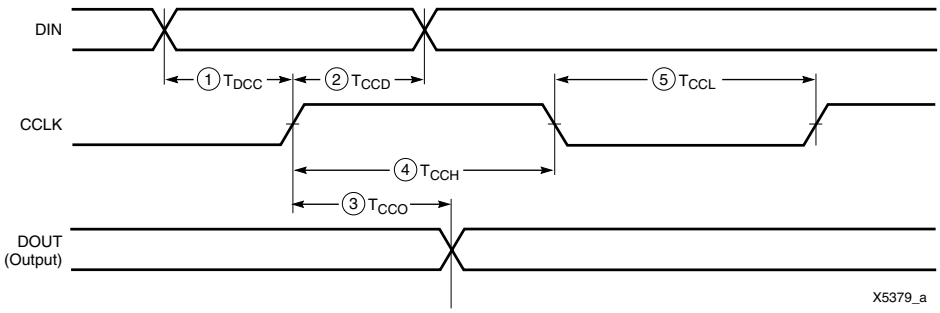


Figure 14: **Slave-Serial Mode Programming Switching Characteristics**

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

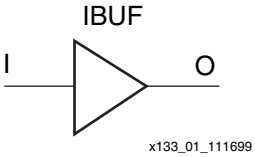


Figure 37: **Input Buffer (IBUF) Symbols**

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF}, the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 49. DC voltage specifications appear in Table 28.

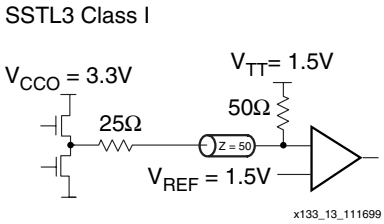


Figure 49: **Terminated SSTL3 Class I**

Table 28: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL} = V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.6	1.9	-	-
V_{OL} = V_{REF} – 0.6	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 50. DC voltage specifications appear in Table 29.

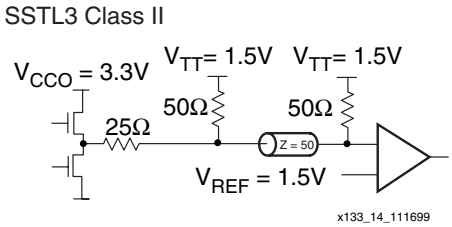


Figure 50: **Terminated SSTL3 Class II**

Table 29: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF} = 0.45 × V_{CCO}	1.3	1.5	1.7
V_{TT} = V_{REF}	1.3	1.5	1.7
V_{IH} = V_{REF} + 0.2	1.5	1.7	3.9(1)
V_{IL}= V_{REF} – 0.2	–0.3(2)	1.3	1.5
V_{OH} = V_{REF} + 0.8	2.1	-	-
V_{OL}= V_{REF} – 0.8	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 51. DC voltage specifications appear in Table 30.

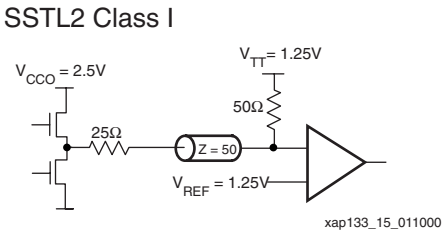


Figure 51: **Terminated SSTL2 Class I**

Table 30: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF} = 0.5 × V_{CCO}	1.15	1.25	1.35
V_{TT} = V_{REF} + N(1)	1.11	1.25	1.39
V_{IH} = V_{REF} + 0.18	1.33	1.43	3.0(2)
V_{IL} = V_{REF} – 0.18	–0.3(3)	1.07	1.17
V_{OH} = V_{REF} + 0.61	1.76	-	-
V_{OL}= V_{REF} – 0.61	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Table 44: **Bidirectional I/O Library Macros**

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

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8/1/00	1.6	• Reformatted entire document to follow new style guidelines. • Changed speed grade values in tables on pages 35-37.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade				
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.20	–0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2	0.10	+0.09	+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18	0.10	+0.7	+0.7	+0.7	ns
	T_{OLVDS}	LVDS	–0.39	–1.2	–1.2	–1.2	ns
	$T_{OLVPECL}$	LVPECL	–0.20	–0.41	–0.41	–0.41	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.41	–0.41	–0.41	ns
	T_{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T_{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.51	–0.51	–0.51	ns
	T_{OHSTL_III}	HSTL III	–0.10	–0.91	–0.91	–0.91	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.01	–1.01	–1.01	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.51	–0.51	–0.51	ns
	T_{OSSTL2_II}	SSTL2 II	–0.20	–0.91	–0.91	–0.91	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.51	–0.51	–0.51	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.01	–1.01	–1.01	ns
	T_{OCTT}	CTT	0.0	–0.61	–0.61	–0.61	ns
	T_{OAGP}	AGP	–0.1	–0.91	–0.91	–0.91	ns

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
GCLK IOB and Buffer						
Global Clock PAD to output.	T_{GPIO}	0.38	0.7	0.7	0.7	ns, max
Global Clock Buffer I input to O output	T_{GIO}	0.11	0.20	0.45	0.50	ns, max

I/O Standard Global Clock Input Adjustments

Description	Symbol[1]	Standard	Speed Grade				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific global clock input delay adjustments	$T_{GPLVTTL}$	LVTTL	0.0	0.0	0.0	0.0	ns, max
	$T_{GPLVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns, max
	$T_{GPLVCMOS18}$	LVCMOS18	0.12	0.20	0.20	0.20	ns, max
	T_{GLVDS}	LVDS	0.23	0.38	0.38	0.38	ns, max
	$T_{GLVPECL}$	LVPECL	0.23	0.38	0.38	0.38	ns, max
	$T_{GPPCI33\_3}$	PCI, 33 MHz, 3.3 V	–0.05	0.08	0.08	0.08	ns, max
	$T_{GPPCI66\_3}$	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns, max
	T_{GPGTL}	GTL	0.20	0.37	0.37	0.37	ns, max
	T_{GPGTLP}	GTL+	0.20	0.37	0.37	0.37	ns, max
	T_{GPHSTL}	HSTL	0.18	0.27	0.27	0.27	ns, max
	$T_{GPSSTL2}$	SSTL2	0.21	0.27	0.27	0.27	ns, max
	$T_{GPSSTL3}$	SSTL3	0.18	0.27	0.27	0.27	ns, max
	T_{GPCTT}	CTT	0.22	0.33	0.33	0.33	ns, max
	T_{GPAGP}	AGP	0.21	0.27	0.27	0.27	ns, max

Notes:
1. Input timing for GPLVTTL is measured at 1.4 V. For other I/O standards, see Table 4.

Table 5: **CS144 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
18	5	N8	M6	NA	IO_LVDS_DLL
19	5	K6	N5	√	-
20	5	K5	N4	√	VREF
21	5	N3	M3	√	-
22	6	K3	L1	√	-
23	6	J2	J3	1	VREF
24	6	H3	H4	√	-
25	6	H1	H2	1	VREF
26	7	F2	G1	NA	-
27	7	E1	F4	1	VREF
28	7	E3	E2	√	-
29	7	D2	D1	1	VREF

Note 1: AO in the XCV50E

PQ240 Plastic Quad Flat-Pack Packages

XCV50E, XCV100E, XCV200E, XCV300E and XCV400E devices in PQ240 Plastic Flat-pack packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 6, see Table 7 for Differential Pair information.

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P238	IO	0
P237	IO_L0N_Y	0
P236[2]	IO_VREF_L0P_Y	0
P235	IO_L1N_YY	0
P234	IO_L1P_YY	0
P231	IO_VREF	0
P230	IO	0
P229[1]	IO_VREF_L2N_YY	0
P228	IO_L2P_YY	0
P224	IO_L3N_YY	0
P223	IO_L3P_YY	0

Table 6: **PQ240 — XCV50E, XCV100E, XCV200E, XCV300E, XCV400E**

Pin #	Pin Description	Bank
P222	IO	0
P221	IO_L4N_Y	0
P220	IO_L4P_Y	0
P218	IO_VREF_L5N_Y	0
P217	IO_L5P_Y	0
P216[3]	IO_VREF	0
P215	IO_LVDS_DLL_L6N	0
P213	GCK3	0
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208[3]	IO_VREF	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201	IO	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P195	IO_L10N_YY	1
P194[1]	IO_VREF_L10P_YY	1
P193	IO	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187[2]	IO_VREF_L13N_Y	1
P186	IO_L13P_Y	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P175[2]	IO_VREF	2
P174	IO_L16P_Y	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P138	IO_D5_L26N_YY	3
P137	VCCINT	NA
P136	VCCO	3
P135	GND	NA
P134	IO_D6_L27P_Y	3
P133	IO_VREF_L27N_Y	3
P132	IO_VREF	3
P131	IO_L28P_Y	3
P130	IO_VREF_L28N_Y	3
P129	GND	NA
P128	IO_L29P_Y	3
P127	IO_L29N_Y	3
P126	IO_VREF_L30P_Y	3
P125	IO_L30N_Y	3
P124	IO_D7_L31P_YY	3
P123	IO_INIT_L31N_YY	3
P122	PROGRAM	NA
P121	VCCO	3
P120	DONE	3
P119	GND	NA
P118	IO_L32P_YY	4
P117	IO_L32N_YY	4
P116	VCCO	4
P115	IO_VREF	4
P114	IO_L33P_YY	4
P113	IO_L33N_YY	4
P112	GND	NA
P111	IO_VREF_L34P_YY	4
P110	IO_L34N_YY	4
P109	IO_VREF	4
P108	IO_VREF_L35P_YY	4
P107	IO_L35N_YY	4
P106	GND	NA
P105	VCCO	4
P104	VCCINT	NA
P103	IO_L36P_YY	4

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P102	IO_L36N_YY	4
P101[1]	IO_VREF	4
P100	IO_L37P_Y	4
P99	IO_L37N_Y	4
P98	GND	NA
P97	IO_VREF_L38P_Y	4
P96	IO_L38N_Y	4
P95	IO_L39P	4
P94	IO_VREF_L39N	4
P93	IO_LVDS_DLL_L40P	4
P92	GCK0	4
P91	GND	NA
P90	VCCO	4
P89	GCK1	5
P88	VCCINT	NA
P87	IO_LVDS_DLL_L40N	5
P86	IO_VREF	5
P85	VCCO	5
P84	IO_VREF_L41P	5
P83	GND	NA
P82	IO_L41N	5
P81	IO	5
P80[1]	IO_VREF	5
P79	IO_L42P_YY	5
P78	IO_L42N_YY	5
P77	VCCINT	NA
P76	VCCO	5
P75	GND	NA
P74	IO_L43P_YY	5
P73	IO_VREF_L43N_YY	5
P72	IO_VREF	5
P71	IO_L44P_YY	5
P70	IO_VREF_L44N_YY	5
P69	GND	NA
P68	IO_L45P_YY	5
P67	IO_L45N_YY	5

HQ240 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 9: **HQ240 Differential Pin Pair Summary XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	P92	P93	NA	IO _DLL_L40P
1	5	P89	P87	NA	IO _DLL_L40N
2	1	P210	P209	NA	IO _DLL_L6P
3	0	P213	P215	NA	IO _DLL_L6N
IO LVDS Total Pairs: 64, Asynchronous Output Pairs: 53					
0	0	P236	P237	NA	VREF
1	0	P234	P235	√	-
2	0	P228	P229	√	VREF
3	0	P223	P224	√	-
4	0	P220	P221	√	-
5	0	P217	P218	√	VREF
6	1	P209	P215	NA	IO_LVDS_DLL
7	1	P205	P206	√	VREF
8	1	P202	P203	√	-
9	1	P199	P200	√	-
10	1	P194	P195	√	VREF
11	1	P191	P192	√	VREF
12	1	P188	P189	√	-
13	1	P186	P187	NA	VREF
14	1	P184	P185	√	CS
15	2	P178	P177	√	DIN, D0

Table 9: **HQ240 Differential Pin Pair Summary XCV600E, XCV1000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
16	2	P174	P173	√	-
17	2	P171	P170	√	VREF
18	2	P168	P167	√	D1
19	2	P163	P162	√	D2
20	2	P160	P159	√	-
21	2	P157	P156	√	D3
22	2	P155	P154	1	VREF
23	2	P153	P152	√	-
24	3	P145	P144	√	D4, VREF
25	3	P142	P141	√	-
26	3	P139	P138	√	D5
27	3	P134	P133	√	VREF
28	3	P131	P130	√	VREF
29	3	P128	P127	√	-
30	3	P126	P125	1	VREF
31	3	P124	P123	√	INIT
32	4	P118	P117	√	-
33	4	P114	P113	√	-
34	4	P111	P110	√	VREF
35	4	P108	P107	√	VREF
36	4	P103	P102	√	-
37	4	P100	P99	√	-
38	4	P97	P96	√	VREF
39	4	P95	P94	NA	VREF
40	5	P93	P87	NA	IO_LVDS_DLL
41	5	P84	P82	NA	VREF
42	5	P79	P78	√	-
43	5	P74	P73	√	VREF
44	5	P71	P70	√	VREF
45	5	P68	P67	√	-
46	5	P66	P65	NA	VREF
47	5	P64	P63	√	-

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO_L132P_Y	G28
7	IO_L133N	E31
7	IO_L133P	E30
7	IO_L134N_Y	F29
7	IO_VREF_L134P_Y	F28
7	IO_L135N_Y	D31
7	IO_L135P_Y	D30
7	IO_L136N	E29
7	IO_L136P	E28
2	CCLK	D4
3	DONE	AH4
NA	DXN	AH27
NA	DXP	AK29
NA	M0	AH28
NA	M1	AH29
NA	M2	AJ28
NA	PROGRAM	AH3
NA	TCK	D28
NA	TDI	B3
2	TDO	C4
NA	TMS	D29
NA	VCCINT	A10
NA	VCCINT	A17
NA	VCCINT	B23
NA	VCCINT	B26
NA	VCCINT	C7
NA	VCCINT	C14
NA	VCCINT	C19
NA	VCCINT	F1
NA	VCCINT	F30
NA	VCCINT	K3
NA	VCCINT	K29
NA	VCCINT	N2
NA	VCCINT	N29

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	VCCINT	T1
NA	VCCINT	T29
NA	VCCINT	W2
NA	VCCINT	W31
NA	VCCINT	AB2
NA	VCCINT	AB30
NA	VCCINT	AE29
NA	VCCINT	AF1
NA	VCCINT	AH8
NA	VCCINT	AH24
NA	VCCINT	AJ10
NA	VCCINT	AJ16
NA	VCCINT	AK22
NA	VCCINT	AK13
NA	VCCINT	AK19
0	VCCO	A21
0	VCCO	C29
0	VCCO	D21
1	VCCO	A1
1	VCCO	A11
1	VCCO	D11
2	VCCO	C3
2	VCCO	L4
2	VCCO	L1
3	VCCO	AA1
3	VCCO	AA4
3	VCCO	AJ3
4	VCCO	AH11
4	VCCO	AL1
4	VCCO	AL11
5	VCCO	AH21
5	VCCO	AL21
5	VCCO	AJ29
6	VCCO	AA28
6	VCCO	AA31

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
1	IO_L43N_Y	C5	
1	IO_VREF_L43P_Y	E7	3
1	IO_WRITE_L44N_YY	D6	
1	IO_CS_L44P_YY	A2	
2	IO	D3	
2	IO	F3	
2	IO	G1	
2	IO	J2	
2	IO_DOUT_BUSY_L45P_YY	D4	
2	IO_DIN_D0_L45N_YY	E4	
2	IO_L46P_Y	F5	
2	IO_VREF_L46N_Y	B3	3
2	IO_L47P_Y	F4	
2	IO_L47N_Y	C1	
2	IO_VREF_L48P_Y	G5	
2	IO_L48N_Y	E3	
2	IO_L49P_Y	D2	
2	IO_L49N_Y	G4	
2	IO_L50P_Y	H5	
2	IO_L50N_Y	E2	
2	IO_VREF_L51P_YY	H4	
2	IO_L51N_YY	G3	
2	IO_L52P_Y	J5	
2	IO_VREF_L52N_Y	F1	1
2	IO_L53P_Y	J4	
2	IO_L53N_Y	H3	
2	IO_VREF_L54P_Y	K5	4
2	IO_L54N_Y	H2	
2	IO_L55P_Y	J3	
2	IO_L55N_Y	K4	
2	IO_VREF_L56P_YY	L5	
2	IO_D1_L56N_YY	K3	
2	IO_D2_L57P_YY	L4	
2	IO_L57N_YY	K2	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	IO_L58P_Y	M5	
2	IO_L58N_Y	L3	
2	IO_L59P_Y	L1	
2	IO_L59N_Y	M4	
2	IO_VREF_L60P_Y	N5	3
2	IO_L60N_Y	M2	
2	IO_L61P_Y	N4	
2	IO_L61N_Y	N3	
2	IO_L62P_Y	N2	
2	IO_L62N_Y	P5	
2	IO_VREF_L63P_YY	P4	
2	IO_D3_L63N_YY	P3	
2	IO_L64P_Y	P2	
2	IO_L64N_Y	R5	
2	IO_L65P_Y	R4	
2	IO_L65N_Y	R3	
2	IO_VREF_L66P_Y	R1	
2	IO_L66N_Y	T4	
2	IO_L67P_Y	T5	
2	IO_VREF_L67N_Y	T3	2
2	IO_L68P_YY	T2	
2	IO_L68N_YY	U3	
3	IO	AE3	
3	IO	AF3	
3	IO	AH3	
3	IO	AK3	
3	IO_VREF_L69P_Y	U1	2
3	IO_L69N_Y	U2	
3	IO_L70P_Y	V2	
3	IO_VREF_L70N_Y	V4	
3	IO_L71P_Y	V5	
3	IO_L71N_Y	V3	
3	IO_L72P_Y	W1	
3	IO_L72N_Y	W3	

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
3	IO_L50N_YY	P19
3	IO_L51P_YY	P18
3	IO_D5_L51N_YY	R21
3	IO_D6_L52P_Y	T22
3	IO_VREF_L52N_Y	R19
3	IO_L53P_Y	U22
3	IO_L53N_Y	R18
3	IO_L54P_YY	T21
3	IO_L54N_YY	V22
3	IO_L55P_YY	T20
3	IO_VREF_L55N_YY	U21
3	IO_L56P_YY	W22
3	IO_L56N_YY	T18
3	IO_L57P_YY	U19
3	IO_VREF_L57N_YY	U20
3	IO_L58P_YY	W21
3	IO_L58N_YY	AA22
3	IO_D7_L59P_YY	Y21
3	IO_INIT_L59N_YY	V19
3	IO	M22
4	GCK0	W12
4	IO	W14
4	IO	Y13
4	IO	Y17
4	IO	AA16[1]
4	IO	AA19
4	IO	AB12[1]
4	IO	AB17
4	IO	AB21[1]
4	IO_L60P_YY	W18
4	IO_L60N_YY	AA20
4	IO_L61P	Y18
4	IO_L61N	V17
4	IO_VREF_L62P_YY	AB20
4	IO_L62N_YY	W17
4	IO_L63P	AA18

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
4	IO_L63N	V16
4	IO_VREF_L64P_YY	AB19
4	IO_L64N_YY	AB18
4	IO_L65P_Y	W16
4	IO_L65N_Y	AA17
4	IO_L66P_Y	Y16
4	IO_L66N_Y	V15
4	IO_VREF_L67P_YY	AB16
4	IO_L67N_YY	Y15
4	IO_L68P_YY	AA15
4	IO_L68N_YY	AB15
4	IO_L69P_Y	W15
4	IO_L69N_Y	Y14
4	IO_L70P_Y	V14
4	IO_L70N_Y	AA14
4	IO_L71P	AB14
4	IO_L71N	V13
4	IO_VREF_L72P_YY	AA13
4	IO_L72N_YY	AB13
4	IO_L73P_Y	W13
4	IO_L73N_Y	AA12
4	IO_L74P_Y	Y12
4	IO_L74N_Y	V12
4	IO_LVDS_DLL_L75P	U12
5	IO	U11[1]
5	IO	V8
5	IO	W5
5	IO	AA3[1]
5	IO	AA9
5	IO	AA10
5	IO	AB4
5	IO	AB7[1]
5	IO	AB8
5	GCK1	Y11
5	IO_LVDS_DLL_L75N	AA11
5	IO_L76P_Y	AB11

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	M9
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	L9
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	J14
NA	GND	J13
NA	GND	J12
NA	GND	J11
NA	GND	J10
NA	GND	J9
NA	GND	C20
NA	GND	C3
NA	GND	B21
NA	GND	B2
NA	GND	A22
NA	GND	A1

Note 1: NC in the XCV200E device.

FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	W12	U12	NA	IO_DLL_L75P
1	5	Y11	AA11	NA	IO_DLL_L75N
2	1	A11	D11	NA	IO_DLL_L13P
3	0	C11	B11	NA	IO_DLL_L13N
IO LVDS Total Pairs: 119, Asynchronous Output Pairs: 69					
0	0	B3	D5	NA	-
1	0	E6	B4	√	VREF
2	0	E7	A4	NA	-
3	0	D6	C6	√	VREF
4	0	B6	A5	1	-
5	0	C7	D7	1	-
6	0	B7	E8	√	VREF
7	0	E9	A7	√	-
8	0	B8	C8	1	-
9	0	A8	D9	1	-
10	0	E10	C9	NA	-
11	0	C10	A9	√	VREF
12	0	B10	F11	2	-
13	1	D11	B11	NA	IO_LVDS_DLL
14	1	D12	C12	2	-
15	1	A13	B12	2	-
16	1	B13	E12	√	VREF
17	1	D13	C13	√	-

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	GND	P14
NA	GND	P13
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Notes:
1. NC in the XCV400E.
2. V_{REF} or I/O option only in the XCV600E; otherwise, I/O option only.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
4	IO_L147N_YY	AW7
4	IO_L148P_Y	AY7
4	IO_L148N_Y	BB8
4	IO_L149P_Y	BA9
4	IO_L149N_Y	AV8
4	IO_L150P_YY	AW8
4	IO_L150N_YY	BA10
4	IO_VREF_L151P_YY	BB10
4	IO_L151N_YY	AY8
4	IO_L152P_Y	AV9
4	IO_L152N_Y	BA11
4	IO_VREF_L153P_Y	BB11[2]
4	IO_L153N_Y	AW9
4	IO_L154P_YY	AY9
4	IO_L154N_YY	BA12
4	IO_VREF_L155P_YY	BB12
4	IO_L155N_YY	AV10
4	IO_L156P_Y	BA13
4	IO_L156N_Y	AW10
4	IO_L157P_Y	BB13
4	IO_L157N_Y	AY10
4	IO_VREF_L158P_YY	AV11
4	IO_L158N_YY	BA14
4	IO_L159P_YY	AW11
4	IO_L159N_YY	BB14
4	IO_L160P_Y	AV12
4	IO_L160N_Y	BA15
4	IO_L161P_Y	AW12
4	IO_L161N_Y	AY15
4	IO_L162P_Y	AW13
4	IO_L162N_Y	BB15
4	IO_L163P_Y	AV14
4	IO_L163N_Y	BA16
4	IO_L164P_YY	AW14
4	IO_L164N_YY	AY16
4	IO_VREF_L165P_YY	BB16
4	IO_L165N_YY	AV15
4	IO_L166P_Y	AY17
4	IO_L166N_Y	AW15
4	IO_L167P_Y	BB17
4	IO_L167N_Y	AU16
4	IO_L168P_YY	AV16
4	IO_L168N_YY	AY18
4	IO_VREF_L169P_YY	AW16
4	IO_L169N_YY	BA18
4	IO_L170P_Y	BB19
4	IO_L170N_Y	AW17
4	IO_L171P_Y	AY19
4	IO_L171N_Y	AV18
4	IO_L172P_YY	AW18
4	IO_L172N_YY	BB20
4	IO_VREF_L173P_YY	AY20
4	IO_L173N_YY	AV19
4	IO_L174P_Y	BB21
4	IO_L174N_Y	AW19
4	IO_VREF_L175P_Y	AY21[1]
4	IO_L175N_Y	AV20
4	IO_LVDS_DLL_L176P	AW20
5	GCK1	AY22
5	IO	AV24
5	IO	AV34
5	IO	AW27
5	IO	AW36
5	IO	AY23
5	IO	AY31
5	IO	AY33
5	IO	BA26
5	IO	BA29
5	IO	BA33
5	IO	BB25
5	IO_LVDS_DLL_L176N	AW21
5	IO_L177P_Y	BB22
5	IO_VREF_L177N_Y	AW22[1]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO_L154N	AG23
4	IO_L155P_YY	AF22
4	IO_L155N_YY	AE22
4	IO_VREF_L156P_YY	AJ22
4	IO_L156N_YY	AG22
4	IO_L157P	AK24[4]
4	IO_L157N	AD20[3]
4	IO_L158P_YY	AA19
4	IO_L158N_YY	AF21
4	IO_L159P	AH22[4]
4	IO_VREF_L159N	AA18
4	IO_L160P	AG21
4	IO_L160N	AK23
4	IO_L161P_YY	AH21[4]
4	IO_L161N_YY	AD19[4]
4	IO_L162P	AE20
4	IO_L162N	AJ21
4	IO_L163P	AG20
4	IO_L163N	AF20
4	IO_L164P	AC18[4]
4	IO_L164N	AF19[4]
4	IO_L165P_YY	AJ20
4	IO_L165N_YY	AE19
4	IO_VREF_L166P_YY	AK22[1]
4	IO_L166N_YY	AH20
4	IO_L167P	AG19
4	IO_L167N	AB17
4	IO_L168P	AJ19
4	IO_L168N	AD17
4	IO_L169P_YY	AA16
4	IO_L169N_YY	AA17
4	IO_VREF_L170P_YY	AK21
4	IO_L170N_YY	AB16
4	IO_L171P	AG18
4	IO_L171N	AK20
4	IO_L172P	AK19
4	IO_L172N	AD16

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO_L173P_YY	AE16
4	IO_L173N_YY	AE17
4	IO_VREF_L174P_YY	AG17
4	IO_L174N_YY	AJ17
4	IO_L175P	AD15[4]
4	IO_L175N	AH17[3]
4	IO_VREF_L176P_YY	AG16[2]
4	IO_L176N_YY	AK17
4	IO_LVDS_DLL_L177P	AF16
5	GCK1	AK16
5	IO	AA11[4]
5	IO	AA14[4]
5	IO	AD14[4]
5	IO	AE7[5]
5	IO	AE8[5]
5	IO	AE10[4]
5	IO	AF6[4]
5	IO	AF10[4]
5	IO	AG9[4]
5	IO	AG12[4]
5	IO	AG14[5]
5	IO	AH8[4]
5	IO	AK6[5]
5	IO	AK14[5]
5	IO	AJ13[4]
5	IO	AJ15[4]
5	IO_LVDS_DLL_L177N	AH16
5	IO_L178P_YY	AC15[4]
5	IO_VREF_L178N_YY	AG15[2,3]
5	IO_L179P_YY	AB15
5	IO_L179N_YY	AF15
5	IO_L180P_YY	AA15
5	IO_VREF_L180N_YY	AF14
5	IO_L181P_YY	AH15
5	IO_L181N_YY	AK15
5	IO_L182P	AB14

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_2	T23
NA	VCCO_2	T24
NA	VCCO_2	R23
NA	VCCO_2	R24
NA	VCCO_2	P23
NA	VCCO_2	P24
NA	VCCO_2	P32
NA	VCCO_2	N23
NA	VCCO_3	V23
NA	VCCO_3	V24
NA	VCCO_3	Y23
NA	VCCO_3	Y24
NA	VCCO_3	W23
NA	VCCO_3	W24
NA	VCCO_3	AJ34
NA	VCCO_3	AE30
NA	VCCO_3	AC24
NA	VCCO_3	AB23
NA	VCCO_3	AB24
NA	VCCO_3	AA23
NA	VCCO_3	AA24
NA	VCCO_3	AA32
NA	VCCO_4	AD18
NA	VCCO_4	AC18
NA	VCCO_4	AC19
NA	VCCO_4	AC20
NA	VCCO_4	AC21
NA	VCCO_4	AC22
NA	VCCO_4	AP29
NA	VCCO_4	AM21
NA	VCCO_4	AK25
NA	VCCO_4	AD19
NA	VCCO_4	AD20
NA	VCCO_4	AD21

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	VCCO_4	AD22
NA	VCCO_4	AD23
NA	VCCO_5	AC17
NA	VCCO_5	AD17
NA	VCCO_5	AC13
NA	VCCO_5	AC14
NA	VCCO_5	AC15
NA	VCCO_5	AC16
NA	VCCO_5	AP6
NA	VCCO_5	AM14
NA	VCCO_5	AK10
NA	VCCO_5	AD12
NA	VCCO_5	AD13
NA	VCCO_5	AD14
NA	VCCO_5	AD15
NA	VCCO_5	AD16
NA	VCCO_6	V11
NA	VCCO_6	V12
NA	VCCO_6	Y11
NA	VCCO_6	Y12
NA	VCCO_6	W11
NA	VCCO_6	W12
NA	VCCO_6	AJ1
NA	VCCO_6	AE5
NA	VCCO_6	AC11
NA	VCCO_6	AB11
NA	VCCO_6	AB12
NA	VCCO_6	AA3
NA	VCCO_6	AA11
NA	VCCO_6	AA12
NA	VCCO_7	U11
NA	VCCO_7	U12
NA	VCCO_7	N12
NA	VCCO_7	M11

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	R15
NA	GND	P15
NA	GND	L3
NA	GND	G7
NA	GND	E30
NA	GND	C24
NA	GND	B34
NA	GND	AP32
NA	GND	AM1
NA	GND	AM34
NA	GND	AJ29
NA	GND	AF9
NA	GND	AA17
NA	GND	Y17
NA	GND	W16
NA	GND	V16
NA	GND	U17
NA	GND	T17
NA	GND	R16
NA	GND	P16
NA	GND	L32
NA	GND	G28
NA	GND	D4
NA	GND	C32
NA	GND	A1
NA	GND	AP33
NA	GND	AM2
NA	GND	AL4
NA	GND	AH1
NA	GND	AF26
NA	GND	AA18
NA	GND	Y18
NA	GND	W17
NA	GND	V17

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	U18
NA	GND	T18
NA	GND	R17
NA	GND	P17
NA	GND	J9
NA	GND	G34
NA	GND	D31
NA	GND	C33
NA	GND	A2
NA	GND	AB17
NA	GND	AB18
NA	GND	N17
NA	GND	N18
NA	GND	U13
NA	GND	V13
NA	GND	U22
NA	GND	V22

Notes:

1. V_{REF} or I/O option only in the XCV1600E, XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E, XCV2600E, and XCV3200E; otherwise, I/O option only.
3. No Connect in the XCV1000E, XCV1600E.
4. No Connect in the XCV1000E.
5. I/O in the XCV1000E.