AMD Xilinx - XCV1000E-8FG860C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	6144
Number of Logic Elements/Cells	27648
Total RAM Bits	393216
Number of I/O	660
Number of Gates	1569178
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	860-BGA Exposed Pad
Supplier Device Package	860-FBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv1000e-8fg860c

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1: **Virtex-E Field-Programmable Gate Array Family Members**

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	196	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 μm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 μm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing

For in-circuit debugging, an optional download and read-back cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary Scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3 V or 2.5 V. At 3.3 V the pins operate as LVTTL, and at 2.5 V they operate as LVCMOS. All affected pins fall in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary Scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the Boundary Scan port is always available, independent of the mode selection. Selecting the Boundary Scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

Table 8: **Configuration Codes**

Configuration Mode	M2[1]	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups[1]
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary Scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary Scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Notes:

1. M2 is sampled continuously from power up until the end of the configuration. Toggling M2 while INIT is being held externally Low can cause the configuration pull-up settings to change.

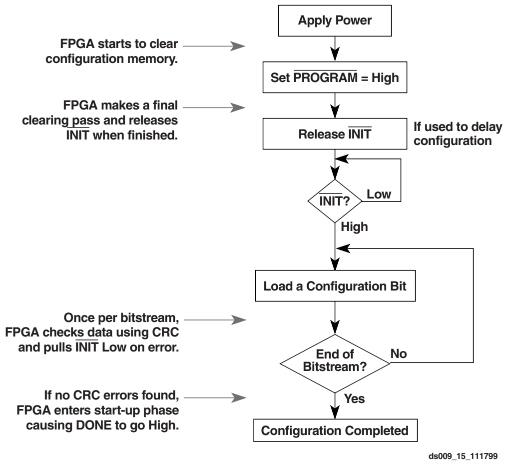
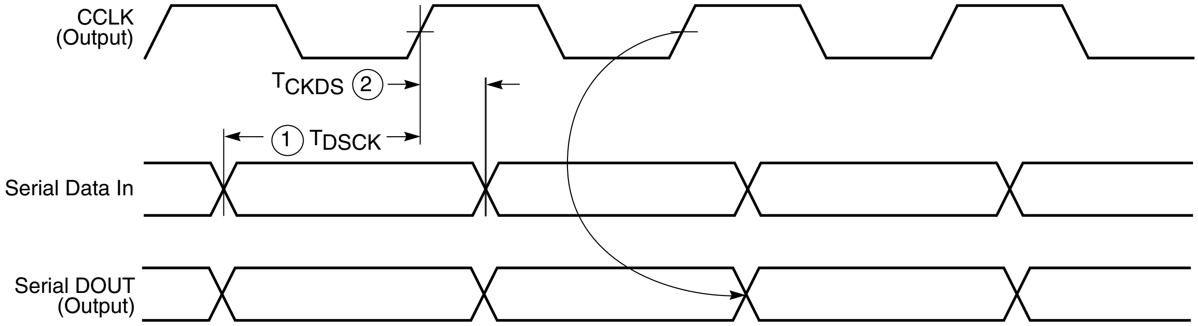


Figure 15: **Serial Configuration Flowchart**

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16.



DS022_44_071201

Figure 16: **Master-Serial Mode Programming Switching Characteristics**

At power-up, V_{CC} must rise from 1.0 V to V_{CC} Min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 17.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or de-asserted. Otherwise, an abort is initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 27 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

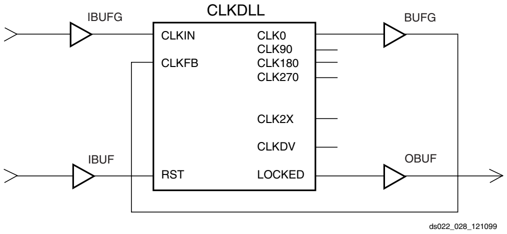


Figure 27: **Standard DLL Implementation**

Board Level Deskew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 28 can be used to deskew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

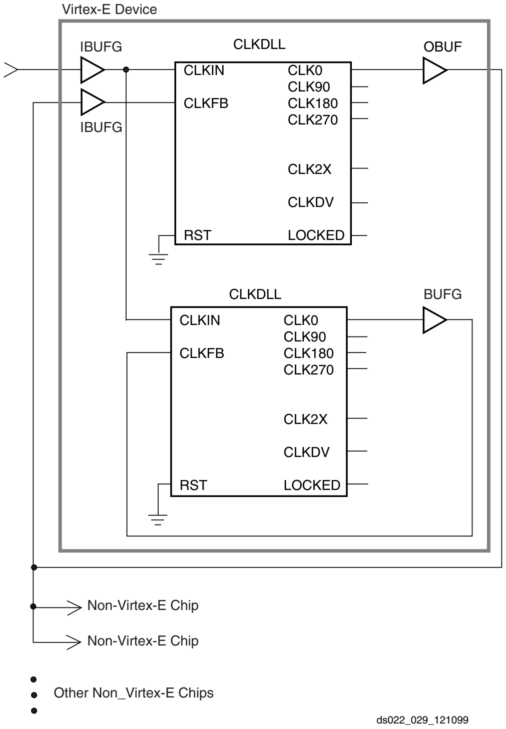


Figure 28: **DLL Deskew of Board Level Clock**

Board-level deskew is not required for low-fanout clock networks. It is recommended for systems that have fanout limitations on the clock network, or if the clock distribution chip cannot handle the load.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

The dll_mirror_1 files in the xapp132.zip file show the VHDL and Verilog implementation of this circuit.

Deskew of Clock and Its 2x Multiple

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with a zero ns skew between registers on the same chip. Alternatively, a clock divider circuit can be implemented using similar connections.

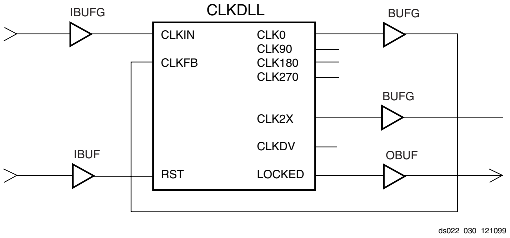


Figure 29: **DLL Deskew of Clock and 2x Multiple**

Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels in Table 2. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.

Table 2: **IOB Input Switching Characteristics**

			Speed Grade(1)				
Description(2)	**Symbol**	**Device**	**Min**	**-8**	**-7**	**-6**	**Units**
Propagation Delays							
Pad to I output, no delay	T_{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T_{IOPID}	XCV50E	0.51	1.0	1.0	1.0	ns, max
		XCV100E	0.51	1.0	1.0	1.0	ns, max
		XCV200E	0.51	1.0	1.0	1.0	ns, max
		XCV300E	0.51	1.0	1.0	1.0	ns, max
		XCV400E	0.51	1.0	1.0	1.0	ns, max
		XCV600E	0.51	1.0	1.0	1.0	ns, max
		XCV1000E	0.55	1.1	1.1	1.1	ns, max
		XCV1600E	0.55	1.1	1.1	1.1	ns, max
		XCV2000E	0.55	1.1	1.1	1.1	ns, max
		XCV2600E	0.55	1.1	1.1	1.1	ns, max
		XCV3200E	0.55	1.1	1.1	1.1	ns, max
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.8	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XCV50E	1.31	2.9	3.0	3.1	ns, max
		XCV100E	1.31	2.9	3.0	3.1	ns, max
		XCV200E	1.39	3.1	3.2	3.3	ns, max
		XCV300E	1.39	3.1	3.2	3.3	ns, max
		XCV400E	1.43	3.2	3.3	3.4	ns, max
		XCV600E	1.55	3.5	3.6	3.7	ns, max
		XCV1000E	1.55	3.5	3.6	3.7	ns, max
		XCV1600E	1.59	3.6	3.7	3.8	ns, max
		XCV2000E	1.59	3.6	3.7	3.8	ns, max
		XCV2600E	1.59	3.6	3.7	3.8	ns, max
		XCV3200E	1.59	3.6	3.7	3.8	ns, max

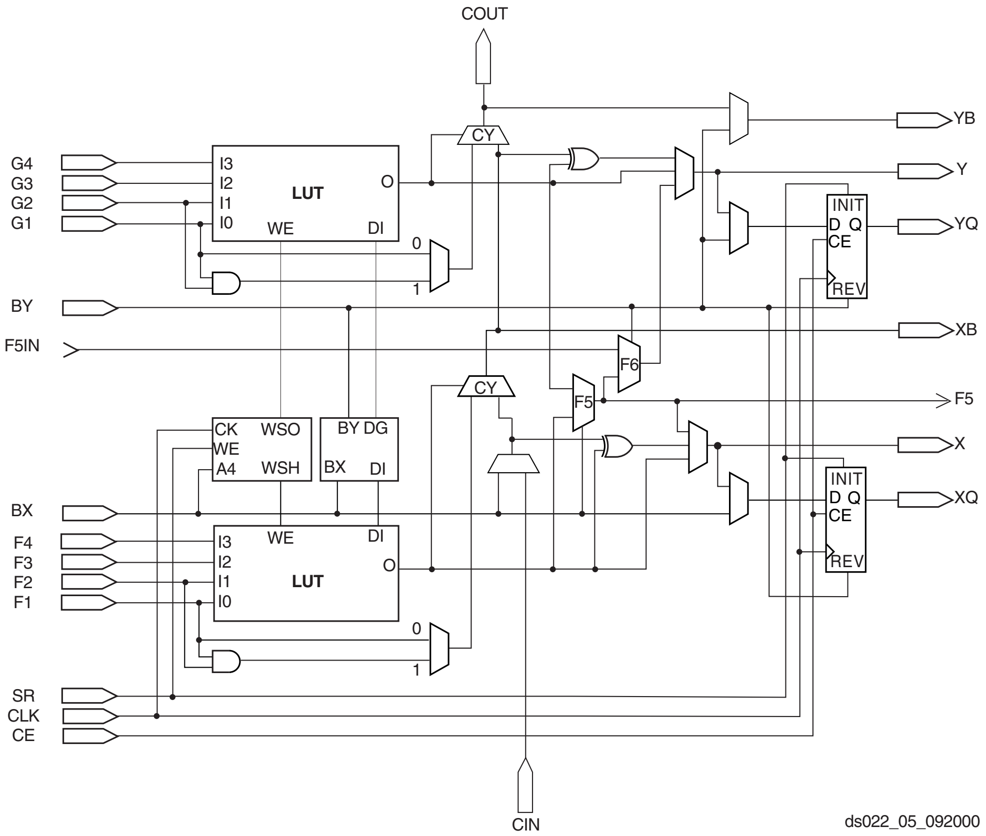


Figure 2: **Detailed View of Virtex-E Slice**

Pinout Differences Between Virtex and Virtex-E Families

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions, listed in Table 1.

XCV200E Device, FG456 Package

The Virtex-E XCV200E has two I/O pins swapped with the Virtex XCV200 to accommodate differential clock pairing.

XCV400E Device, FG676 Package

The Virtex-E XCV400E has two I/O pins swapped with the Virtex XCV400 to accommodate differential clock pairing.

All Devices, PQ240 and HQ240 Packages

The Virtex devices in PQ240 and HQ240 packages do not have V_{CCO} banking, but Virtex-E devices do. To achieve this, eight Virtex I/O pins (P232, P207, P176, P146, P116, P85, P55, and P25) are now VCCO pins in the Virtex-E family. This change also requires one Virtex I/O or VREF pin to be swapped with a standard I/O pin.

Additionally, accommodating differential clock input pairs in Virtex-E caused some IO_V_{REF} differences in the XCV400E and XCV600E devices only. Virtex IO_V_{REF} pins P215 and P87 are Virtex-E IO_V_{REF} pins P216 and P86, respectively. Virtex-E pins P215 and P87 are IO_DLL.

Table 1: **Pinout Differences Summary**

Part	Package	Pins	Virtex	Virtex-E
XCV200	FG456	E11, U11	I/O	No Connect
		B11, AA11	No Connect	IO_LVDS_DLL
XCV400	FG676	D13, Y13	I/O	No Connect
		B13, AF13	No Connect	IO_LVDS_DLL
XCV400/600	PQ240/HQ240	P215, P87	IO_V_{REF}	IO_LVDS_DLL
		P216, P86	I/O	IO_V_{REF}
All	PQ240/HQ240	P232, P207, P176, P146, P116, P85, P55, and P25	I/O	V_{CCO}
		P231	I/O	IO_V_{REF}

Low Voltage Differential Signals

The Virtex-E family incorporates low-voltage signalling (LVDS and LVPECL). Two pins are utilized for these signals to be connected to a Virtex-E device. These are known as differential pin pairs. Each differential pin pair has a Positive (P) and a Negative (N) pin. These pairs are labeled in the following manner.

IO_L#[P/N]

where

L = LVDS or LVPECL pin
# = Pin Pair Number
P = Positive
N = Negative

I/O pins for differential signals can either be synchronous or asynchronous, input or output. The pin pairs can be used for synchronous input and output signals as well as asynchronous input signals. However, only some of the low-voltage pairs can be used for asynchronous output signals.

DIfferential signals require the pins of a pair to switch almost simultaneously. If the signals driving the pins are from IOB flip-flops, they are synchronous. If the signals driving the pins are from internal logic, they are asynchronous. Table 2 defines the names and function of the different types of low-voltage pin pairs in the Virtex-E family.

Table 2: **LVDS Pin Pairs**

Pin Name	Description
IO_L#[P/N] Example: IO_L22N	Represents a general IO or a synchronous input/output differential signal. When used as a differential signal, N means Negative I/O and P means Positive I/O.
IO_L#[P/N]_Y Example: IO_L22N_Y	Represents a general IO or a synchronous input/output differential signal, or a part-dependent asynchronous output differential signal.
IO_L#[P/N]_YY Example: O_L22N_YY	Represents a general IO or a synchronous input/output differential signal, or an asynchronous output differential signal.
IO_LVDS_DLL_L#[P/N] Example: IO_LVDS_DLL_L16N	Represents a general IO or a synchronous input/output differential signal, a differential clock input signal, or a DLL input. When used as a differential clock input, this pin is paired with the adjacent GCK pin. The GCK pin is always the positive input in the differential clock input configuration.

Virtex-E Package Pinouts

The Virtex-E family of FPGAs is available in 12 popular packages, including chip-scale, plastic and high heat-dissipation quad flat packs, and ball grid and fine-pitch ball grid arrays. Family members have footprint compatibility across devices provided in the same package. The pinout tables in this section indicate function, pin, and bank information for each package/device combination. Following each pinout table is an additional table summarizing information specific to differential pin pairs for all devices provided in that package.

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
NA	VCCINT	N29	
NA	VCCINT	N33	
NA	VCCINT	U5	
NA	VCCINT	U30	
NA	VCCINT	Y2	
NA	VCCINT	Y31	
NA	VCCINT	AB2	
NA	VCCINT	AB32	
NA	VCCINT	AD2	
NA	VCCINT	AD32	
NA	VCCINT	AG3	
NA	VCCINT	AG31	
NA	VCCINT	AJ13	
NA	VCCINT	AK8	
NA	VCCINT	AK11	
NA	VCCINT	AK17	
NA	VCCINT	AK20	
NA	VCCINT	AL14	
NA	VCCINT	AL22	
NA	VCCINT	AL27	
NA	VCCINT	AN25	
0	VCCO	A22	
0	VCCO	A26	
0	VCCO	A30	
0	VCCO	B19	
0	VCCO	B32	
1	VCCO	A10	
1	VCCO	A16	
1	VCCO	B13	
1	VCCO	C3	
1	VCCO	E5	
2	VCCO	B2	
2	VCCO	D1	
2	VCCO	H1	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	VCCO	M1	
2	VCCO	R2	
3	VCCO	V1	
3	VCCO	AA2	
3	VCCO	AD1	
3	VCCO	AK1	
3	VCCO	AL2	
4	VCCO	AN4	
4	VCCO	AN8	
4	VCCO	AN12	
4	VCCO	AM2	
4	VCCO	AM15	
5	VCCO	AL31	
5	VCCO	AM21	
5	VCCO	AN18	
5	VCCO	AN24	
5	VCCO	AN30	
6	VCCO	W32	
6	VCCO	AB33	
6	VCCO	AF33	
6	VCCO	AK33	
6	VCCO	AM32	
7	VCCO	C32	
7	VCCO	D33	
7	VCCO	K33	
7	VCCO	N32	
7	VCCO	T33	
NA	GND	A1	
NA	GND	A7	
NA	GND	A12	
NA	GND	A14	
NA	GND	A18	
NA	GND	A20	
NA	GND	A24	

Table 15: **BG560 Differential Pin Pair Summary XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF
173	7	H33	L29	4	-
174	7	H32	J31	18	VREF
175	7	H31	K29	14	-
176	7	G32	J30	20	VREF
177	7	G31	J29	√	VREF
178	7	E32	E33	15	-
179	7	F31	H29	14	-
180	7	E31	D32	15	VREF
181	7	C33	G29	14	-
182	7	D31	F30	14	VREF

Notes:

1. AO in the XCV1600E.
2. AO in the XCV2000E.
3. AO in the XCV1600E, 2000E.
4. AO in the XCV1000E, 1600E.
5. AO in the XCV1000E, 2000E.
6. AO in the XCV1000E.
7. AO in the XCV1000E, 1600E, 2000E.
8. AO in the XCV600E, 1600E.
9. AO in the XCV400E, 600E, 1600E.
10. AO in the XCV400E, 600E, 1000E, 2000E.
11. AO in the XCV400E, 600E, 1000E.
12. AO in the XCV400E, 1000E, 2000E.
13. AO in the XCV400E, 600E, 1000E, 1600E.
14. AO in the XCV400E, 1000E, 1600E.
15. AO in the XCV600E, 1000E, 2000E.
16. AO in the XCV600E, 2000E.
17. AO in the XCV400E, 600E, 1600E, 2000E.
18. AO in the XCV600E, 1000E, 1600E, 2000E.
19. AO in the XCV400E, 600E, 2000E.
20. AO in the XCV400E, 1000E.

FG256 Fine-Pitch Ball Grid Array Packages

XCV50E, XCV100E, XCV200E, and XCV300E devices in FG256 fine-pitch Ball Grid Array packages have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 16, see Table 17 for Differential Pair information.

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
0	GCK3	B8
0	IO	B3
0	IO	E7
0	IO	D8
0	IO_L0N_Y	C5
0	IO_VREF_L0P_Y	A3[2]
0	IO_L1N_YY	D5
0	IO_L1P_YY	E6
0	IO_VREF_L2N_YY	B4
0	IO_L2P_YY	A4
0	IO_L3N_Y	D6
0	IO_L3P_Y	B5
0	IO_VREF_L4N_YY	C6[1]
0	IO_L4P_YY	A5
0	IO_L5N_YY	B6
0	IO_L5P_YY	C7
0	IO_L6N_Y	D7
0	IO_L6P_Y	C8
0	IO_VREF_L7N_Y	B7
0	IO_L7P_Y	A6
0	IO_LVDS_DLL_L8N	A7
1	GCK2	C9
1	IO	B10
1	IO_LVDS_DLL_L8P	A8
1	IO_L9N_Y	D9
1	IO_L9P_Y	A9
1	IO_L10N_Y	E10
1	IO_VREF_L10P_Y	B9

Table 17: **FG256 Differential Pin Pair Summary XCV50E, XCV100E, XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
19	2	C15	D14	√	DIN, D0
20	2	B16	E13	6	VREF
21	2	C16	E14	√	-
22	2	F13	E15	1	VREF
23	2	F12	D16	5	-
24	2	F14	E16	3	D1
25	2	F15	G13	√	D2
26	2	F16	G12	6	-
27	2	G15	G14	√	-
28	2	H13	G16	3	D3
29	2	J13	H15	4	-
30	2	H14	H16	√	-
31	3	K15	J14	4	-
32	3	J16	K16	3	VREF
33	3	K12	L15	√	-
34	3	K13	L16	6	-
35	3	K14	M16	√	D5
36	3	N16	L13	3	VREF
37	3	P16	L12	5	-
38	3	M15	L14	1	VREF
39	3	M14	R16	√	-
40	3	M13	T15	6	VREF
41	3	N14	N15	√	INIT
42	4	T14	P13	√	-
43	4	P12	R13	7	VREF
44	4	N12	T13	√	-
45	4	T12	P11	√	VREF
46	4	R12	N11	2	-
47	4	T11	M11	√	VREF
48	4	R11	T10	√	-
49	4	R10	M10	1	-
50	4	P9	T9	1	VREF
51	4	N10	R9	1	-
52	5	N9	T8	NA	IO_LVDS_DLL
53	5	R7	P8	1	VREF
54	5	P7	T6	1	-
55	5	M7	R6	√	-
56	5	P6	R5	√	VREF
57	5	N6	T5	2	-
58	5	M6	T4	√	VREF
59	5	T3	P5	√	-
60	5	T2	N5	7	VREF
61	6	R1	M3	√	-
62	6	N2	M4	6	VREF
63	6	P1	L5	√	-
64	6	L3	N1	1	VREF
65	6	L4	M2	5	-
66	6	K4	M1	3	VREF
67	6	L1	L2	√	-
68	6	K1	K3	6	-
69	6	K5	K2	√	-
70	6	J1	J3	3	VREF
71	6	H1	J4	4	-
72	7	H4	G1	√	-
73	7	H2	G5	4	-
74	7	H3	G4	3	VREF
75	7	F5	G2	√	-
76	7	F1	F4	6	-
77	7	F2	G3	√	-
78	7	D1	E1	3	VREF
79	7	E2	E4	5	-
80	7	C1	F3	1	VREF
81	7	E3	D2	√	-
82	7	A2	B1	6	VREF

Notes:

1. AO in the XCV50E, 200E, 300E.
2. AO in the XCV50E, 200E.
3. AO in the XCV50E, 300E.
4. AO in the XCV100E, 200E.
5. AO in the XCV200E.
6. AO in the XCV100E.
7. AO in the XCV50E.

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
7	IO_L234N_YY	K38
7	IO_L234P_YY	L37
7	IO_L235N_YY	J39
7	IO_VREF_L235P_YY	L36
7	IO_L236N	J38
7	IO_L236P	K37
7	IO_L237N	H39
7	IO_VREF_L237P	K36[3]
7	IO_L238N_YY	H38
7	IO_L238P_YY	J37
7	IO_L239N_YY	G39
7	IO_VREF_L239P_YY	G38
7	IO_L240N_Y	J36
7	IO_L240P_Y	F39
7	IO_L241N	H37
7	IO_L241P	F38
7	IO_L242N_YY	H36
7	IO_L242P_YY	E39
7	IO_L243N_Y	G37
7	IO_VREF_L243P_Y	E38
7	IO_L244N	G36
7	IO_L244P	D39
7	IO_L245N	D38
7	IO_VREF_L245P	F36[1]
7	IO_L246N_Y	D37
7	IO_L246P_Y	E37
2	CCLK	E4
3	DONE	AU5
NA	DXN	AV37
NA	DXP	AU35
NA	M0	AT37
NA	M1	AU38
NA	M2	AT35
NA	PROGRAM	AT5
NA	TCK	C36

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	TDI	B3
2	TDO	C4
NA	TMS	E36
NA	VCCINT	E8
NA	VCCINT	E9
NA	VCCINT	E15
NA	VCCINT	E16
NA	VCCINT	E24
NA	VCCINT	E25
NA	VCCINT	E31
NA	VCCINT	E32
NA	VCCINT	H5
NA	VCCINT	H35
NA	VCCINT	J5
NA	VCCINT	J35
NA	VCCINT	R5
NA	VCCINT	R35
NA	VCCINT	T5
NA	VCCINT	T35
NA	VCCINT	AD5
NA	VCCINT	AD35
NA	VCCINT	AE5
NA	VCCINT	AE35
NA	VCCINT	AL5
NA	VCCINT	AL35
NA	VCCINT	AM5
NA	VCCINT	AM35
NA	VCCINT	AR8
NA	VCCINT	AR9
NA	VCCINT	AR15
NA	VCCINT	AR16
NA	VCCINT	AR24
NA	VCCINT	AR25
NA	VCCINT	AR31
NA	VCCINT	AR32

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	D20
NA	GND	D12
NA	GND	C39
NA	GND	C37
NA	GND	C3
NA	GND	C20
NA	GND	C1
NA	GND	B39
NA	GND	B38
NA	GND	B2
NA	GND	B1
NA	GND	AW39
NA	GND	AW38
NA	GND	AW37
NA	GND	AW3
NA	GND	AW2
NA	GND	AW1
NA	GND	AV39
NA	GND	AV38
NA	GND	AV2
NA	GND	AV1
NA	GND	AU39
NA	GND	AU37
NA	GND	AU3
NA	GND	AU20
NA	GND	AU1
NA	GND	AT4
NA	GND	AT36
NA	GND	AT28
NA	GND	AT20
NA	GND	AT12
NA	GND	AR5
NA	GND	AR35
NA	GND	AR28
NA	GND	AR21
NA	GND	AR20
NA	GND	AR19
NA	GND	AR12
NA	GND	AH5
NA	GND	AH4
NA	GND	AH36
NA	GND	AH35
NA	GND	AA5
NA	GND	AA35
NA	GND	A39
NA	GND	A38
NA	GND	A37
NA	GND	A3
NA	GND	A2
NA	GND	A1

Notes:

1. V_{REF} or I/O option only in the XCV1000E, 1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
3. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
188	5	AY27	AV28	√	-
189	5	BA27	AW29	5	-
190	5	BB28	AV29	1	-
191	5	AY28	AW30	1	-
192	5	BA28	AW31	2	-
193	5	BB29	AV31	√	-
194	5	AY29	AY32	√	VREF
195	5	AW32	BB30	2	-
196	5	AV32	AY30	2	-
197	5	BA30	AW33	√	VREF
198	5	BB31	AV33	√	-
199	5	AY34	BA31	1	VREF
200	5	AW34	BB32	1	-
201	5	BA32	AY35	√	VREF
202	5	BB33	AW35	√	-
203	5	AV35	BB34	5	-
204	5	AY36	BA34	5	-
205	5	BB35	AV36	√	VREF
206	5	BA35	AY37	√	-
207	5	BB36	BA36	5	-
208	5	AW37	BB37	1	VREF
209	5	BA37	AY38	1	-
210	5	BB38	AY39	2	-
211	6	AV42	AV41	√	-
212	6	AU41	AW40	3	-
213	6	AU42	AV39	1	-
214	6	AU38	AT41	2	VREF
215	6	AV40	AT42	4	-
216	6	AU39	AR41	2	-
217	6	AU40	AR42	1	VREF
218	6	AP42	AT38	√	-
219	6	AT39	AN41	2	-
220	6	AM40	AT40	1	-
221	6	AM41	AR38	√	VREF
222	6	AR40	AM42	√	-
223	6	AP38	AL40	5	VREF
224	6	AL42	AP39	2	-
225	6	AK40	AP40	√	VREF
226	6	AN39	AK41	√	-
227	6	AN40	AK42	2	-
228	6	AJ41	AM38	√	VREF
229	6	AM39	AJ42	√	-
230	6	AH41	AH40	3	-
231	6	AH42	AL38	1	-
232	6	AG41	AL39	2	-
233	6	AG40	AK39	4	-
234	6	AG42	AJ38	2	-
235	6	AJ39	AF42	1	VREF
236	6	AH38	AF41	√	-
237	6	AH39	AE42	2	-
238	6	AE41	AG38	1	-
239	6	AD42	AG39	√	VREF
240	6	AF39	AD40	√	-
241	6	AE38	AD41	5	-
242	6	AC40	AE39	2	-
243	6	AC41	AD38	√	VREF
244	6	AC38	AB42	√	-
245	6	AC39	AB40	2	VREF
246	7	AB39	AA41	√	-
247	7	AA39	Y41	2	VREF
248	7	Y39	Y40	√	-
249	7	W41	Y38	√	VREF
250	7	W39	W40	2	-
251	7	V41	W38	5	-
252	7	V40	V39	√	-
253	7	U39	V42	√	VREF
254	7	U38	U41	1	-
255	7	T39	U42	2	-

Table 25: **FG860 Differential Pin Pair Summary XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	T38	T41	√	-
257	7	T42	R39	1	VREF
258	7	R38	R42	2	-
259	7	P39	R40	4	-
260	7	P38	R41	2	-
261	7	N39	P42	1	-
262	7	M39	P40	3	-
263	7	M38	P41	√	-
264	7	L39	N42	√	VREF
265	7	N41	L38	2	-
266	7	M42	K40	√	-
267	7	K38	M40	√	VREF
268	7	J40	M41	2	-
269	7	L40	J39	5	VREF
270	7	L41	J38	√	-
271	7	H39	K42	√	VREF
272	7	H38	K41	1	-
273	7	G40	J41	2	-
274	7	G39	H42	√	-
275	7	G42	G38	1	VREF
276	7	F40	G41	2	-
277	7	F41	F42	4	-
278	7	E42	F39	2	VREF
279	7	E41	E40	1	-
280	7	D41	E39	3	-

Notes:

1. AO in the XCV1000E, 2000E.
2. AO in the XCV1000E, 1600E.
3. AO in the XCV2000E.
4. AO in the XCV1600E.
5. AO in the XCV1000E.

FG900 Fine-Pitch Ball Grid Array Package

XCV600E, XCV1000E, and XCV1600E devices in the FG900 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 26, see Table 27 for Differential Pair information.

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
0	GCK3	C15
0	IO	A7[4]
0	IO	A13[4]
0	IO	C5[4]
0	IO	C6[4]
0	IO	C14[4]
0	IO	D8[5]
0	IO	D10
0	IO	D13[4]
0	IO	E6
0	IO	E9[5]
0	IO	E14[5]
0	IO	F9[4]
0	IO	F14[5]
0	IO	G15
0	IO	K11[5]
0	IO	K12
0	IO	L13[4]
0	IO_L0N_YY	C4[4]
0	IO_L0P_YY	F7[3]
0	IO_L1N_Y	D5
0	IO_L1P_Y	G8
0	IO_VREF_L2N_Y	A3[1]
0	IO_L2P_Y	H9
0	IO_L3N_Y	B4[4]
0	IO_L3P_Y	J10[4]
0	IO_L4N_YY	A4
0	IO_L4P_YY	D6
0	IO_VREF_L5N_YY	E7
0	IO_L5P_YY	B5

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
7	IO	E3
7	IO	F1[4]
7	IO	G1[5]
7	IO	G4[5]
7	IO	H3[5]
7	IO	J1[4]
7	IO	J3[4]
7	IO	J4[4]
7	IO	J6[4]
7	IO	L10[4]
7	IO	N2[4]
7	IO	N8[4]
7	IO	N10[4]
7	IO	P3[5]
7	IO	P9[4]
7	IO	R1[5]
7	IO	T3[4]
7	IO_L247P	R10
7	IO_L248N_YY	R5[3]
7	IO_L248P_YY	R6[4]
7	IO_L249N_YY	R8
7	IO_VREF_L249P_YY	R4[2]
7	IO_L250N_YY	R7
7	IO_L250P_YY	R3
7	IO_L251N_YY	P10
7	IO_VREF_L251P_YY	P6
7	IO_L252N_YY	P5
7	IO_L252P_YY	P2
7	IO_L253N	P7
7	IO_L253P	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6
7	IO_L256P	N6
7	IO_L257N_YY	N5
7	IO_L257P_YY	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N	M2
7	IO_VREF_L259P	M1[1]
7	IO_L260N_YY	L4
7	IO_L260P_YY	L2
7	IO_L261N_Y	M7[4]
7	IO_L261P_Y	L5[4]
7	IO_L262N_YY	L1
7	IO_L262P_YY	M8
7	IO_L263N	K2
7	IO_L263P	M9
7	IO_L264N	L3[4]
7	IO_L264P	M10[4]
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6
7	IO_VREF_L266P_YY	K3
7	IO_L267N_YY	L7
7	IO_L267P_YY	K4
7	IO_L268N_YY	L8
7	IO_L268P_YY	J5
7	IO_L269N_YY	K6
7	IO_VREF_L269P_YY	H4
7	IO_L270N_YY	H1
7	IO_L270P_YY	K7
7	IO_L271N	J7
7	IO_L271P	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
32	0	B14	E14	3200 2600 2000 1600 1000	-
33	0	D14	G15	3200 2600 2000 1600 1000	VREF
34	0	D15	J16	3200 1600	-
35	0	B15	F15	3200 2000 1000	-
36	0	E15	A15	3200 2000 1000	-
37	0	A16	G16	3200 2600	-
38	0	J17	F16	3200 2600 2000 1600 1000	-
39	0	B16	C16	3200 2600 2000 1600 1000	VREF
40	0	A17	H17	2600 1600 1000	-
41	0	B17	G17	2600 1600 1000	VREF
42	1	J18	C17	None	IO_LVDS_DLL
43	1	C18	G18	2600 1600 1000	VREF
44	1	F18	H18	2600 1600 1000	-
45	1	A19	B19	3200 2600 2000 1600 1000	VREF
46	1	C19	K19	3200 2600 2000 1600 1000	-
47	1	E19	F19	3200 2600	-
48	1	J19	G19	3200 2000 1000	-
49	1	G20	A20	3200 2000 1000	-
50	1	F20	B20	3200 1600	-
51	1	E20	D20	3200 2600 2000 1600 1000	VREF
52	1	A21	H20	3200 2600 2000 1600 1000	-
53	1	J20	E21	3200	-
54	1	K20	D21	3200 2600 1000	-
55	1	H21	B21	3200 2600 1000	-
56	1	F21	G21	2000 1600	-
57	1	B22	A22	3200 2600 2000 1600 1000	VREF
58	1	C22	J21	3200 2600 2000 1600 1000	-
59	1	G22	D22	3200 2600 1000	-
60	1	A23	K21	3200 2000 1000	-
61	1	B23	F22	3200 2000 1000	-
62	1	H22	C23	3200 1600 1000	-
63	1	K22	D23	3200 2600 2000 1600 1000	-
64	1	J22	A24	3200 2600 2000 1600 1000	VREF
65	1	D24	H23	2600 1600 1000	-
66	1	E24	A25	2600 1600 1000	-
67	1	C25	A26	3200 2600 2000 1600 1000	VREF
68	1	B26	F24	3200 2600 2000 1600 1000	-
69	1	F25	K23	3200 2600	-
70	1	H24	C26	3200 2000 1000	VREF

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
311	7	P2	R8	2600 2000 1000	-
312	7	N1	R9	3200 2600 2000	-
313	7	R10	P4	3200 2600 1600 1000	-
314	7	N2	P8	3200 2600 2000 1600 1000	-
315	7	P7	P6	3200 2600 2000 1600	-
316	7	N4	M1	2600 2000 1000	VREF
317	7	N3	N6	3200 1600 1000	-
318	7	M2	P9	2600 1600	-
319	7	M3	N7	3200 2600 1600 1000	-
320	7	M4	P10	2000 1000	-
321	7	N8	L1	3200 2600 2000	-
322	7	N9	L2	3200 2600 2000 1600 1000	-
323	7	K1	M7	2000 1600 1000	VREF
324	7	L4	M8	3200 1600 1000	-
325	7	L5	J1	3200 2600 2000 1600 1000	-
326	7	K3	J2	3200 2600 2000 1600 1000	VREF
327	7	J3	L7	3200 2600 1600 1000	-
328	7	H2	M9	3200 2600 1600	-
329	7	K6	J4	2600 1000	VREF
330	7	G2	L8	3200 2600 2000 1600 1000	-
331	7	K7	H3	2000 1600	-
332	7	J5	G3	3200 2600 2000 1600 1000	VREF
333	7	H5	L9	2600 2000 1000	-
334	7	H4	J6	3200 2600 2000	-
335	7	K8	G4	3200 2600 1600 1000	-
336	7	F2	J7	3200 2600 2000 1600 1000	-
337	7	L10	F3	3200 2600 2000 1600	-
338	7	H6	E1	2600 2000 1000	VREF
339	7	E2	G5	3200 2600 1600 1000	-
340	7	D1	K9	2600 1600	-
341	7	J8	E3	3200 2600 1600 1000	VREF
342	7	D2	E4	2600 2000 1000	-
343	7	D3	F4	3200 2600 2000	-

Date	Version	Revision
4/2/01	2.0	• Updated numerous values in **Virtex-E Switching Characteristics** tables. • Changed pinout table footnotes from "V_{REF} option only" to "V_{REF} or I/O option only" to improve clarity. • Converted file to modularized format. See the **Virtex-E Data Sheet** section.
7/26/01	2.1	• Changed pinout table footnotes from "V_{REF} or I/O option only" to "V_{REF} or I/O option only; otherwise I/O only" to improve clarity. • Changed designation for pin pair 300 in Table 29 from AO to footnote 9.
10/25/01	2.2	• Changed Table 29 to clarify which devices in the FG1156 package can use each pin pair as an asynchronous output. • Updated references to the XCV3200E device in the FG1156 package.
11/15/01	2.3	• Fixed cosmetic error.
07/17/02	2.4	• Added “VREF” to the description for pin B15 in Table 12. • Changed designation for pin pair 129 in Table 15 from AO to “AO in the XCV1000E, 1600E, 2000E“. • Data sheet designation upgraded from Preliminary to Production.
03/14/03	2.5	• Removed the Virtex-E XCV300E section under **Pinout Differences Between Virtex and Virtex-E Families** (and revised Table 1), since these differences do not exist.

Virtex-E Data Sheet

The Virtex-E Data Sheet contains the following modules:

- DS022-1, Virtex-E 1.8V FPGAs: **Introduction and Ordering Information (Module 1)**
- DS022-2, Virtex-E 1.8V FPGAs: **Functional Description (Module 2)**
- DS022-3, Virtex-E 1.8V FPGAs: **DC and Switching Characteristics (Module 3)**
- DS022-4, Virtex-E 1.8V FPGAs: **Pinout Tables (Module 4)**