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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	196
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	352-LBGA Exposed Pad, Metal
Supplier Device Package	352-MBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-6bg352i

Architectural Description

Virtex-E Array

The Virtex-E user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

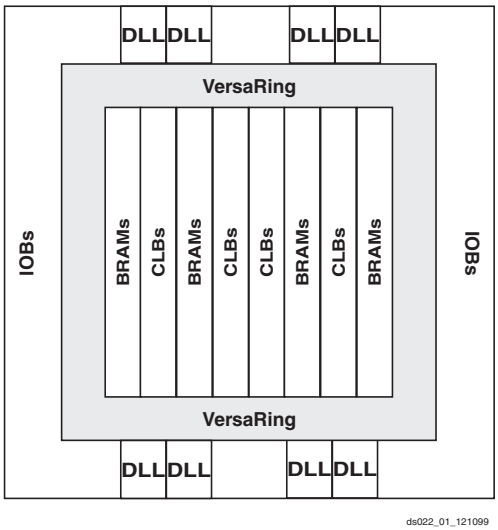


Figure 1: **Virtex-E Architecture Overview**

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Input/Output Block

The Virtex-E IOB, Figure 2, features SelectI/O+ inputs and outputs that support a wide variety of I/O signalling standards, see Table 1.

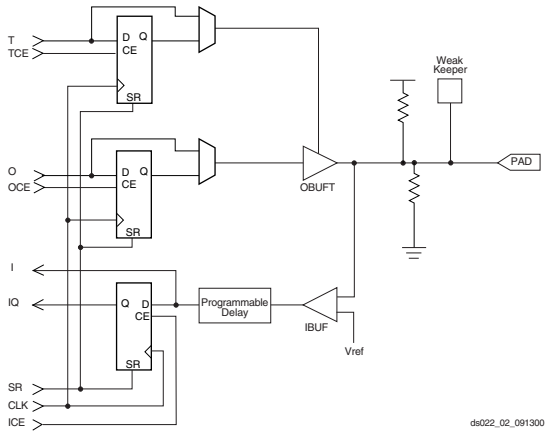


Figure 2: **Virtex-E Input/Output Block (IOB)**

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

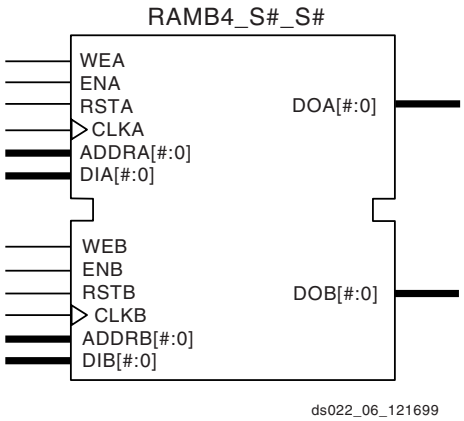


Figure 6: **Dual-Port Block SelectRAM**

Table 5 shows the depth and width aspect ratios for the block SelectRAM. The Virtex-E block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAMs. Refer to XAPP130 for block SelectRAM timing waveforms.

Table 5: **Block SelectRAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex-E routing architecture and its place-and-route software were defined in a joint optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources (see Figure 7), providing three types of connections:

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

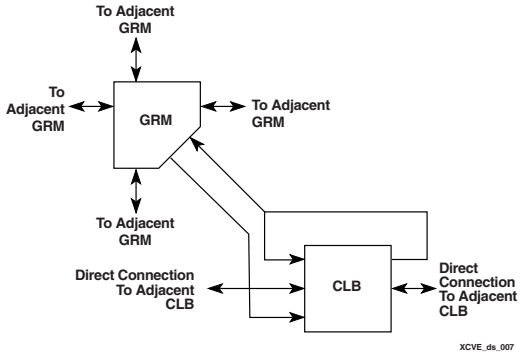


Figure 7: **Virtex-E Local Routing**

General Purpose Routing

Most Virtex-E signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. General-purpose routing resources are located in horizontal and vertical routing channels associated with the CLB rows and columns and are as follows:

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines are driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex-E devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple devices.

To guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. For more information about DLL functionality, see the Design Consideration section of the data sheet.

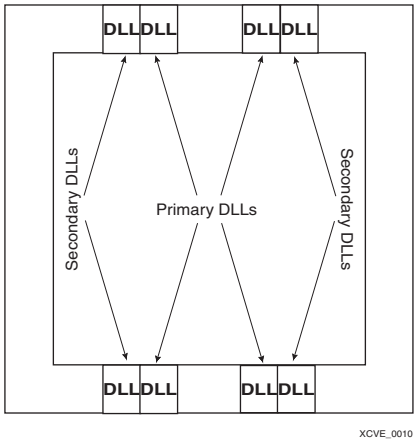


Figure 10: **DLL Locations**

Boundary Scan

Virtex-E devices support all the mandatory Boundary Scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary Scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the Boundary Scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the Boundary Scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the Boundary Scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series Boundary Scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Data Registers

The primary data register is the Boundary Scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream Boundary Scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the Boundary Scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the Boundary Scan data-register bits are ordered as shown in Figure 12.

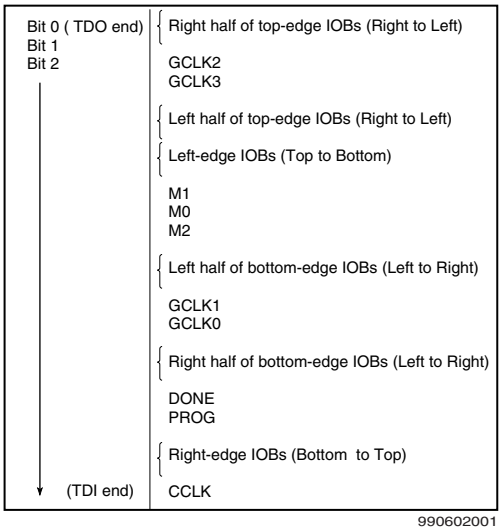


Figure 12: **Boundary Scan Bit Sequence**

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for

XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Note:

Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the Boundary Scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the Boundary Scan symbol and connect the necessary pins as appropriate.

3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

Table 11: **SelectMAP Write Timing Characteristics**

	Description		Symbol		Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0 / 1.7	ns, min
	$\overline{CS}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0 / 1.7	ns, min
	$\overline{WRITE}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

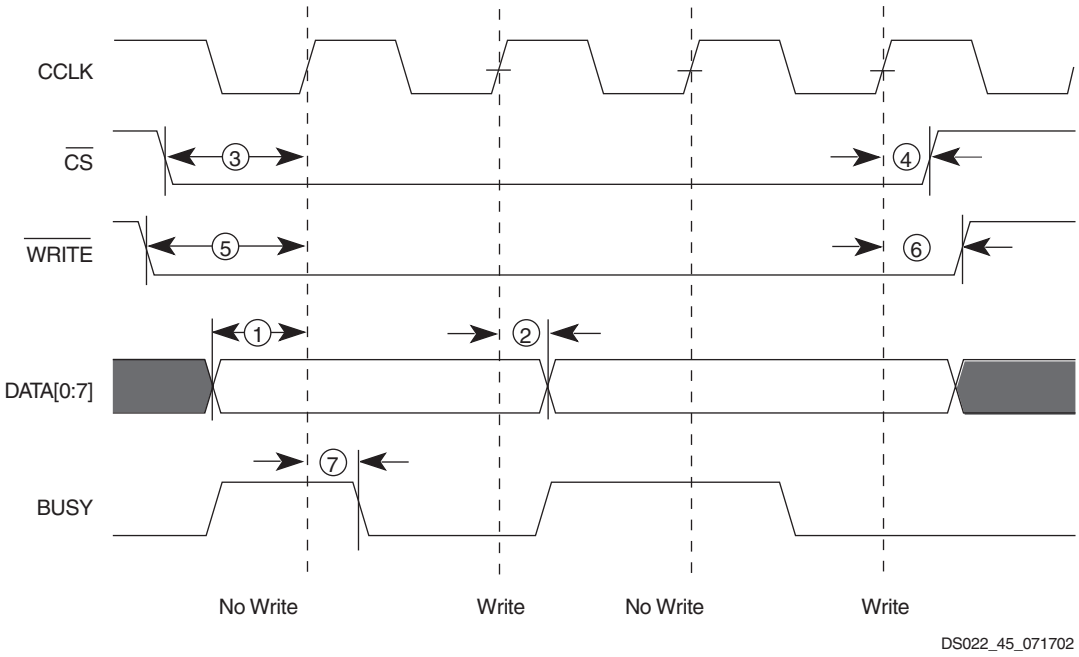


Figure 17: **Write Operations**

A flowchart for the write operation is shown in Figure 18. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important.

While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, resolve this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory buses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak “keeper” circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 52. DC voltage specifications appear in Table 31.

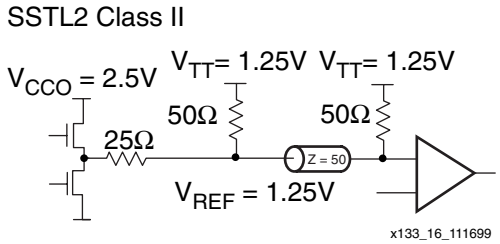


Figure 52: **Terminated SSTL2 Class II**

Table 31: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} - 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 53. DC voltage specifications appear in Table 32.

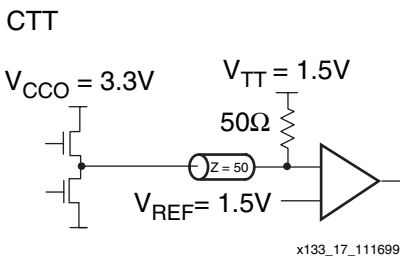


Figure 53: **Terminated CTT**

Table 32: **CTT Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL}= V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 33.

Table 33: **PCI33_3 and PCI66_3 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO} + 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL}= 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:
1. Tested according to the relevant specification.

LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in Figure 54. A sample circuit illustrating a valid termination for receiving LVDS signals appears in Figure 55. Table 38 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

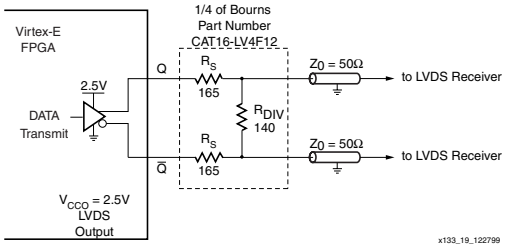


Figure 54: **Transmitting LVDS Signal Circuit**

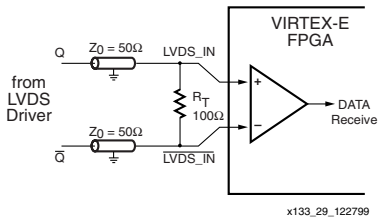


Figure 55: **Receiving LVDS Signal Circuit**

Table 38: **LVDS Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
V_{ICM}(2)	0.2	1.25	2.2
V_{OCM}(1)	1.125	1.25	1.375
V_{IDIFF} (1)	0.1	0.35	-
V_{ODIFF} (1)	0.25	0.35	0.45
V_{OH}(1)	1.25	-	-
V_{OL}(1)	-	-	1.25

Notes:
1. Measured with a 100 Ω resistor across Q and $\overline{Q}$.
2. Measured with a differential input voltage = +/– 350 mV.

LVPECL

Depending on whether the device is transmitting or receiving an LVPECL signal, two different circuits are used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in Figure 56. A sample circuit illustrating a valid termination for receiving LVPECL signals appears in Figure 57. Table 39 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 40.

Table 39: **LVPECL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.49	-	2.72
V_{IL}	0.86	-	2.125
V_{OH}	1.8	-	-
V_{OL}	-	-	1.57

Notes:
1. For more detailed information, see **DS022-3**: *Virtex-E 1.8V FPGA DC and Switching Characteristics*, Module 3, LVPECL DC Specifications section.

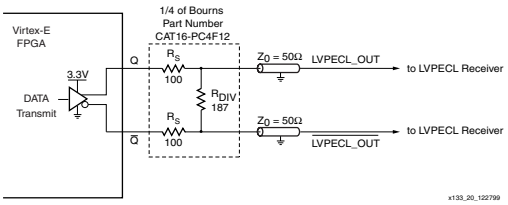


Figure 56: **Transmitting LVPECL Signal Circuit**

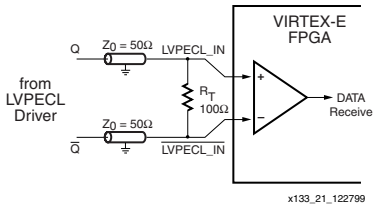


Figure 57: **Receiving LVPECL Signal Circuit**

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the global clock buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUFG connection has a net connected to it. Since the N-side IBUFG does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_p_external, O=>clk_internal);

gclk0_n : IBUFG_LVDS port map
(I=>clk_n_external, O=>clk_internal);
```

Verilog Instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_p_external),
.O(clk_internal));

IBUFG_LVDS gclk0_n (.I(clk_n_external),
.O(clk_internal));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET clk_p_external LOC = GCLKPAD3;

NET clk_n_external LOC = C17;
```

GCLKPAD3 can also be replaced with the package pin name, such as D17 for the BG432 package.

Creating LVDS Input Buffers

An LVDS input buffer can be placed in a wide number of IOB locations. The exact location is dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Only one input buffer is required to be instantiated in the design and placed on the correct IO_L#P location. The N-side of the buffer is reserved and no other IOB is allowed to be placed on this location. In the physical device, a configuration option is enabled that routes the pad wire from the IO_L#N IOB to the differential input buffer located in the IO_L#P IOB. The output of this buffer then drives the output of the IO_L#P cell or the input register in the IO_L#P IOB. In EPIC it appears that the second buffer is unused. Any attempt to use this location for another purpose leads to a DRC error in the software.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map (I=>data(0),
O=>data_int(0));
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data[0]),
.O(data_int[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data<0> LOC = D28; # IO_L0P
```

Optional N-side

Some designers might prefer to also instantiate the N-side buffer for the input buffer. This allows the top-level net list to include net connections for both PCB layout and system-level integration. In this case, only the output P-side IBUF connection has a net connected to it. Since the N-side IBUF does not have a connection in the EDIF net list, it is trimmed from the design in MAP.

VHDL Instantiation

```
data0_p : IBUF_LVDS port map
(I=>data_p(0), O=>data_int(0));

data0_n : IBUF_LVDS port map
(I=>data_n(0), O=>open);
```

Verilog Instantiation

```
IBUF_LVDS data0_p (.I(data_p[0]),
.O(data_int[0]));

IBUF_LVDS data0_n (.I(data_n[0]), .O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this can be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Adding an Input Register

All LVDS buffers can have an input register in the IOB. The input register is in the P-side IOB only. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries available to explicitly create these structures. The input library macros are listed in Table 42. The I and IB inputs to the macros are the external net connections.

Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels in Table 2. For other standards, adjust the delays with the values shown in **IOB Input Switching Characteristics Standard Adjustments**, page 8.

Table 2: **IOB Input Switching Characteristics**

			Speed Grade(1)				
Description(2)	**Symbol**	**Device**	**Min**	**-8**	**-7**	**-6**	**Units**
Propagation Delays							
Pad to I output, no delay	T_{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T_{IOPID}	XCV50E	0.51	1.0	1.0	1.0	ns, max
		XCV100E	0.51	1.0	1.0	1.0	ns, max
		XCV200E	0.51	1.0	1.0	1.0	ns, max
		XCV300E	0.51	1.0	1.0	1.0	ns, max
		XCV400E	0.51	1.0	1.0	1.0	ns, max
		XCV600E	0.51	1.0	1.0	1.0	ns, max
		XCV1000E	0.55	1.1	1.1	1.1	ns, max
		XCV1600E	0.55	1.1	1.1	1.1	ns, max
		XCV2000E	0.55	1.1	1.1	1.1	ns, max
		XCV2600E	0.55	1.1	1.1	1.1	ns, max
		XCV3200E	0.55	1.1	1.1	1.1	ns, max
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.8	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XCV50E	1.31	2.9	3.0	3.1	ns, max
		XCV100E	1.31	2.9	3.0	3.1	ns, max
		XCV200E	1.39	3.1	3.2	3.3	ns, max
		XCV300E	1.39	3.1	3.2	3.3	ns, max
		XCV400E	1.43	3.2	3.3	3.4	ns, max
		XCV600E	1.55	3.5	3.6	3.7	ns, max
		XCV1000E	1.55	3.5	3.6	3.7	ns, max
		XCV1600E	1.59	3.6	3.7	3.8	ns, max
		XCV2000E	1.59	3.6	3.7	3.8	ns, max
		XCV2600E	1.59	3.6	3.7	3.8	ns, max
		XCV3200E	1.59	3.6	3.7	3.8	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.19	0.40	0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.36	0.76	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.35	0.74	0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.35	0.74	0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.04	0.11	0.20	0.22	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.27	0.63	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.19	0.38	0.46	0.51	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.34	0.78	0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.40	0.77	0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK						
4-input function: F/G Inputs	T_{ICK} / T_{CKI}	0.39 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK} / T_{CKIF5}	0.55 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
6-input function: F5IN input	T_{F5INCK} / T_{CKF5IN}	0.27 / 0	0.6 / 0	0.8 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK} / T_{CKIF6}	0.58 / 0	1.3 / 0	1.5 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK} / T_{CKDI}	0.25 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK} / T_{CKCE}	0.28 / 0	0.55 / 0	0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK} / T_{CKR}	0.24 / 0	0.46 / 0	0.52 / 0	0.6 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}	0.56	1.2	1.3	1.4	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	0.94	1.9	2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.39	0.8	0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}	-	416	400	357	MHz

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM Switching Characteristics

Description	Symbol	Speed Grade(1)				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	0.63	2.46	3.1	3.5	ns, max
Setup and Hold Times before Clock CLK						
ADDR inputs	T_{BACK}/T_{BCKA}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.42 / 0	0.9 / 0	1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	0.97 / 0	2.0 / 0	2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	0.9 / 0	1.8 / 0	2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	0.86 / 0	1.7 / 0	2.0 / 0	2.2 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.6	1.2	1.35	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.6	1.2	1.35	1.5	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}	1.2	2.4	2.7	3.0	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
Combinatorial Delays						
IN input to OUT output	T_{IO}	0.0	0.0	0.0	0 .0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.092	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.092	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

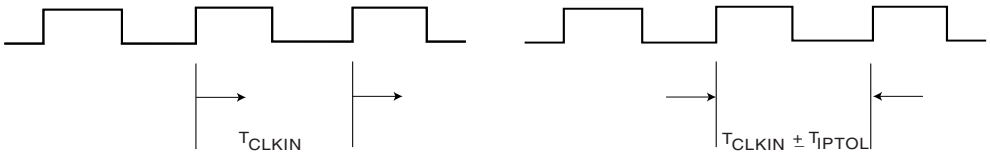
Description	Symbol	Value	Units
TMS and TDI Setup times before TCK	T_{TAPTK}	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	MHz, max

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	350	60	320	60	275	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥2□5 MHz	5.0		5.0		5.0		ns
		≥□50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥□150 MHz	2.0		2.0		2.0		ns
		≥□200 MHz	1.8		1.8		1.8		ns
		≥□250 MHz	1.5		1.5		1.5		ns
		≥□300 MHz	1.3		1.3		NA		ns

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

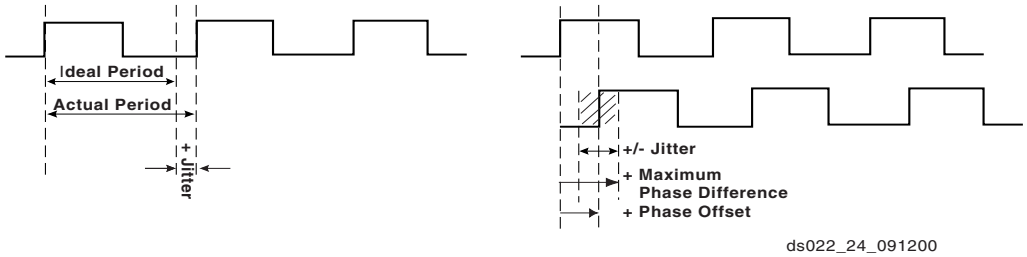


Figure 4: **DLL Timing Waveforms**

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	VCCINT	V24
NA	VCCINT	R23
NA	VCCINT	P25
NA	VCCINT	L25
NA	VCCINT	J24
0	VCCO	D19
0	VCCO	B25
0	VCCO	A17
1	VCCO	D13
1	VCCO	D7
1	VCCO	A10
2	VCCO	K1
2	VCCO	H4
2	VCCO	B2
3	VCCO	Y4
3	VCCO	U1
3	VCCO	P4
4	VCCO	AF10
4	VCCO	AE2
4	VCCO	AC8
5	VCCO	AF17
5	VCCO	AC20
5	VCCO	AC14
6	VCCO	AE25
6	VCCO	W23
6	VCCO	U26
7	VCCO	N23
7	VCCO	K26
7	VCCO	G23
NA	GND	A26
NA	GND	A25
NA	GND	A22

Table 10: **BG352 — XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
NA	GND	A19
NA	GND	A14
NA	GND	A8
NA	GND	A5
NA	GND	A2
NA	GND	A1
NA	GND	B26
NA	GND	B1
NA	GND	E26
NA	GND	E1
NA	GND	H26
NA	GND	H1
NA	GND	N1
NA	GND	P26
NA	GND	W26
NA	GND	W1
NA	GND	AB26
NA	GND	AB1
NA	GND	AE26
NA	GND	AE1
NA	GND	AF26
NA	GND	AF25
NA	GND	AF22
NA	GND	AF19
NA	GND	AF13
NA	GND	AF8
NA	GND	AF5
NA	GND	AF2
NA	GND	AF1

Notes:
1. No Connect in the XCV100E.
2. V_{REF} or I/O option only in the XCV200E and XCV300E; otherwise, I/O option only.

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO_L132P_Y	G28
7	IO_L133N	E31
7	IO_L133P	E30
7	IO_L134N_Y	F29
7	IO_VREF_L134P_Y	F28
7	IO_L135N_Y	D31
7	IO_L135P_Y	D30
7	IO_L136N	E29
7	IO_L136P	E28
2	CCLK	D4
3	DONE	AH4
NA	DXN	AH27
NA	DXP	AK29
NA	M0	AH28
NA	M1	AH29
NA	M2	AJ28
NA	PROGRAM	AH3
NA	TCK	D28
NA	TDI	B3
2	TDO	C4
NA	TMS	D29
NA	VCCINT	A10
NA	VCCINT	A17
NA	VCCINT	B23
NA	VCCINT	B26
NA	VCCINT	C7
NA	VCCINT	C14
NA	VCCINT	C19
NA	VCCINT	F1
NA	VCCINT	F30
NA	VCCINT	K3
NA	VCCINT	K29
NA	VCCINT	N2
NA	VCCINT	N29

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	VCCINT	T1
NA	VCCINT	T29
NA	VCCINT	W2
NA	VCCINT	W31
NA	VCCINT	AB2
NA	VCCINT	AB30
NA	VCCINT	AE29
NA	VCCINT	AF1
NA	VCCINT	AH8
NA	VCCINT	AH24
NA	VCCINT	AJ10
NA	VCCINT	AJ16
NA	VCCINT	AK22
NA	VCCINT	AK13
NA	VCCINT	AK19
0	VCCO	A21
0	VCCO	C29
0	VCCO	D21
1	VCCO	A1
1	VCCO	A11
1	VCCO	D11
2	VCCO	C3
2	VCCO	L4
2	VCCO	L1
3	VCCO	AA1
3	VCCO	AA4
3	VCCO	AJ3
4	VCCO	AH11
4	VCCO	AL1
4	VCCO	AL11
5	VCCO	AH21
5	VCCO	AL21
5	VCCO	AJ29
6	VCCO	AA28
6	VCCO	AA31

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
1	IO_L57N_Y	D9
1	IO_VREF_L57P_Y	A12[2]
1	IO_L58N_Y	E9
1	IO_L58P_Y	C12
1	IO_L59N_YY	B12
1	IO_VREF_L59P_YY	D8
1	IO_L60N_YY	A11
1	IO_L60P_YY	E8
1	IO_L61N_Y	C7
1	IO_L61P_Y	A10
1	IO_L62N_Y	C6
1	IO_L62P_Y	B10
1	IO_L63N_YY	A9
1	IO_VREF_L63P_YY	B9
1	IO_L64N_YY	A8
1	IO_L64P_YY	E7
1	IO_L65N_Y	B8
1	IO_L65P_Y	C5
1	IO_L66N_Y	A7
1	IO_VREF_L66P_Y	A6
1	IO_L67N_Y	B7
1	IO_L67P_Y	D6
1	IO_L68N_Y	A5
1	IO_L68P_Y	C4
1	IO_WRITE_L69N_YY	B6
1	IO_CS_L69P_YY	E6
2	IO	H2
2	IO	H3
2	IO	J1
2	IO	K5
2	IO	M2
2	IO	N1
2	IO	R5
2	IO	U1
2	IO	U4
2	IO	W3
2	IO	Y3
2	IO	AA3
2	IO_DOUT_BUSY_L70P_YY	F5
2	IO_DIN_D0_L70N_YY	D2
2	IO_L71P_Y	E4
2	IO_L71N_Y	E2
2	IO_L72P_Y	D3
2	IO_L72N_Y	F2
2	IO_VREF_L73P_Y	E1
2	IO_L73N_Y	F4
2	IO_L74P	G2
2	IO_L74N	E3
2	IO_L75P_Y	F1
2	IO_L75N_Y	G5
2	IO_VREF_L76P_Y	G1
2	IO_L76N_Y	F3
2	IO_L77P_YY	G4
2	IO_L77N_YY	H1
2	IO_L78P_Y	J2
2	IO_L78N_Y	G3
2	IO_L79P_Y	H5
2	IO_L79N_Y	K2
2	IO_VREF_L80P_YY	H4
2	IO_L80N_YY	K1
2	IO_L81P_YY	L2
2	IO_L81N_YY	L3
2	IO_VREF_L82P_Y	L1[2]
2	IO_L82N_Y	J5
2	IO_L83P_Y	J4
2	IO_L83N_Y	M3
2	IO_VREF_L84P_YY	J3
2	IO_L84N_YY	M1
2	IO_L85P_YY	N2
2	IO_L85N_YY	K4
2	IO_L86P_Y	N3
2	IO_L86N_Y	K3
2	IO_VREF_L87P_YY	L5

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	C42
NA	GND	C41
NA	GND	C40
NA	GND	C3
NA	GND	C2
NA	GND	C1
NA	GND	BB41
NA	GND	BB40
NA	GND	BB4
NA	GND	BB39
NA	GND	BB3
NA	GND	BB2
NA	GND	BA42
NA	GND	BA41
NA	GND	BA40
NA	GND	BA3
NA	GND	BA2
NA	GND	BA1
NA	GND	B42
NA	GND	B41
NA	GND	B40
NA	GND	B3
NA	GND	B2
NA	GND	B1
NA	GND	AY42
NA	GND	AY41
NA	GND	AY40
NA	GND	AY3
NA	GND	AY2
NA	GND	AY1
NA	GND	AW42
NA	GND	AW4
NA	GND	AW39
NA	GND	AW1
NA	GND	AV5
NA	GND	AV38
NA	GND	AV30

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
NA	GND	AV22
NA	GND	AV21
NA	GND	AV13
NA	GND	AU6
NA	GND	AU37
NA	GND	AU30
NA	GND	AU22
NA	GND	AU21
NA	GND	AU13
NA	GND	AK6
NA	GND	AK5
NA	GND	AK38
NA	GND	AK37
NA	GND	AB6
NA	GND	AB5
NA	GND	AB38
NA	GND	AB37
NA	GND	AA6
NA	GND	AA5
NA	GND	AA38
NA	GND	AA37
NA	GND	A41
NA	GND	A40
NA	GND	A4
NA	GND	A39
NA	GND	A3
NA	GND	A2

Notes:
1. V_{REF} or I/O option only in the XCV1600E, 2000E; otherwise, I/O option only.
2. V_{REF} or I/O option only in the XCV2000E; otherwise, I/O option only.

Table 25: **FG860 Differential Pin Pair Summary**
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	1	D11	B15	√	VREF
53	1	C14	E11	2	-
54	1	B14	C10	2	-
55	1	E10	A13	√	VREF
56	1	C9	C13	√	-
57	1	A12	D9	1	VREF
58	1	C12	E9	1	-
59	1	D8	B12	√	VREF
60	1	E8	A11	√	-
61	1	A10	C7	5	-
62	1	B10	C6	5	-
63	1	B9	A9	√	VREF
64	1	E7	A8	√	-
65	1	C5	B8	5	-
66	1	A6	A7	1	VREF
67	1	D6	B7	1	-
68	1	C4	A5	2	-
69	1	E6	B6	√	CS
70	2	F5	D2	√	DIN, D0
71	2	E4	E2	3	-
72	2	D3	F2	1	-
73	2	E1	F4	2	VREF
74	2	G2	E3	4	-
75	2	F1	G5	2	-
76	2	G1	F3	1	VREF
77	2	G4	H1	√	-
78	2	J2	G3	2	-
79	2	H5	K2	1	-
80	2	H4	K1	√	VREF
81	2	L2	L3	√	-
82	2	L1	J5	5	VREF
83	2	J4	M3	2	-
84	2	J3	M1	√	VREF
85	2	N2	K4	√	-

Table 25: **FG860 Differential Pin Pair Summary**
XCV1000E, XCV1600E, XCV2000E

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	2	N3	K3	2	-
87	2	L5	P2	√	D1
88	2	P3	L4	√	D2
89	2	P1	R2	3	-
90	2	M5	R3	1	-
91	2	M4	R1	2	-
92	2	N4	T2	4	-
93	2	P5	T3	2	-
94	2	P4	T1	1	VREF
95	2	U2	R4	√	-
96	2	U3	T5	2	-
97	2	T4	V2	1	-
98	2	U5	V3	√	D3
99	2	V1	V5	√	-
100	2	W2	V4	5	-
101	2	W5	W1	2	-
102	2	Y2	W4	√	VREF
103	2	Y1	Y5	√	-
104	2	AA1	Y4	2	VREF
105	2	AA4	AA2	√	-
106	3	AB3	AC4	2	VREF
107	3	AB1	AC5	√	-
108	3	AD4	AC3	√	VREF
109	3	AC1	AD5	2	-
110	3	AE4	AD3	5	-
111	3	AE5	AD2	√	-
112	3	AE1	AF5	√	VREF
113	3	AE2	AG4	1	-
114	3	AG5	AF1	2	-
115	3	AH4	AF2	√	-
116	3	AF3	AJ4	1	VREF
117	3	AG1	AJ5	2	-
118	3	AG2	AK4	4	-
119	3	AG3	AL4	2	-

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_VREF_L265N_Y	AJ3
6	IO_L265P_Y	AG5
6	IO_L266N_YY	AD9[4]
6	IO_L266P_YY	AJ2[5]
6	IO_L267N_YY	AC10
6	IO_L267P_YY	AH2
6	IO_L268N_Y	AH3
6	IO_L268P_Y	AF5
6	IO_L269N_Y	AE8[4]
6	IO_L269P_Y	AG3[5]
6	IO_L270N_Y	AE7
6	IO_L270P_Y	AG2
6	IO_VREF_L271N_YY	AF6
6	IO_L271P_YY	AG1
6	IO_L272N_YY	AC9[4]
6	IO_L272P_YY	AG4[5]
6	IO_L273N_YY	AE6
6	IO_L273P_YY	AF3
6	IO_VREF_L274N_Y	AF1[2]
6	IO_L274P_Y	AF4
6	IO_L275N	AB10[4]
6	IO_L275P	AF2[5]
6	IO_L276N_Y	AC8
6	IO_L276P_Y	AE1
6	IO_VREF_L277N_YY	AD5
6	IO_L277P_YY	AE3
6	IO_L278N_YY	AC7
6	IO_L278P_YY	AD1
6	IO_L279N_Y	AD6
6	IO_L279P_Y	AD2
6	IO_VREF_L280N_YY	AB8
6	IO_L280P_YY	AC1
6	IO_L281N_YY	AC5
6	IO_L281P_YY	AC2

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
6	IO_L282N_Y	AA9
6	IO_L282P_Y	AC3
6	IO_L283N_Y	AC4
6	IO_L283P_Y	AD4
6	IO_L284N_Y	AA8
6	IO_L284P_Y	AB6
6	IO_L285N	AB1
6	IO_L285P	Y10
6	IO_L286N_Y	AB2
6	IO_L286P_Y	AA7
6	IO_VREF_L287N_Y	AA4
6	IO_L287P_Y	AA1
6	IO_L288N_YY	Y9[4]
6	IO_L288P_YY	AB4[5]
6	IO_L289N_YY	AA2
6	IO_L289P_YY	Y8
6	IO_L290N_Y	AA6
6	IO_L290P_Y	AA5
6	IO_L291N_Y	AB3[4]
6	IO_L291P_Y	Y7[5]
6	IO_L292N_Y	Y1
6	IO_L292P_Y	W10
6	IO_VREF_L293N_YY	Y5
6	IO_L293P_YY	Y2
6	IO_L294N_YY	W9[4]
6	IO_L294P_YY	W2[5]
6	IO_L295N_YY	W7
6	IO_L295P_YY	Y4
6	IO_L296N_Y	W1
6	IO_L296P_Y	Y6
6	IO_L297N_Y	W6[4]
6	IO_L297P_Y	W3[5]
6	IO_L298N_Y	V9
6	IO_L298P_Y	W4

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16