AMD Xilinx - XCV100E-6FG256C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	176
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-6fg256c

resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex-E (-7)
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Virtex-E Device/Package Combinations and Maximum I/O

Table 3: **Virtex-E Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

	XCV 50E	XCV 100E	XCV 200E	XCV 300E	XCV 400E	XCV 600E	XCV 1000E	XCV 1600E	XCV 2000E	XCV 2600E	XCV 3200E
CS144	94	94	94								
PQ240	158	158	158	158	158						
HQ240						158	158				
BG352		196	260	260							
BG432				316	316	316					
BG560					404	404	404	404	404		
FG256	176	176	176	176							
FG456			284	312							
FG676					404	444					
FG680						512	512	512	512		
FG860							660	660	660		
FG900						512	660	700			
FG1156							660	724	804	804	804

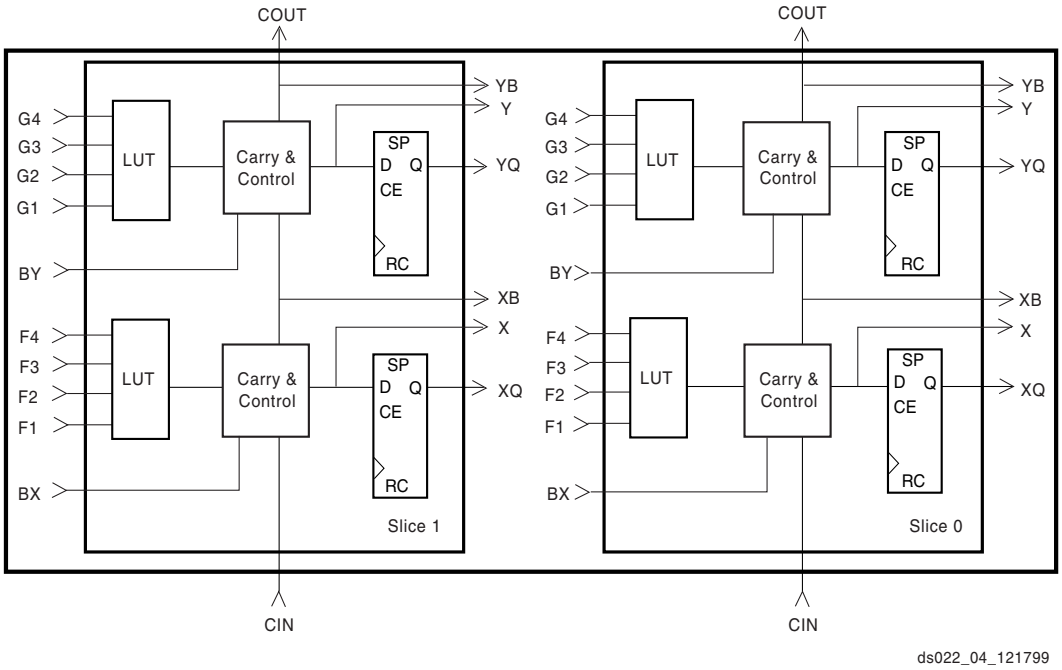

Figure 4: **2-Slice Virtex-E CLB**

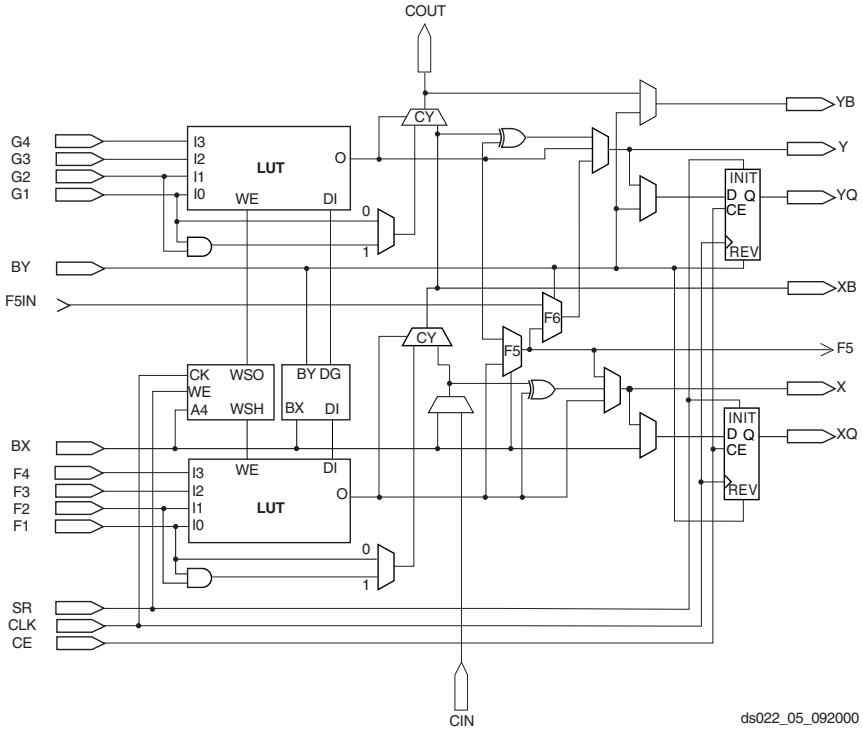

Figure 5: **Detailed View of Virtex-E Slice**

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR

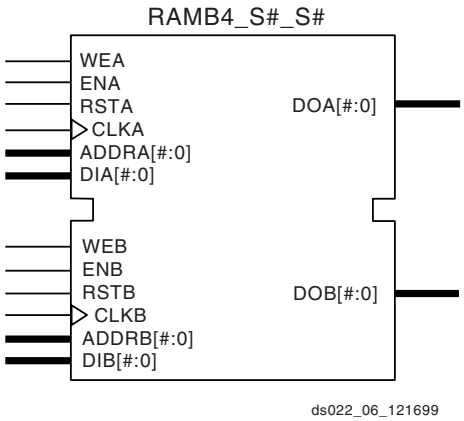

Figure 6: **Dual-Port Block SelectRAM**

Table 5 shows the depth and width aspect ratios for the block SelectRAM. The Virtex-E block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAMs. Refer to XAPP130 for block SelectRAM timing waveforms.

Table 5: **Block SelectRAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex-E routing architecture and its place-and-route software were defined in a joint optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources (see Figure 7), providing three types of connections:

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

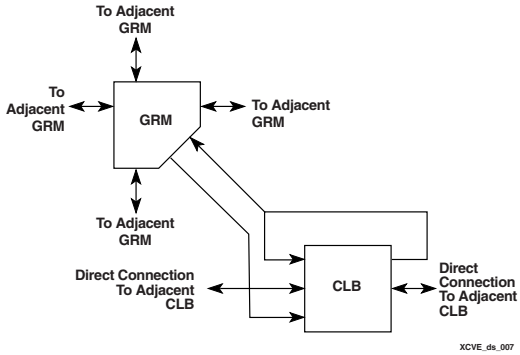

Figure 7: **Virtex-E Local Routing**

General Purpose Routing

Most Virtex-E signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. General-purpose routing resources are located in horizontal and vertical routing channels associated with the CLB rows and columns and are as follows:

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines are driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex-E devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

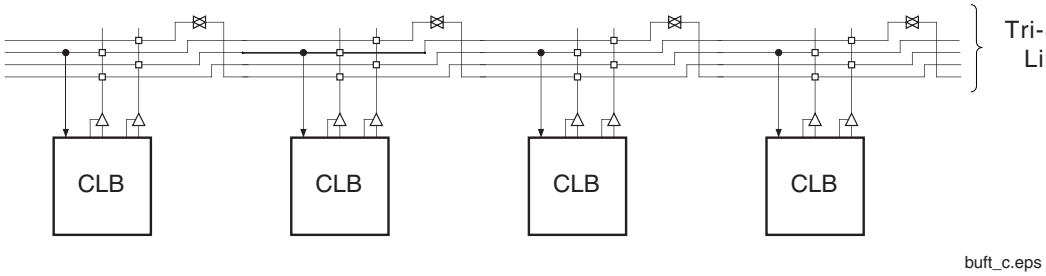

Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

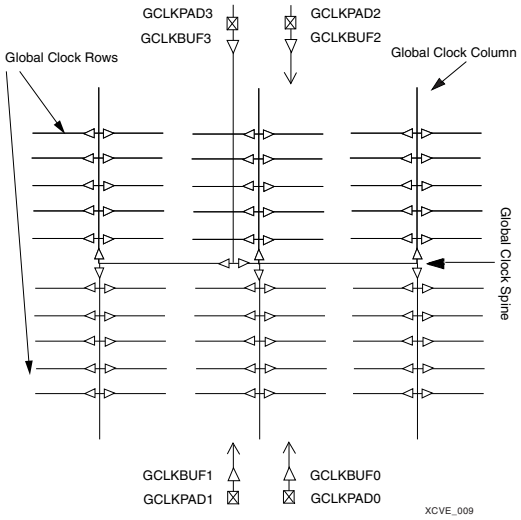

Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

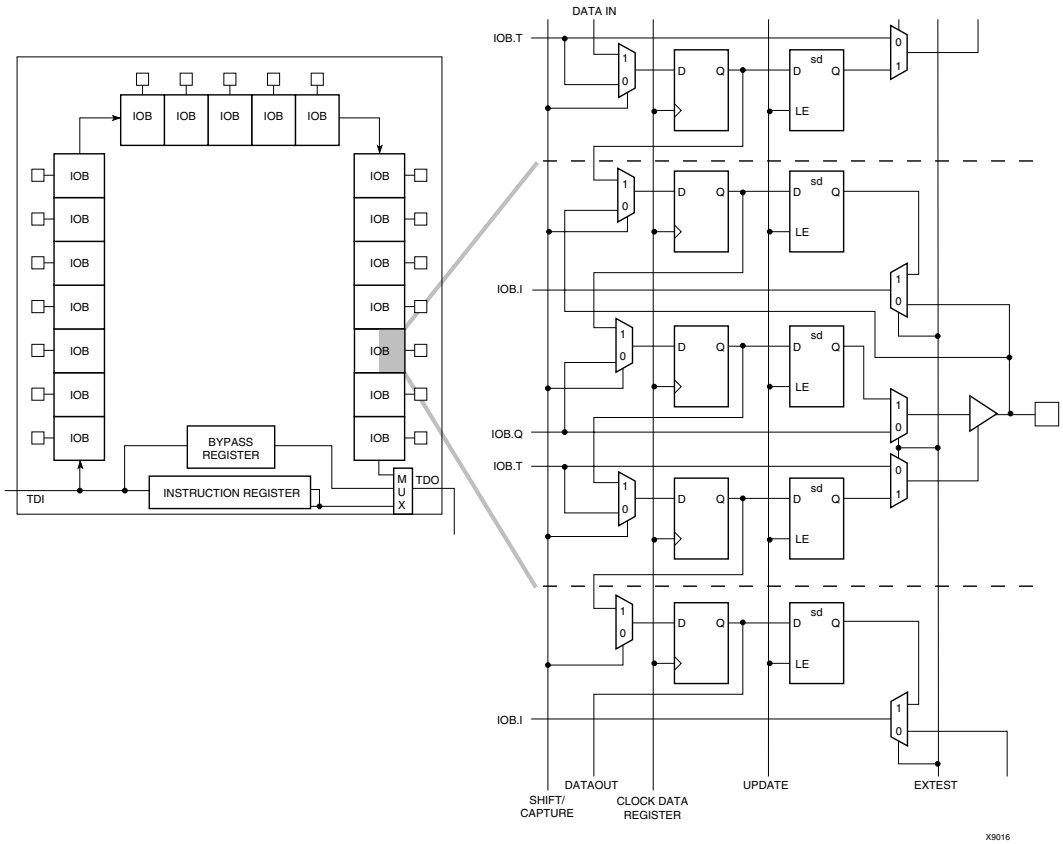

Figure 11: **Virtex-E Family Boundary Scan Logic**

Instruction Set

The Virtex-E series Boundary Scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6..

Table 6: **Boundary Scan Instructions**

Boundary Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables Boundary Scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables Boundary Scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.

Table 6: **Boundary Scan Instructions *(Continued)***

Boundary Scan Command	Binary Code(4:0)	Description
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables Boundary Scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	3-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0V. The fastest ramp rate is 0V to nominal voltage in 2 ms, and the slowest allowed ramp rate is 0V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description(2)	Current Requirement(3)
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Note: Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under **LVPECL**, with a 100 Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P210	GCK2	1
P209	IO_LVDS_DLL_L6P	1
P208	IO_VREF	1
P207	VCCO	1
P206	IO_L7N_Y	1
P205	IO_VREF_L7P_Y	1
P204	GND	NA
P203	IO_L8N_Y	1
P202	IO_L8P_Y	1
P201[1]	IO_VREF	1
P200	IO_L9N_YY	1
P199	IO_L9P_YY	1
P198	VCCINT	NA
P197	VCCO	1
P196	GND	NA
P195	IO_L10N_YY	1
P194	IO_VREF_L10P_YY	1
P193	IO_VREF	1
P192	IO_L11N_YY	1
P191	IO_VREF_L11P_YY	1
P190	GND	NA
P189	IO_L12N_YY	1
P188	IO_L12P_YY	1
P187	IO_VREF_L13N	1
P186	IO_L13P	1
P185	IO_WRITE_L14N_YY	1
P184	IO_CS_L14P_YY	1
P183	TDI	NA
P182	GND	NA
P181	TDO	2
P180	VCCO	1
P179	CCLK	2
P178	IO_DOUT_BUSY_L15P_YY	2
P177	IO_DIN_D0_L15N_YY	2
P176	VCCO	2
P175	IO_VREF	2

Table 8: **HQ240 — XCV600E, XCV1000E**

Pin #	Pin Description	Bank
P174	IO_L16P_Y	2
P173	IO_L16N_Y	2
P172	GND	NA
P171	IO_VREF_L17P_Y	2
P170	IO_L17N_Y	2
P169	IO_VREF	2
P168	IO_VREF_L18P_Y	2
P167	IO_D1_L18N_Y	2
P166	GND	NA
P165	VCCO	2
P164	VCCINT	NA
P163	IO_D2_L19P_YY	2
P162	IO_L19N_YY	2
P161[1]	IO_VREF	2
P160	IO_L20P_Y	2
P159	IO_L20N_Y	2
P158	GND	NA
P157	IO_VREF_L21P_Y	2
P156	IO_D3_L21N_Y	2
P155	IO_L22P_Y	2
P154	IO_VREF_L22N_Y	2
P153	IO_L23P_YY	2
P152	IO_L23N_YY	2
P151	GND	NA
P150	VCCO	2
P149	IO	3
P148	VCCINT	NA
P147	IO_VREF	3
P146	VCCO	3
P145	IO_D4_L24P_Y	3
P144	IO_VREF_L24N_Y	3
P143	GND	NA
P142	IO_L25P_Y	3
P141	IO_L25N_Y	3
P140[1]	IO_VREF	3
P139	IO_L26P_YY	3

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
7	IO_L132P_Y	G28
7	IO_L133N	E31
7	IO_L133P	E30
7	IO_L134N_Y	F29
7	IO_VREF_L134P_Y	F28
7	IO_L135N_Y	D31
7	IO_L135P_Y	D30
7	IO_L136N	E29
7	IO_L136P	E28
2	CCLK	D4
3	DONE	AH4
NA	DXN	AH27
NA	DXP	AK29
NA	M0	AH28
NA	M1	AH29
NA	M2	AJ28
NA	PROGRAM	AH3
NA	TCK	D28
NA	TDI	B3
2	TDO	C4
NA	TMS	D29
NA	VCCINT	A10
NA	VCCINT	A17
NA	VCCINT	B23
NA	VCCINT	B26
NA	VCCINT	C7
NA	VCCINT	C14
NA	VCCINT	C19
NA	VCCINT	F1
NA	VCCINT	F30
NA	VCCINT	K3
NA	VCCINT	K29
NA	VCCINT	N2
NA	VCCINT	N29

Table 12: **BG432 — XCV300E, XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	VCCINT	T1
NA	VCCINT	T29
NA	VCCINT	W2
NA	VCCINT	W31
NA	VCCINT	AB2
NA	VCCINT	AB30
NA	VCCINT	AE29
NA	VCCINT	AF1
NA	VCCINT	AH8
NA	VCCINT	AH24
NA	VCCINT	AJ10
NA	VCCINT	AJ16
NA	VCCINT	AK22
NA	VCCINT	AK13
NA	VCCINT	AK19
0	VCCO	A21
0	VCCO	C29
0	VCCO	D21
1	VCCO	A1
1	VCCO	A11
1	VCCO	D11
2	VCCO	C3
2	VCCO	L4
2	VCCO	L1
3	VCCO	AA1
3	VCCO	AA4
3	VCCO	AJ3
4	VCCO	AH11
4	VCCO	AL1
4	VCCO	AL11
5	VCCO	AH21
5	VCCO	AL21
5	VCCO	AJ29
6	VCCO	AA28
6	VCCO	AA31

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
1	IO_L43N_Y	C5	
1	IO_VREF_L43P_Y	E7	3
1	IO_WRITE_L44N_YY	D6	
1	IO_CS_L44P_YY	A2	
2	IO	D3	
2	IO	F3	
2	IO	G1	
2	IO	J2	
2	IO_DOUT_BUSY_L45P_YY	D4	
2	IO_DIN_D0_L45N_YY	E4	
2	IO_L46P_Y	F5	
2	IO_VREF_L46N_Y	B3	3
2	IO_L47P_Y	F4	
2	IO_L47N_Y	C1	
2	IO_VREF_L48P_Y	G5	
2	IO_L48N_Y	E3	
2	IO_L49P_Y	D2	
2	IO_L49N_Y	G4	
2	IO_L50P_Y	H5	
2	IO_L50N_Y	E2	
2	IO_VREF_L51P_YY	H4	
2	IO_L51N_YY	G3	
2	IO_L52P_Y	J5	
2	IO_VREF_L52N_Y	F1	1
2	IO_L53P_Y	J4	
2	IO_L53N_Y	H3	
2	IO_VREF_L54P_Y	K5	4
2	IO_L54N_Y	H2	
2	IO_L55P_Y	J3	
2	IO_L55N_Y	K4	
2	IO_VREF_L56P_YY	L5	
2	IO_D1_L56N_YY	K3	
2	IO_D2_L57P_YY	L4	
2	IO_L57N_YY	K2	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	IO_L58P_Y	M5	
2	IO_L58N_Y	L3	
2	IO_L59P_Y	L1	
2	IO_L59N_Y	M4	
2	IO_VREF_L60P_Y	N5	3
2	IO_L60N_Y	M2	
2	IO_L61P_Y	N4	
2	IO_L61N_Y	N3	
2	IO_L62P_Y	N2	
2	IO_L62N_Y	P5	
2	IO_VREF_L63P_YY	P4	
2	IO_D3_L63N_YY	P3	
2	IO_L64P_Y	P2	
2	IO_L64N_Y	R5	
2	IO_L65P_Y	R4	
2	IO_L65N_Y	R3	
2	IO_VREF_L66P_Y	R1	
2	IO_L66N_Y	T4	
2	IO_L67P_Y	T5	
2	IO_VREF_L67N_Y	T3	2
2	IO_L68P_YY	T2	
2	IO_L68N_YY	U3	
3	IO	AE3	
3	IO	AF3	
3	IO	AH3	
3	IO	AK3	
3	IO_VREF_L69P_Y	U1	2
3	IO_L69N_Y	U2	
3	IO_L70P_Y	V2	
3	IO_VREF_L70N_Y	V4	
3	IO_L71P_Y	V5	
3	IO_L71N_Y	V3	
3	IO_L72P_Y	W1	
3	IO_L72N_Y	W3	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_L165N_YY	P32	
7	IO_VREF_L165P_YY	P31	
7	IO_L166N_Y	P30	
7	IO_L166P_Y	P29	
7	IO_L167N_Y	M32	
7	IO_L167P_Y	N31	
7	IO_L168N_Y	N30	
7	IO_VREF_L168P_Y	L33	3
7	IO_L169N_Y	M31	
7	IO_L169P_Y	L32	
7	IO_L170N_Y	M30	
7	IO_L170P_Y	L31	
7	IO_L171N_YY	M29	
7	IO_L171P_YY	J33	
7	IO_L172N_YY	L30	
7	IO_VREF_L172P_YY	K31	
7	IO_L173N_Y	L29	
7	IO_L173P_Y	H33	
7	IO_L174N_Y	J31	
7	IO_VREF_L174P_Y	H32	4
7	IO_L175N_Y	K29	
7	IO_L175P_Y	H31	
7	IO_L176N_Y	J30	
7	IO_VREF_L176P_Y	G32	1
7	IO_L177N_YY	J29	
7	IO_VREF_L177P_YY	G31	
7	IO_L178N_Y	E33	
7	IO_L178P_Y	E32	
7	IO_L179N_Y	H29	
7	IO_L179P_Y	F31	
7	IO_L180N_Y	D32	
7	IO_VREF_L180P_Y	E31	
7	IO_L181N_Y	G29	
7	IO_L181P_Y	C33	
7	IO_L182N_Y	F30	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
7	IO_VREF_L182P_Y	D31	3
2	CCLK	C4	
3	DONE	AJ5	
NA	DXN	AK29	
NA	DXP	AJ28	
NA	M0	AJ29	
NA	M1	AK30	
NA	M2	AN32	
NA	PROGRAM	AM1	
NA	TCK	E29	
NA	TDI	D5	
2	TDO	E6	
NA	TMS	B33	
NA	NC	C31	
NA	NC	AC2	
NA	NC	AK4	
NA	NC	AL3	
NA	VCCINT	A21	
NA	VCCINT	B12	
NA	VCCINT	B14	
NA	VCCINT	B18	
NA	VCCINT	B28	
NA	VCCINT	C22	
NA	VCCINT	C24	
NA	VCCINT	E9	
NA	VCCINT	E12	
NA	VCCINT	F2	
NA	VCCINT	H30	
NA	VCCINT	J1	
NA	VCCINT	K32	
NA	VCCINT	M3	
NA	VCCINT	N1	

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
4	IO_L43P_Y	P12
4	IO_VREF_L43N_Y	R13[2]
4	IO_L44P_YY	N12
4	IO_L44N_YY	T13
4	IO_VREF_L45P_YY	T12
4	IO_L45N_YY	P11
4	IO_L46P_Y	R12
4	IO_L46N_Y	N11
4	IO_VREF_L47P_YY	T11[1]
4	IO_L47N_YY	M11
4	IO_L48P_YY	R11
4	IO_L48N_YY	T10
4	IO_L49P_Y	R10
4	IO_L49N_Y	M10
4	IO_VREF_L50P_Y	P9
4	IO_L50N_Y	T9
4	IO_L51P_Y	N10
4	IO_L51N_Y	R9
4	IO_LVDS_DLL_L52P	N9
5	GCK1	R8
5	IO	N7
5	IO	T7
5	IO_LVDS_DLL_L52N	T8
5	IO_L53P_Y	R7
5	IO_VREF_L53N_Y	P8
5	IO_L54P_Y	P7
5	IO_L54N_Y	T6
5	IO_L55P_YY	M7
5	IO_L55N_YY	R6
5	IO_L56P_YY	P6
5	IO_VREF_L56N_YY	R5[1]
5	IO_L57P_Y	N6
5	IO_L57N_Y	T5
5	IO_L58P_YY	M6

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
5	IO_VREF_L58N_YY	T4
5	IO_L59P_YY	T3
5	IO_L59N_YY	P5
5	IO_VREF_L60P_Y	T2[2]
5	IO_L60N_Y	N5
6	IO_L61N_YY	M3
6	IO_L61P_YY	R1
6	IO_L62N	M4
6	IO_VREF_L62P	N2[2]
6	IO_L63N_YY	L5
6	IO_L63P_YY	P1
6	IO_VREF_L64N_Y	N1
6	IO_L64P_Y	L3
6	IO_L65N	M2
6	IO_L65P	L4
6	IO_VREF_L66N_Y	M1[1]
6	IO_L66P_Y	K4
6	IO_L67N_YY	L2
6	IO_L67P_YY	L1
6	IO_L68N	K3
6	IO_L68P	K1
6	IO_L69N_YY	K2
6	IO_L69P_YY	K5
6	IO_VREF_L70N_Y	J3
6	IO_L70P_Y	J1
6	IO_L71N	J4
6	IO_L71P	H1
6	IO	J2
7	IO	C2
7	IO_L72N_YY	G1
7	IO_L72P_YY	H4
7	IO_L73N	G5
7	IO_L73P	H2

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	VREF
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	1	VREF
83	3	Y25	V21	2	-
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF

Table 21: **FG676 Differential Pin Pair Summary XCV400E, XCV600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
86	3	AA24	Y23	1	-
87	3	AB26	W21	2	-
88	3	Y22	W22	1	VREF
89	3	AA23	AB24	2	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	1	-
101	4	AF20	AB18	1	VREF
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	1	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	1	-
113	4	AF15	Y14	1	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	1	VREF
117	5	AC13	W13	1	-
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF

Table 22: **FG680 - XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
3	IO_L97N	AA2
3	IO_L98P_YY	AC5
3	IO_L98N_YY	AB1
3	IO_D4_L99P_YY	AD3
3	IO_VREF_L99N_YY	AC1
3	IO_L100P_Y	AD1
3	IO_L100N_Y	AD4
3	IO_L101P	AD2
3	IO_L101N	AE3
3	IO_L102P_YY	AE1
3	IO_L102N_YY	AE4
3	IO_L103P_Y	AE2
3	IO_VREF_L103N_Y	AF3[1]
3	IO_L104P	AF4
3	IO_L104N	AF1
3	IO_L105P	AG3
3	IO_L105N	AF2
3	IO_L106P_Y	AG4
3	IO_L106N_Y	AG1
3	IO_L107P_YY	AH3
3	IO_D5_L107N_YY	AG2
3	IO_D6_L108P_YY	AH1
3	IO_VREF_L108N_YY	AJ2
3	IO_L109P	AH2
3	IO_L109N	AJ3
3	IO_L110P_YY	AJ1
3	IO_L110N_YY	AJ4
3	IO_L111P_YY	AK1
3	IO_VREF_L111N_YY	AK3
3	IO_L112P	AK2
3	IO_L112N	AK4
3	IO_L113P	AL1
3	IO_VREF_L113N	AL2[3]
3	IO_L114P_YY	AM1
3	IO_L114N_YY	AL3
3	IO_L115P_YY	AM2
3	IO_VREF_L115N_YY	AL4
3	IO_L116P_Y	AM3
3	IO_L116N_Y	AN1
3	IO_L117P	AM4
3	IO_L117N	AP1
3	IO_L118P_YY	AN2
3	IO_L118N_YY	AP2
3	IO_L119P_Y	AN3
3	IO_VREF_L119N_Y	AR1
3	IO_L120P	AN4
3	IO_L120N	AT1
3	IO_L121P	AR2
3	IO_VREF_L121N	AP4[1]
3	IO_L122P_Y	AT2
3	IO_L122N_Y	AR3
3	IO_D7_L123P_YY	AR4
3	IO_INIT_L123N_YY	AU2
4	GCK0	AW19
4	IO	AV3
4	IO_L124P_YY	AU4
4	IO_L124N_YY	AV5
4	IO_L125P_Y	AT6
4	IO_L125N_Y	AV4
4	IO_VREF_L126P_Y	AU6[1]
4	IO_L126N_Y	AW4
4	IO_L127P_YY	AT7
4	IO_L127N_YY	AW5
4	IO_VREF_L128P_YY	AU7
4	IO_L128N_YY	AV6
4	IO_L129P_Y	AT8
4	IO_L129N_Y	AW6
4	IO_L130P_Y	AU8
4	IO_L130N_Y	AV7
4	IO_L131P_YY	AT9
4	IO_L131N_YY	AW7

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
120	3	AN4	AT1	4	-
121	3	AR2	AP4	4	VREF
122	3	AT2	AR3	6	-
123	3	AR4	AU2	√	INIT
124	4	AU4	AV5	√	-
125	4	AT6	AV4	5	-
126	4	AU6	AW4	5	VREF
127	4	AT7	AW5	√	-
128	4	AU7	AV6	√	VREF
129	4	AT8	AW6	3	-
130	4	AU8	AV7	3	-
131	4	AT9	AW7	√	-
132	4	AV8	AU9	√	VREF
133	4	AW8	AT10	5	-
134	4	AV9	AU10	5	VREF
135	4	AW9	AT11	√	-
136	4	AV10	AU11	√	VREF
137	4	AW10	AU12	2	-
138	4	AV11	AT13	2	-
139	4	AW11	AU13	√	VREF
140	4	AT14	AV12	√	-
141	4	AU14	AW12	5	-
142	4	AT15	AV13	5	-
143	4	AU15	AW13	√	-
144	4	AV14	AT16	√	VREF
145	4	AW14	AU16	3	-
146	4	AV15	AR17	3	-
147	4	AW15	AT17	√	-
148	4	AU17	AV16	√	VREF
149	4	AR18	AW16	5	-
150	4	AT18	AV17	5	-
151	4	AU18	AW17	√	-
152	4	AT19	AV18	√	VREF
153	4	AU19	AW18	2	-

Table 23: **FG680 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E, XCV2000E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
154	4	AU21	AV19	2	VREF
155	5	AT21	AT22	NA	IO_LVDS_DLL
156	5	AV20	AR22	8	VREF
157	5	AV23	AW21	√	VREF
158	5	AU23	AV21	√	-
159	5	AT23	AW22	5	-
160	5	AR23	AV22	5	-
161	5	AV24	AW23	√	VREF
162	5	AW24	AU24	√	-
163	5	AW25	AT24	3	-
164	5	AV25	AU25	3	-
165	5	AW26	AT25	√	VREF
166	5	AV26	AW27	√	-
167	5	AU26	AV27	5	-
168	5	AT26	AW28	5	-
169	5	AU27	AV28	√	-
170	5	AW29	AT27	√	VREF
171	5	AW30	AU28	2	-
172	5	AV30	AV29	2	-
173	5	AW31	AU29	√	VREF
174	5	AV31	AT29	√	-
175	5	AW32	AU30	5	VREF
176	5	AW33	AT30	5	-
177	5	AV33	AU31	√	VREF
178	5	AT31	AW34	√	-
179	5	AV32	AV34	3	-
180	5	AU32	AW35	3	-
181	5	AT32	AV35	√	VREF
182	5	AU33	AW36	√	-
183	5	AT33	AV36	5	VREF
184	5	AU34	AU36	5	-
185	6	AT38	AR36	√	-
186	6	AP36	AR38	6	-
187	6	AP37	AT39	4	VREF

FG860 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 24, see Table 25 for Differential Pair information.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	GCK3	C22
0	IO	A26
0	IO	B31
0	IO	B34
0	IO	C24
0	IO	C29
0	IO	C34
0	IO	D24
0	IO	D36
0	IO	D40
0	IO	E26
0	IO	E28
0	IO	E35
0	IO_L0N_Y	A38
0	IO_L0P_Y	D38
0	IO_L1N_Y	B37
0	IO_L1P_Y	E37
0	IO_VREF_L2N_Y	A37
0	IO_L2P_Y	C39
0	IO_L3N_Y	B36
0	IO_L3P_Y	C38
0	IO_L4N_YY	A36
0	IO_L4P_YY	B35
0	IO_VREF_L5N_YY	A35
0	IO_L5P_YY	D37
0	IO_L6N_Y	C37
0	IO_L6P_Y	A34
0	IO_L7N_Y	E36
0	IO_L7P_Y	B33
0	IO_L8N_YY	A33
0	IO_L8P_YY	C32
0	IO_VREF_L9N_YY	C36
0	IO_L9P_YY	B32
0	IO_L10N_Y	A32
0	IO_L10P_Y	D35
0	IO_VREF_L11N_Y	C31[2]
0	IO_L11P_Y	C35
0	IO_L12N_YY	E34
0	IO_L12P_YY	A31
0	IO_VREF_L13N_YY	D34
0	IO_L13P_YY	C30
0	IO_L14N_Y	B30
0	IO_L14P_Y	E33
0	IO_L15N_Y	A30
0	IO_L15P_Y	D33
0	IO_VREF_L16N_YY	C33
0	IO_L16P_YY	B29
0	IO_L17N_YY	E32
0	IO_L17P_YY	A29
0	IO_L18N_Y	D32
0	IO_L18P_Y	C28
0	IO_L19N_Y	E31
0	IO_L19P_Y	B28
0	IO_L20N_Y	D31
0	IO_L20P_Y	A28
0	IO_L21N_Y	D30
0	IO_L21P_Y	C27
0	IO_L22N_YY	E29
0	IO_L22P_YY	B27
0	IO_VREF_L23N_YY	D29
0	IO_L23P_YY	A27
0	IO_L24N_Y	C26
0	IO_L24P_Y	D28
0	IO_L25N_Y	B26
0	IO_L25P_Y	F27
0	IO_L26N_YY	E27
0	IO_L26P_YY	C25

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO	AJ40
6	IO	AL41
6	IO	AN38
6	IO	AN42
6	IO	AP41
6	IO	AR39
6	IO_L211N_YY	AV41
6	IO_L211P_YY	AV42
6	IO_L212N_Y	AW40
6	IO_L212P_Y	AU41
6	IO_L213N_Y	AV39
6	IO_L213P_Y	AU42
6	IO_VREF_L214N_Y	AT41
6	IO_L214P_Y	AU38
6	IO_L215N	AT42
6	IO_L215P	AV40
6	IO_L216N_Y	AR41
6	IO_L216P_Y	AU39
6	IO_VREF_L217N_Y	AR42
6	IO_L217P_Y	AU40
6	IO_L218N_YY	AT38
6	IO_L218P_YY	AP42
6	IO_L219N_Y	AN41
6	IO_L219P_Y	AT39
6	IO_L220N_Y	AT40
6	IO_L220P_Y	AM40
6	IO_VREF_L221N_YY	AR38
6	IO_L221P_YY	AM41
6	IO_L222N_YY	AM42
6	IO_L222P_YY	AR40
6	IO_VREF_L223N_Y	AL40[2]
6	IO_L223P_Y	AP38
6	IO_L224N_Y	AP39
6	IO_L224P_Y	AL42
6	IO_VREF_L225N_YY	AP40
6	IO_L225P_YY	AK40
6	IO_L226N_YY	AK41

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
6	IO_L226P_YY	AN39
6	IO_L227N_Y	AK42
6	IO_L227P_Y	AN40
6	IO_VREF_L228N_YY	AM38
6	IO_L228P_YY	AJ41
6	IO_L229N_YY	AJ42
6	IO_L229P_YY	AM39
6	IO_L230N_Y	AH40
6	IO_L230P_Y	AH41
6	IO_L231N_Y	AL38
6	IO_L231P_Y	AH42
6	IO_L232N_Y	AL39
6	IO_L232P_Y	AG41
6	IO_L233N	AK39
6	IO_L233P	AG40
6	IO_L234N_Y	AJ38
6	IO_L234P_Y	AG42
6	IO_VREF_L235N_Y	AF42
6	IO_L235P_Y	AJ39
6	IO_L236N_YY	AF41
6	IO_L236P_YY	AH38
6	IO_L237N_Y	AE42
6	IO_L237P_Y	AH39
6	IO_L238N_Y	AG38
6	IO_L238P_Y	AE41
6	IO_VREF_L239N_YY	AG39
6	IO_L239P_YY	AD42
6	IO_L240N_YY	AD40
6	IO_L240P_YY	AF39
6	IO_L241N_Y	AD41
6	IO_L241P_Y	AE38
6	IO_L242N_Y	AE39
6	IO_L242P_Y	AC40
6	IO_VREF_L243N_YY	AD38
6	IO_L243P_YY	AC41
6	IO_L244N_YY	AB42
6	IO_L244P_YY	AC38

Table 27: **FG900 Differential Pin Pair Summary XCV600E, XCV1000E, XCV1600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
256	7	N6	M6	1	-
257	7	N1	N5	4	-
258	7	M5	M4	√	-
259	7	M1	M2	1	VREF
260	7	L2	L4	4	-
261	7	L5	M7	3	-
262	7	M8	L1	4	-
263	7	M9	K2	1	-
264	7	M10	L3	NA	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	4	-
268	7	J5	L8	4	-
269	7	H4	K6	4	VREF
270	7	K7	H1	4	-
271	7	J2	J7	2	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	1	-
275	7	E1	G3	4	-
276	7	E2	H6	√	-
277	7	K9	E4	1	VREF
278	7	F4	J8	4	-
279	7	H7	D1	3	-
280	7	C2	G6	4	VREF
281	7	F5	D2	1	-
282	7	K10	D3	4	-

Notes:
1. AO in the XCV600E, 1000E.
2. AO in the XCV1000E.
3. AO in the XCV1600E.
4. AO in the XCV1000E, XCV1600E.

FG1156 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, XCV2000E, XCV2600E, and XCV3200E devices in the FG1156 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled IO_VREF can be used as either V_{REF} or general I/O, unless indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 28, see Table 29 for Differential Pair information.

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	GCK3	E17
0	IO	B4
0	IO	B9
0	IO	B10
0	IO	D9[3]
0	IO	D16
0	IO	E7[3]
0	IO	E11[3]
0	IO	E13[3]
0	IO	E16[3]
0	IO	F17[3]
0	IO	J12[3]
0	IO	J13[3]
0	IO	J14[3]
0	IO	K11[3]
0	IO_L0N_Y	F7
0	IO_L0P_Y	H9
0	IO_L1N_Y	C5
0	IO_L1P_Y	J10
0	IO_VREF_L2N_Y	E6
0	IO_L2P_Y	D6
0	IO_L3N_Y	A4
0	IO_L3P_Y	G8
0	IO_L4N_YY	C6
0	IO_L4P_YY	J11
0	IO_VREF_L5N_YY	G9
0	IO_L5P_YY	F8
0	IO_L6N_YY	A5[4]

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L6P_YY	H10[5]
0	IO_L7N_Y	D7
0	IO_L7P_Y	B5
0	IO_L8N_Y	K12
0	IO_L8P_Y	E8
0	IO_L9N	B6[4]
0	IO_L9P	F9[5]
0	IO_L10N_YY	G10
0	IO_L10P_YY	C7
0	IO_VREF_L11N_YY	D8
0	IO_L11P_YY	B7
0	IO_L12N	H11[4]
0	IO_L12P	C8[5]
0	IO_L13N_Y	E9
0	IO_L13P_Y	B8
0	IO_VREF_L14N_Y	K13[2]
0	IO_L14P_Y	G11
0	IO_L15N	A8[4]
0	IO_L15P	F10[5]
0	IO_L16N_YY	C9
0	IO_L16P_YY	H12
0	IO_VREF_L17N_YY	D10
0	IO_L17P_YY	A9
0	IO_L18N_Y	F11
0	IO_L18P_Y	A10
0	IO_L19N_Y	K14
0	IO_L19P_Y	C10
0	IO_VREF_L20N_YY	H13
0	IO_L20P_YY	G12
0	IO_L21N_YY	A11
0	IO_L21P_YY	B11
0	IO_L22N_Y	E12
0	IO_L22P_Y	D11
0	IO_L23N_Y	G13

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
0	IO_L23P_Y	C12
0	IO_L24N_Y	K15
0	IO_L24P_Y	A12
0	IO_L25N_Y	B12
0	IO_L25P_Y	H14
0	IO_L26N_YY	D12
0	IO_L26P_YY	F13
0	IO_VREF_L27N_YY	A13
0	IO_L27P_YY	B13
0	IO_L28N_YY	J15[4]
0	IO_L28P_YY	G14[5]
0	IO_L29N_Y	C13
0	IO_L29P_Y	F14
0	IO_L30N_Y	H15
0	IO_L30P_Y	D13
0	IO_L31N	A14[4]
0	IO_L31P	K16[5]
0	IO_L32N_YY	E14
0	IO_L32P_YY	B14
0	IO_VREF_L33N_YY	G15
0	IO_L33P_YY	D14
0	IO_L34N	J16[4]
0	IO_L34P	D15[5]
0	IO_L35N_Y	F15
0	IO_L35P_Y	B15
0	IO_L36N_Y	A15
0	IO_L36P_Y	E15
0	IO_L37N	G16[4]
0	IO_L37P	A16[5]
0	IO_L38N_YY	F16
0	IO_L38P_YY	J17
0	IO_VREF_L39N_YY	C16
0	IO_L39P_YY	B16
0	IO_L40N_Y	H17

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_L324P_Y	L4
7	IO_L325N_YY	J1
7	IO_L325P_YY	L5
7	IO_L326N_YY	J2
7	IO_VREF_L326P_YY	K3
7	IO_L327N_Y	L7
7	IO_L327P_Y	J3
7	IO_L328N_Y	M9[5]
7	IO_L328P_Y	H2[4]
7	IO_L329N_Y	J4
7	IO_VREF_L329P_Y	K6[2]
7	IO_L330N_YY	L8
7	IO_L330P_YY	G2
7	IO_L331N_YY	H3[5]
7	IO_L331P_YY	K7[4]
7	IO_L332N_YY	G3
7	IO_VREF_L332P_YY	J5
7	IO_L333N_Y	L9
7	IO_L333P_Y	H5
7	IO_L334N_Y	J6[5]
7	IO_L334P_Y	H4[4]
7	IO_L335N_Y	G4
7	IO_L335P_Y	K8
7	IO_L336N_YY	J7
7	IO_L336P_YY	F2
7	IO_L337N_YY	F3[5]
7	IO_L337P_YY	L10[4]
7	IO_L338N_Y	E1
7	IO_VREF_L338P_Y_Y	H6
7	IO_L339N_Y	G5
7	IO_L339P_Y	E2
7	IO_L340N	K9
7	IO_L340P	D1
7	IO_L341N_Y	E3

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
7	IO_VREF_L341P_Y	J8
7	IO_L342N_Y	E4
7	IO_L342P_Y	D2
7	IO_L343N_Y	F4
7	IO_L343P_Y	D3
2	CCLK	C31
3	DONE	AM31
NA	DXN	AJ5
NA	DXP	AL5
NA	M0	AK4
NA	M1	AG7
NA	M2	AL3
NA	PROGRAM	AG28
NA	TCK	D5
NA	TDI	C30
2	TDO	K26
NA	TMS	C4
NA	VCCINT	K10
NA	VCCINT	K17
NA	VCCINT	K18
NA	VCCINT	K25
NA	VCCINT	L11
NA	VCCINT	L24
NA	VCCINT	M12
NA	VCCINT	M23
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N19
NA	VCCINT	N20
NA	VCCINT	N21