AMD Xilinx - XCV100E-6PQ240C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	81920
Number of I/O	158
Number of Gates	128236
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv100e-6pq240c

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state buses. Four partitionable bus lines are provided per CLB row, permitting multiple buses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

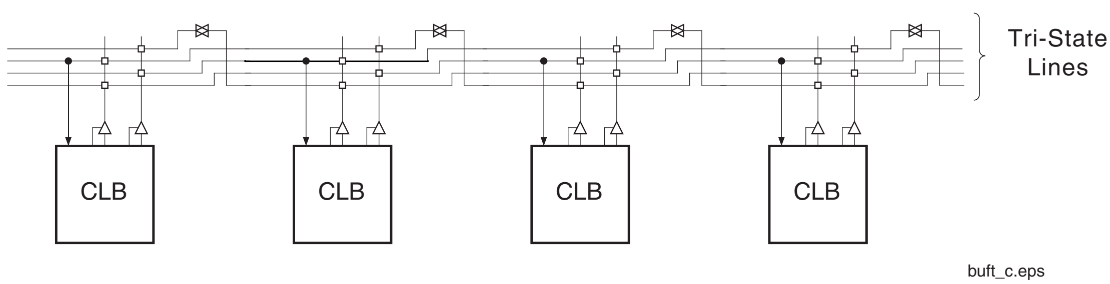

Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

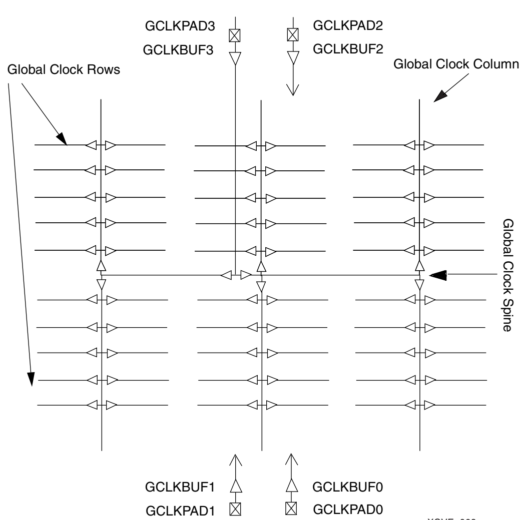

Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

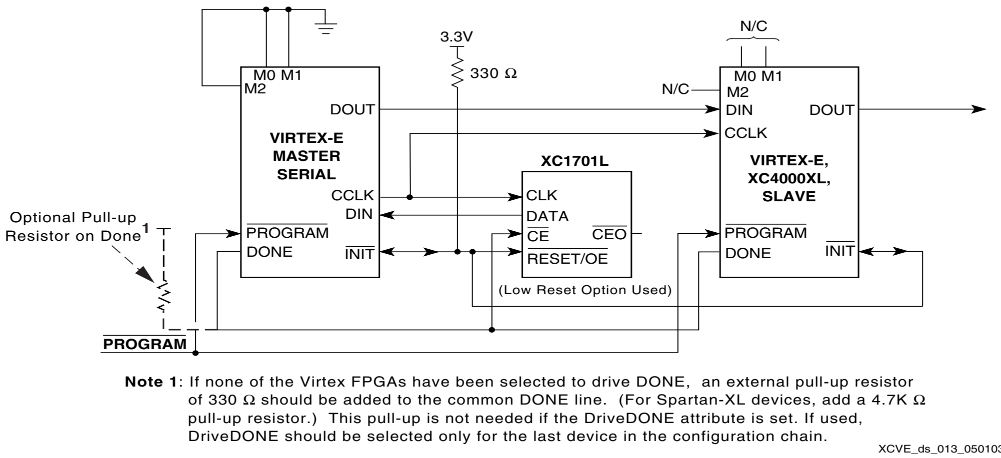

Figure 13: **Master/Slave Serial Mode Circuit Diagram**

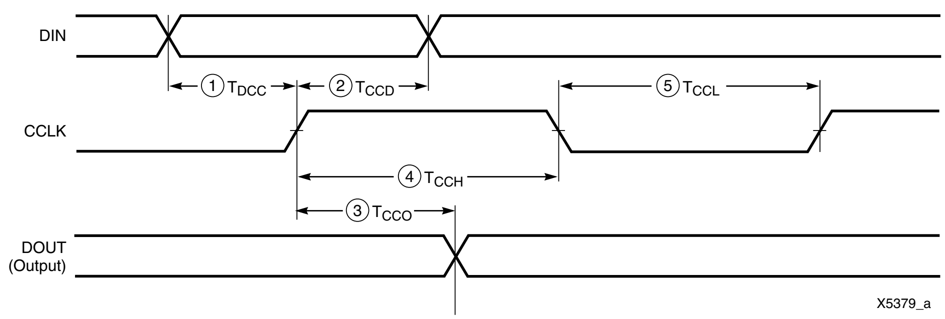

Figure 14: **Slave-Serial Mode Programming Switching Characteristics**

Master-Serial Mode

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The maximum capacity for a single LOUT/DOUT write is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,4000 bits.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK, which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

In a full master/slave system (Figure 13), the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM RESET pin is driven by INIT, and the CE input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

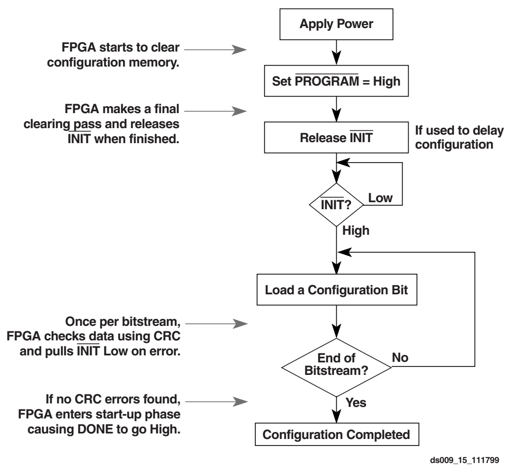

Figure 15: **Serial Configuration Flowchart**

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16.

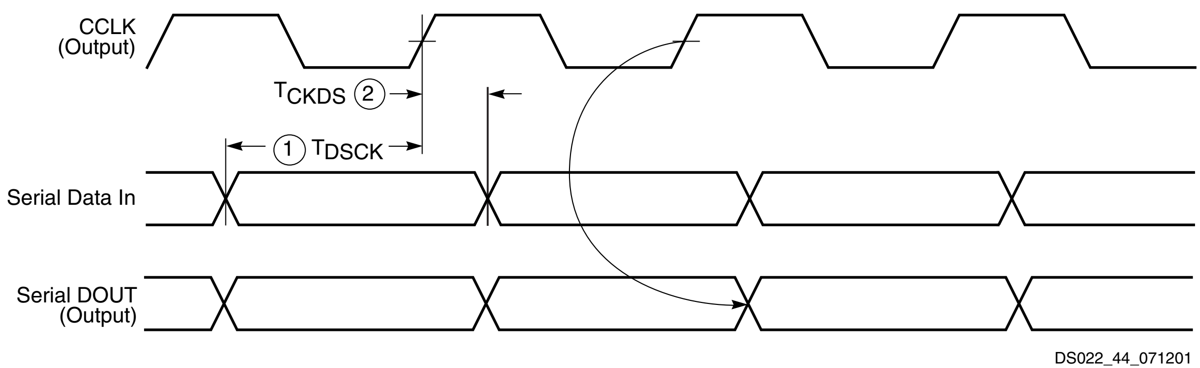

Figure 16: **Master-Serial Mode Programming Switching Characteristics**

At power-up, V_{CC} must rise from 1.0 V to V_{CC} Min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 17.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or de-asserted. Otherwise, an abort is initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.

VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (

INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 37. The extension

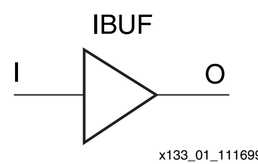

Figure 37: **Input Buffer (IBUF) Symbols**

to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a V_{REF}, the IBUF automatically configures as a differential amplifier input buffer. The V_{REF} voltage must be supplied on the V_{REF} pins. In the case of LVDS, LVPECL, and BLVDS, V_{REF} is not required.

Virtex-E Electrical Characteristics

Definition of Terms

Electrical and switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance: These speed files are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These speed files are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production: These speed files are released once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

Table 1 correlates the current status of each Virtex-E device with a corresponding speed file designation.

Table 1: **Virtex-E Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XCV50E			–8, –7, –6
XCV100E			–8, –7, –6
XCV200E			–8, –7, –6
XCV300E			–8, –7, –6
XCV400E			–8, –7, –6
XCV600E			–8, –7, –6
XCV1000E			–8, –7, –6
XCV1600E			–8, –7, –6
XCV2000E			–8, –7, –6
XCV2600E			–8, –7, –6
XCV3200E			–8, –7, –6

All specifications are subject to change without notice.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in **IOB Output Switching Characteristics Standard Adjustments**, page 10.	T_{ICKOF}	XCV50E	1.5	4.2	4.4	4.6	ns
		XCV100E	1.5	4.2	4.4	4.6	ns
		XCV200E	1.5	4.3	4.5	4.7	ns
		XCV300E	1.5	4.3	4.5	4.7	ns
		XCV400E	1.5	4.4	4.6	4.8	ns
		XCV600E	1.6	4.5	4.7	4.9	ns
		XCV1000E	1.7	4.6	4.8	5.0	ns
		XCV1600E	1.8	4.7	4.9	5.1	ns
		XCV2000E	1.8	4.8	5.0	5.2	ns
		XCV2600E	2.0	5.0	5.2	5.4	ns
		XCV3200E	2.2	5.2	5.4	5.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 3 and Table 4.

BG432 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 13: **BG432 Differential Pin Pair Summary XCV300E, XCV400E, XC600E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	AL16	AH15	NA	IO_DLL_L86P
1	5	AK16	AL17	NA	IO_DLL_L86N
2	1	A16	B16	NA	IO_DLL_L16P
3	0	D17	C17	NA	IO_DLL_L16N
IO LVDS Total Outputs: 137, Asynchronous Output Pairs: 63					
0	0	D27	B29	1	-
1	0	C27	B28	√	-
2	0	A28	D26	√	VREF
3	0	C26	B27	2	-
4	0	A27	D25	√	-
5	0	C25	D24	√	VREF
6	0	D23	B25	1	-
7	0	B24	C24	1	VREF
8	0	A24	D22	√	VREF
9	0	B22	C22	√	-
10	0	D20	C21	√	-
11	0	C20	B21	√	-
12	0	D19	A20	√	-
13	0	A19	B19	√	VREF
14	0	D18	B18	1	-
15	0	B17	C18	1	VREF
16	1	B16	C17	NA	IO_LVDS_DLL
17	1	B15	A15	1	VREF
18	1	D15	C15	1	-
19	1	A13	B14	√	VREF
20	1	D14	B13	√	-
21	1	B12	C13	√	-
22	1	C12	D13	√	-
23	1	C11	D12	√	-
24	1	C10	B10	√	VREF
25	1	D10	C9	1	VREF
26	1	B8	A8	1	-
27	1	B7	C8	√	VREF
28	1	A6	D8	√	-
29	1	D7	B6	2	-
30	1	C6	A5	√	VREF
31	1	D6	B5	√	-
32	1	C5	A4	1	-
33	1	D5	B4	√	CS, WRITE
34	2	D3	C2	√	DIN, D0, BUSY
35	2	D2	E4	3	-
36	2	D1	E3	4	-
37	2	E2	F4	1	VREF
38	2	E1	F3	5	-
39	2	F2	G4	1	-
40	2	G3	G2	√	VREF
41	2	H3	H2	4	-
42	2	H1	J4	1	VREF
43	2	J2	K4	√	D1
44	2	K2	K1	√	D2
45	2	L2	M4	4	-
46	2	M3	M2	1	-
47	2	N4	N3	1	-

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
1	IO_L43N_Y	C5	
1	IO_VREF_L43P_Y	E7	3
1	IO_WRITE_L44N_YY	D6	
1	IO_CS_L44P_YY	A2	
2	IO	D3	
2	IO	F3	
2	IO	G1	
2	IO	J2	
2	IO_DOUT_BUSY_L45P_YY	D4	
2	IO_DIN_D0_L45N_YY	E4	
2	IO_L46P_Y	F5	
2	IO_VREF_L46N_Y	B3	3
2	IO_L47P_Y	F4	
2	IO_L47N_Y	C1	
2	IO_VREF_L48P_Y	G5	
2	IO_L48N_Y	E3	
2	IO_L49P_Y	D2	
2	IO_L49N_Y	G4	
2	IO_L50P_Y	H5	
2	IO_L50N_Y	E2	
2	IO_VREF_L51P_YY	H4	
2	IO_L51N_YY	G3	
2	IO_L52P_Y	J5	
2	IO_VREF_L52N_Y	F1	1
2	IO_L53P_Y	J4	
2	IO_L53N_Y	H3	
2	IO_VREF_L54P_Y	K5	4
2	IO_L54N_Y	H2	
2	IO_L55P_Y	J3	
2	IO_L55N_Y	K4	
2	IO_VREF_L56P_YY	L5	
2	IO_D1_L56N_YY	K3	
2	IO_D2_L57P_YY	L4	
2	IO_L57N_YY	K2	

Table 14: **BG560 — XCV400E, XCV600E, XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin#	See Note
2	IO_L58P_Y	M5	
2	IO_L58N_Y	L3	
2	IO_L59P_Y	L1	
2	IO_L59N_Y	M4	
2	IO_VREF_L60P_Y	N5	3
2	IO_L60N_Y	M2	
2	IO_L61P_Y	N4	
2	IO_L61N_Y	N3	
2	IO_L62P_Y	N2	
2	IO_L62N_Y	P5	
2	IO_VREF_L63P_YY	P4	
2	IO_D3_L63N_YY	P3	
2	IO_L64P_Y	P2	
2	IO_L64N_Y	R5	
2	IO_L65P_Y	R4	
2	IO_L65N_Y	R3	
2	IO_VREF_L66P_Y	R1	
2	IO_L66N_Y	T4	
2	IO_L67P_Y	T5	
2	IO_VREF_L67N_Y	T3	2
2	IO_L68P_YY	T2	
2	IO_L68N_YY	U3	
3	IO	AE3	
3	IO	AF3	
3	IO	AH3	
3	IO	AK3	
3	IO_VREF_L69P_Y	U1	2
3	IO_L69N_Y	U2	
3	IO_L70P_Y	V2	
3	IO_VREF_L70N_Y	V4	
3	IO_L71P_Y	V5	
3	IO_L71N_Y	V3	
3	IO_L72P_Y	W1	
3	IO_L72N_Y	W3	

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
1	IO_L11N_Y	A10
1	IO_L11P_Y	D10
1	IO_L12N_YY	C10
1	IO_L12P_YY	A11
1	IO_L13N_YY	B11
1	IO_VREF_L13P_YY	E11[1]
1	IO_L14N_Y	A12
1	IO_L14P_Y	D11
1	IO_L15N_YY	A13
1	IO_VREF_L15P_YY	C11
1	IO_L16N_YY	B12
1	IO_L16P_YY	D12
1	IO_VREF_L17N_Y	A14[2]
1	IO_L17P_Y	C12
1	IO_WRITE_L18N_YY	C13
1	IO_CS_L18P_YY	B13
2	IO_DOUT_BUSY_L19P_YY	C15
2	IO_DIN_D0_L19N_YY	D14
2	IO_L20P	B16
2	IO_VREF_L20N	E13[2]
2	IO_L21P_YY	C16
2	IO_L21N_YY	E14
2	IO_VREF_L22P_Y	F13
2	IO_L22N_Y	E15
2	IO_L23P	F12
2	IO_L23N	D16
2	IO_VREF_L24P_Y	F14[1]
2	IO_D1_L24N_Y	E16
2	IO_D2_L25P_YY	F15
2	IO_L25N_YY	G13
2	IO_L26P	F16
2	IO_L26N	G12
2	IO_L27P_YY	G15
2	IO_L27N_YY	G14

Table 16: **FG256 Package — XCV50E, XCV100E, XCV200E, XCV300E**

Bank	Pin Description	Pin #
2	IO_VREF_L28P_Y	H13
2	IO_D3_L28N_Y	G16
2	IO_L29P	J13
2	IO_L29N	H15
2	IO_L30P_YY	H14
2	IO_L30N_YY	H16
3	IO	J15
3	IO_L31P	K15
3	IO_L31N	J14
3	IO_D4_L32P_Y	J16
3	IO_VREF_L32N_Y	K16
3	IO_L33P_YY	K12
3	IO_L33N_YY	L15
3	IO_L34P	K13
3	IO_L34N	L16
3	IO_L35P_YY	K14
3	IO_D5_L35N_YY	M16
3	IO_D6_L36P_Y	N16
3	IO_VREF_L36N_Y	L13[1]
3	IO_L37P	P16
3	IO_L37N	L12
3	IO_L38P_Y	M15
3	IO_VREF_L38N_Y	L14
3	IO_L39P_YY	M14
3	IO_L39N_YY	R16
3	IO_VREF_L40P	M13[2]
3	IO_L40N	T15
3	IO_D7_L41P_YY	N14
3	IO_INIT_L41N_YY	N15
4	GCK0	N8
4	IO	P10
4	IO_L42P_YY	T14
4	IO_L42N_YY	P13

Table 18: **FG456 — XCV200E and XCV300E**

Bank	Pin Description	Pin #
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	M9
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	L9
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11
NA	GND	K10
NA	GND	K9
NA	GND	J14
NA	GND	J13
NA	GND	J12
NA	GND	J11
NA	GND	J10
NA	GND	J9
NA	GND	C20
NA	GND	C3
NA	GND	B21
NA	GND	B2
NA	GND	A22
NA	GND	A1

Note 1: NC in the XCV200E device.

FG456 Differential Pin Pairs

Virtex-E devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package. Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair are in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs than can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 19: **FG456 Differential Pin Pair Summary XCV200E, XCV300E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
0	4	W12	U12	NA	IO_DLL_L75P
1	5	Y11	AA11	NA	IO_DLL_L75N
2	1	A11	D11	NA	IO_DLL_L13P
3	0	C11	B11	NA	IO_DLL_L13N
IO LVDS Total Pairs: 119, Asynchronous Output Pairs: 69					
0	0	B3	D5	NA	-
1	0	E6	B4	√	VREF
2	0	E7	A4	NA	-
3	0	D6	C6	√	VREF
4	0	B6	A5	1	-
5	0	C7	D7	1	-
6	0	B7	E8	√	VREF
7	0	E9	A7	√	-
8	0	B8	C8	1	-
9	0	A8	D9	1	-
10	0	E10	C9	NA	-
11	0	C10	A9	√	VREF
12	0	B10	F11	2	-
13	1	D11	B11	NA	IO_LVDS_DLL
14	1	D12	C12	2	-
15	1	A13	B12	2	-
16	1	B13	E12	√	VREF
17	1	D13	C13	√	-

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
0	IO_L9N	A7
0	IO_L9P	D9
0	IO_L10N	B8
0	IO_VREF_L10P	G10
0	IO_L11N_YY	C9
0	IO_L11P_YY	F10
0	IO_L12N_Y	A8
0	IO_L12P_Y	E10
0	IO_L13N_YY	G11
0	IO_L13P_YY	D10
0	IO_L14N_YY	B10
0	IO_L14P_YY	F11
0	IO_L15N	C10
0	IO_L15P	E11
0	IO_L16N_YY	G12
0	IO_L16P_YY	D11
0	IO_VREF_L17N_YY	C11
0	IO_L17P_YY	F12
0	IO_L18N_YY	A11
0	IO_L18P_YY	E12
0	IO_L19N_Y	D12
0	IO_L19P_Y	C12
0	IO_VREF_L20N_Y	A12
0	IO_L20P_Y	H13
0	IO_LVDS_DLL_L21N	B13
1	GCK2	C13
1	IO	A13[1]
1	IO	A16[1]
1	IO	A19
1	IO	A20
1	IO	A22
1	IO	A24[1]
1	IO	B15[1]
1	IO	B17[1]
1	IO	B23
1	IO_LVDS_DLL_L21P	F14
1	IO_L22N	E14
1	IO_L22P	F13
1	IO_L23N_Y	D14
1	IO_VREF_L23P_Y	A14
1	IO_L24N_Y	C14
1	IO_L24P_Y	H14
1	IO_L25N_YY	G14
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_VREF_L35P_Y	B19[2]
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	NC	L2
NA	NC	F6
NA	NC	F25
NA	NC	F21
NA	NC	F2
NA	NC	C26
NA	NC	C25
NA	NC	C2
NA	NC	C1
NA	NC	B6
NA	NC	B26
NA	NC	B24
NA	NC	B21
NA	NC	B16
NA	NC	B11
NA	NC	B1
NA	NC	AF25
NA	NC	AF24
NA	NC	AF2
NA	NC	AE6
NA	NC	AE3
NA	NC	AE26
NA	NC	AE24
NA	NC	AE21
NA	NC	AE16
NA	NC	AE14
NA	NC	AE11
NA	NC	AE1
NA	NC	AD25
NA	NC	AD2
NA	NC	AD1
NA	NC	AA6
NA	NC	AA25
NA	NC	AA21
NA	NC	AA2
NA	NC	A3
NA	NC	A25

Table 20: **FG676 — XCV400E, XCV600E**

Bank	Pin Description	Pin #
NA	NC	A2
NA	NC	A15
NA	VCCINT	G7
NA	VCCINT	G20
NA	VCCINT	H8
NA	VCCINT	H19
NA	VCCINT	J9
NA	VCCINT	J10
NA	VCCINT	J11
NA	VCCINT	J16
NA	VCCINT	J17
NA	VCCINT	J18
NA	VCCINT	K9
NA	VCCINT	K18
NA	VCCINT	L9
NA	VCCINT	L18
NA	VCCINT	T9
NA	VCCINT	T18
NA	VCCINT	U9
NA	VCCINT	U18
NA	VCCINT	V9
NA	VCCINT	V10
NA	VCCINT	V11
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	Y7
NA	VCCINT	Y20
NA	VCCINT	W8
NA	VCCINT	W19
0	VCCO	J13
0	VCCO	J12
0	VCCO	H9
0	VCCO	H12
0	VCCO	H11

FG860 Fine-Pitch Ball Grid Array Package

XCV1000E, XCV1600E, and XCV2000E devices in the FG680 fine-pitch Ball Grid Array package have footprint compatibility. Pins labeled I0_VREF can be used as either in all parts unless device-dependent as indicated in the footnotes. If the pin is not used as V_{REF}, it can be used as general I/O. Immediately following Table 24, see Table 25 for Differential Pair information.

Table 24: **FG860 — XCV1000E, XCV1600E, XCV2000E**

Bank	Pin Description	Pin #
0	GCK3	C22
0	IO	A26
0	IO	B31
0	IO	B34
0	IO	C24
0	IO	C29
0	IO	C34
0	IO	D24
0	IO	D36
0	IO	D40
0	IO	E26
0	IO	E28
0	IO	E35
0	IO_L0N_Y	A38
0	IO_L0P_Y	D38
0	IO_L1N_Y	B37
0	IO_L1P_Y	E37
0	IO_VREF_L2N_Y	A37
0	IO_L2P_Y	C39
0	IO_L3N_Y	B36
0	IO_L3P_Y	C38
0	IO_L4N_YY	A36
0	IO_L4P_YY	B35
0	IO_VREF_L5N_YY	A35
0	IO_L5P_YY	D37
0	IO_L6N_Y	C37
0	IO_L6P_Y	A34
0	IO_L7N_Y	E36
0	IO_L7P_Y	B33
0	IO_L8N_YY	A33
0	IO_L8P_YY	C32
0	IO_VREF_L9N_YY	C36
0	IO_L9P_YY	B32
0	IO_L10N_Y	A32
0	IO_L10P_Y	D35
0	IO_VREF_L11N_Y	C31[2]
0	IO_L11P_Y	C35
0	IO_L12N_YY	E34
0	IO_L12P_YY	A31
0	IO_VREF_L13N_YY	D34
0	IO_L13P_YY	C30
0	IO_L14N_Y	B30
0	IO_L14P_Y	E33
0	IO_L15N_Y	A30
0	IO_L15P_Y	D33
0	IO_VREF_L16N_YY	C33
0	IO_L16P_YY	B29
0	IO_L17N_YY	E32
0	IO_L17P_YY	A29
0	IO_L18N_Y	D32
0	IO_L18P_Y	C28
0	IO_L19N_Y	E31
0	IO_L19P_Y	B28
0	IO_L20N_Y	D31
0	IO_L20P_Y	A28
0	IO_L21N_Y	D30
0	IO_L21P_Y	C27
0	IO_L22N_YY	E29
0	IO_L22P_YY	B27
0	IO_VREF_L23N_YY	D29
0	IO_L23P_YY	A27
0	IO_L24N_Y	C26
0	IO_L24P_Y	D28
0	IO_L25N_Y	B26
0	IO_L25P_Y	F27
0	IO_L26N_YY	E27
0	IO_L26P_YY	C25

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO	J20[5]
1	IO	L18[4]
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N_YY	B16
1	IO_VREF_L35P_YY	F16[2]
1	IO_L36N_YY	A16
1	IO_L36P_YY	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N_Y	A17
1	IO_L39P_Y	E17
1	IO_L40N_Y	F17
1	IO_L40P_Y	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N_Y	B19
1	IO_L43P_Y	G18
1	IO_L44N_Y	D19
1	IO_L44P_Y	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19[1]
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L47N_Y	D20[4]
1	IO_L47P_Y	A20[4]
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L50N_YY	B21[4]
1	IO_L50P_YY	D21[4]
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N_YY	H19
1	IO_L53P_YY	B22
1	IO_L54N_YY	E21
1	IO_L54P_YY	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N_Y	G21
1	IO_L57P_Y	A23
1	IO_L58N_Y	A24
1	IO_L58P_Y	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N_Y	E23
1	IO_L61P_Y	C25
1	IO_L62N_Y	D24
1	IO_L62P_Y	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L65N_Y	C26[4]
1	IO_L65P_Y	F23[4]
1	IO_L66N_Y	B27
1	IO_VREF_L66P_Y	G23[1]
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_L68N_YY	B28[3]
1	IO_L68P_YY	A28[4]
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
3	IO_L127P_YY	Y24
3	IO_VREF_L127N_YY	AB28
3	IO_L128P_YY	AC30
3	IO_L128N_YY	AA25
3	IO_L129P	W21
3	IO_L129N	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P_YY	AC26
3	IO_L133N_YY	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P	AF29
3	IO_VREF_L135N	AB24
3	IO_L136P_YY	AB23
3	IO_L136N_YY	AE28
3	IO_L137P_Y	AG30[3]
3	IO_L137N_Y	AC25[4]
3	IO_L138P_YY	AE26
3	IO_VREF_L138N_YY	AG29[1]
3	IO_L139P	AH30
3	IO_L139N	AC24
3	IO_L140P	AF28[3]
3	IO_L140N	AD25[4]
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19[4]
4	IO	AC16[4]
4	IO	AC19
4	IO	AD18[4]
4	IO	AD21[4]

Table 26: **FG900 — XCV600E, XCV1000E, XCV1600E**

Bank	Pin Description	Pin #
4	IO	AE15[4]
4	IO	AE18[4]
4	IO	AE21
4	IO	AE24[5]
4	IO	AF17[5]
4	IO	AF18[5]
4	IO	AJ18[4]
4	IO	AK18
4	IO	AK25[5]
4	IO	AK27[4]
4	IO	AH23[4]
4	IO	AH24[5]
4	IO_L142P_YY	AF27
4	IO_L142N_YY	AK28
4	IO_L143P_YY	AG26[4]
4	IO_L143N_YY	AH27[3]
4	IO_L144P	AD23
4	IO_L144N	AJ27
4	IO_VREF_L145P	AB21[1]
4	IO_L145N	AF25
4	IO_L146P	AC22[4]
4	IO_L146N	AH26[4]
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
4	IO_L178N_YY	AL28
4	IO_L179P_YY	AE24[4]
4	IO_L179N_YY	AN28[5]
4	IO_L180P_Y	AJ27
4	IO_L180N_Y	AH26
4	IO_L181P_Y	AG25
4	IO_L181N_Y	AK27
4	IO_L182P	AM28[4]
4	IO_L182N	AF24[5]
4	IO_L183P_YY	AJ26
4	IO_L183N_YY	AP27
4	IO_VREF_L184P_YY	AK26
4	IO_L184N_YY	AN27
4	IO_L185P	AE23[4]
4	IO_L185N	AM27[5]
4	IO_L186P_Y	AL26
4	IO_L186N_Y	AP26
4	IO_VREF_L187P_Y	AN26[2]
4	IO_L187N_Y	AJ25
4	IO_L188P	AG24[4]
4	IO_L188N	AP25[5]
4	IO_L189P_YY	AF23
4	IO_L189N_YY	AM26
4	IO_VREF_L190P_YY	AJ24
4	IO_L190N_YY	AN25
4	IO_L191P_Y	AE22
4	IO_L191N_Y	AM25
4	IO_L192P_Y	AK24
4	IO_L192N_Y	AH23
4	IO_VREF_L193P_YY	AF22
4	IO_L193N_YY	AP24
4	IO_L194P_YY	AL24
4	IO_L194N_YY	AK23
4	IO_L195P_Y	AG22
4	IO_L195N_Y	AN23
4	IO_L196P_Y	AP23
4	IO_L196N_Y	AM23
4	IO_L197P_Y	AH22
4	IO_L197N_Y	AP22
4	IO_L198P_Y	AL23
4	IO_L198N_Y	AF21
4	IO_L199P_YY	AL22
4	IO_L199N_YY	AJ22
4	IO_VREF_L200P_YY	AK22
4	IO_L200N_YY	AM22
4	IO_L201P_YY	AG21[4]
4	IO_L201N_YY	AJ21[5]
4	IO_L202P_Y	AP21
4	IO_L202N_Y	AE20
4	IO_L203P_Y	AH21
4	IO_L203N_Y	AL21
4	IO_L204P	AN21[4]
4	IO_L204N	AF20[5]
4	IO_L205P_YY	AK21
4	IO_L205N_YY	AP20
4	IO_VREF_L206P_YY	AE19
4	IO_L206N_YY	AN20
4	IO_L207P_Y	AG20[4]
4	IO_L207N_Y	AL20[5]
4	IO_L208P_Y	AH20
4	IO_L208N_Y	AK20
4	IO_L209P_Y	AN19
4	IO_L209N_Y	AJ20
4	IO_L210P	AF19[4]
4	IO_L210N	AP19[5]
4	IO_L211P_YY	AM19
4	IO_L211N_YY	AH19
4	IO_VREF_L212P_YY	AJ19

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	AP2
NA	GND	AN3
NA	GND	AM20
NA	GND	AK30
NA	GND	AG8
NA	GND	AC29
NA	GND	Y3
NA	GND	Y32
NA	GND	W21
NA	GND	V21
NA	GND	T8
NA	GND	T27
NA	GND	R21
NA	GND	P21
NA	GND	H19
NA	GND	F29
NA	GND	C11
NA	GND	B3
NA	GND	A32
NA	GND	AP3
NA	GND	AN32
NA	GND	AM24
NA	GND	AJ6
NA	GND	AG16
NA	GND	AA14
NA	GND	Y14
NA	GND	W8
NA	GND	W27
NA	GND	U14
NA	GND	T14
NA	GND	R3
NA	GND	R32
NA	GND	M6
NA	GND	H27

Table 28: **FG1156 — XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Bank	Pin Description	Pin #
NA	GND	E5
NA	GND	C15
NA	GND	B32
NA	GND	A33
NA	GND	AP7
NA	GND	AN33
NA	GND	AM32
NA	GND	AJ12
NA	GND	AG19
NA	GND	AA15
NA	GND	Y15
NA	GND	W14
NA	GND	V14
NA	GND	U15
NA	GND	T15
NA	GND	R14
NA	GND	P14
NA	GND	M29
NA	GND	G1
NA	GND	E18
NA	GND	C20
NA	GND	B33
NA	GND	A34
NA	GND	AP28
NA	GND	AN34
NA	GND	AM33
NA	GND	AJ23
NA	GND	AG27
NA	GND	AA16
NA	GND	Y16
NA	GND	W15
NA	GND	V15
NA	GND	U16
NA	GND	T16

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
111	2	M31	R26	2600 1600	-
112	2	N30	P28	3200 1600 1000	-
113	2	N29	N33	2600 2000 1000	VREF
114	2	T25	N34	3200 2600 2000 1600	-
115	2	P34	R27	3200 2600 2000 1600 1000	-
116	2	P29	P31	3200 2600 1600 1000	-
117	2	P33	T26	3200 2600 2000	-
118	2	R34	R28	2600 2000 1000	-
119	2	N31	N32	2000 1600 1000	D3
120	2	P30	R33	2000 1600	-
121	2	R29	T34	3200 2600 2000 1600 1000	-
122	2	R30	T30	1000	-
123	2	T28	R31	3200 1600	-
124	2	T29	U27	3200 2600 1600 1000	-
125	2	T31	T33	2000 1600 1000	VREF
126	2	U28	T32	2000 1600 1000	-
127	2	U29	U33	3200 2600 1600 1000	VREF
128	2	V33	U31	3200 2600 2000 1600 1000	-
129	3	V26	V30	3200 2600 1600 1000	VREF
130	3	W34	V28	2000 1600 1000	-
131	3	W32	W30	2000 1600 1000	VREF
132	3	V29	Y34	3200 2600 1600 1000	-
133	3	W29	Y33	3200 1600	-
134	3	W26	W28	1000	-
135	3	Y31	Y30	3200 2600 2000 1600 1000	-
136	3	AA34	W31	2000 1600	-
137	3	AA33	Y29	2000 1600 1000	VREF
138	3	W25	AB34	2600 2000 1000	-
139	3	Y28	AB33	3200 2600 2000	-
140	3	AA30	Y26	3200 2600 1600 1000	-
141	3	Y27	AA31	3200 2600 2000 1600 1000	-
142	3	AA27	AA29	3200 2600 2000 1600	-
143	3	AB32	AB29	2600 2000 1000	VREF
144	3	AA28	AC34	3200 1600 1000	-
145	3	Y25	AD34	2600 1600	-
146	3	AB30	AC33	3200 2600 1600 1000	-
147	3	AA26	AC32	2000 1000	-
148	3	AD33	AB28	3200 2600 2000	-
149	3	AE34	AB27	3200 2600 2000 1600 1000	D5
150	3	AE33	AC30	2000 1600 1000	VREF
151	3	AA25	AE32	3200 1600 1000	-
152	3	AE31	AD29	3200 2600 2000 1600 1000	-

Table 29: **FG1156 Differential Pin Pair Summary: XCV1000E, XCV1600E, XCV2000E, XCV2600E, XCV3200E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
231	5	AH14	AP12	3200 2600 2000 1600 1000	-
232	5	AJ14	AL14	3200 2600 1000	-
233	5	AF13	AN12	3200 2000 1000	-
234	5	AF14	AP11	3200 2000 1000	-
235	5	AN11	AH13	3200 1600 1000	-
236	5	AM12	AL12	3200 2600 2000 1600 1000	-
237	5	AJ13	AP10	3200 2600 2000 1600 1000	VREF
238	5	AK12	AM10	2600 1600 1000	-
239	5	AP9	AK11	2600 1600 1000	-
240	5	AL11	AL10	3200 2600 2000 1600 1000	VREF
241	5	AE13	AM9	3200 2600 2000 1600 1000	-
242	5	AF12	AP8	3200 2600	-
243	5	AL9	AH11	3200 2000 1000	VREF
244	5	AF11	AN8	3200 2000 1000	-
245	5	AM8	AG11	3200 1600	-
246	5	AL8	AK9	3200 2600 2000 1600 1000	VREF
247	5	AH10	AN7	3200 2600 2000 1600 1000	-
248	5	AE12	AJ9	3200 2600	-
249	5	AM7	AL7	3200 1000	-
250	5	AG10	AN6	3200 1000	-
251	5	AK8	AH9	2000 1600	-
252	5	AP5	AJ8	3200 2600 2000 1600 1000	VREF
253	5	AE11	AN5	3200 2600 2000 1600 1000	-
254	5	AF10	AM6	3200 2600 1000	-
255	5	AL6	AG9	3200 2000 1000	VREF
256	5	AH8	AP4	3200 2000 1000	-
257	5	AN4	AJ7	3200 1600 1000	-
258	5	AM5	AK6	3200 2600 2000 1600 1000	-
259	6	AF8	AH6	3200 2600 2000 1600 1000	-
260	6	AK3	AE9	3200 2600 2000	-
261	6	AL2	AD10	2600 2000 1000	-
262	6	AH4	AL1	3200 2600 1600 1000	VREF
263	6	AK1	AG6	2600 1600	-
264	6	AK2	AF7	3200 2600 1600 1000	-
265	6	AG5	AJ3	2600 2000 1000	VREF
266	6	AJ2	AD9	3200 2600 2000 1600	-
267	6	AH2	AC10	3200 2600 2000 1600 1000	-
268	6	AF5	AH3	3200 2600 1600 1000	-
269	6	AG3	AE8	3200 2600 2000	-